HARRIS SEMICONDUCTOR

CD74HC161, CD74HCT161, CD74HC163, CD74HCT163

High Speed CMOS Logic Presettable Counters

February 1998

Features

- **CD74HC161, CD74HCT161 4-Bit Binary Counter, Asynchronous Reset**
- **CD74HC163, CD74HCT163 4-Bit Binary Counter, Synchronous Reset**
- **Synchronous Counting and Loading**
- **Two Count Enable Inputs for n-Bit Cascading**
- **Look-Ahead Carry for High-Speed Counting**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC161E	-55 to 125	16 Ld PDIP	E16.3
CD74HC161M	-55 to 125	16 Ld SOIC	M16.15
CD74HC163E	-55 to 125	16 Ld PDIP	E16.3
CD74HC163M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT161E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT161M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT163E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT163M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Description

The Harris CD74HC161, CD74HCT161, CD74HC163 and CD74HCT163 are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The CD74HC161 and CD74HCT161 are asynchronous reset decade and binary counters, respectively; the CD74HC163 and CD74HCT163 devices decade and binary counters, respectively and are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, SPE, disables counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for SPE are met).

All counters are reset with a low level on the Master Reset input, MR. In the CD74HC163 and CD74HCT163 counters (synchronous reset types), the requirements for setup and hold time with respect to the clock must be met.

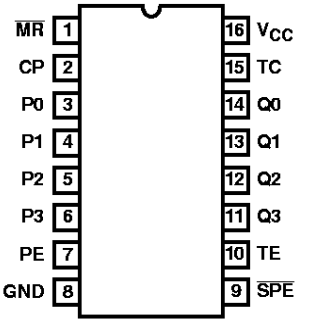
Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters reset action occurs regardless of the level of the $\overline{SPE}$, PE and TE inputs (and the clock input, CP, in the CD74HC161 and CD74HCT161 types).

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

Pinout

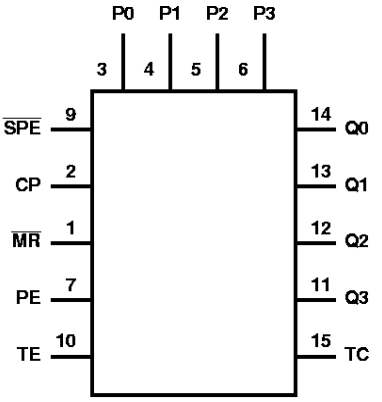
CD74HC161, CD74HCT161, CD74HC163, CD74HCT163
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1550.1**

Functional Diagram



MODE SELECT - FUNCTION TABLE FOR CD74HC/HCT161

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(Note 3)
Count	H	↑	h	h	h (Note 5)	X	Count	(Note 3)
Inhibit	H	X	l (Note 4)	X	h (Note 5)	X	q_n	(Note 3)
	H	X	X	l (Note 4)	h (Note 5)	X	q_n	L

MODE SELECT - FUNCTION TABLE FOR CD74HC/HCT163

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h (Note 5)	↑	X	X	l	l	L	L
	h (Note 5)	↑	X	X	l	h	H	(Note 3)
Count	h (Note 5)	↑	h	h	h (Note 5)	X	Count	(Note 3)
Inhibit	h (Note 5)	X	l (Note 4)	X	h (Note 5)	X	q_n	(Note 3)
	h (Note 5)	X	X	l (Note 4)	h (Note 5)	X	q_n	L

NOTE: H = High voltage level steady state; L = Low voltage level steady state; h = High voltage level one setup time prior to the Low-to-High clock transition; l = Low voltage level one setup time prior to the Low-to-High clock transition; X = Don't Care; q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition; ↑ = Low-to-High clock transition.

3. The TC output is High when TE is High and the counter is at Terminal Count (HHHH for CD74HC/HCT161 and CD74HC/HCT163).
4. The High-to-Low transition of PE or TE on the CD74HC/HCT161 and the CD74HC/HCT163 should only occur while CP is HIGH for conventional operation.
5. The Low-to-High transition of $\overline{SPE}$ on the CD74HC/HCT161 and $\overline{SPE}$ or $\overline{MR}$ on the CD74HC/HCT163 should only occur while CP is HIGH for conventional operation.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V. . . . . ±25mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 6) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 160
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
P0 - P3	0.25
PE	0.65
CP	1.05
$\overline{MR}$	0.8
$\overline{SPE}$	0.5
TE	1.05

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Maximum CP Frequency (Note7)	f_{MAX}	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	24	-	20	-	MHz
			6	35	-	-	28	-	24	-	MHz

Prerequisite For Switching Specifications **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CP Width (Low)	$t_{W(L)}$	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
$\overline{MR}$ Pulse Width (161)	t_W	-	2	100	-	-	125	-	150	-	ns
			4.5	20	-	-	25	-	30	-	ns
			6	17	-	-	21	-	26	-	ns
Setup Time, Pn to CP	t_{SU}	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Setup Time, PE or TE to CP	t_{SU}	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Setup Time, $\overline{SPE}$ to CP	t_{SU}	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Setup Time, $\overline{MR}$ to CP (163)	t_{SU}	-	2	65	-	-	80	-	100	-	ns
			4.5	13	-	-	16	-	20	-	ns
			6	11	-	-	14	-	17	-	ns
Hold Time, PN to CP	t_H	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Hold Time, TE or PE to CP	t_H	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
Hold Time, $\overline{SPE}$ to CP	t_H	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
Recovery Time, $\overline{MR}$ to CP (161)	t_{REC}	-	2	75	-	-	95	-	110	-	ns
			4.5	15	-	-	19	-	22	-	ns
			6	13	-	-	16	-	19	-	ns
HCT TYPES											
Maximum CP Frequency	f_{MAX}	-	4.5	30	-	-	24	-	20	-	MHz
CP Width (Low) (Note 7)	$t_{W(L)}$	-	4.5	16	-	-	20	-	24	-	ns
$\overline{MR}$ Pulse Width (161)	t_W	-	4.5	20	-	-	25	-	30	-	ns
Setup Time, Pn to CP	t_{SU}	-	4.5	10	-	-	13	-	15	-	ns
Setup Time, PE or TE to CP	t_{SU}	-	4.5	13	-	-	16	-	20	-	ns
Setup Time, $\overline{SPE}$ to CP	t_{SU}	-	4.5	12	-	-	15	-	18	-	ns
Setup Time, $\overline{MR}$ to CP (163)	t_{SU}	-	4.5	13	-	-	16	-	20	-	ns
Hold Time, PN to CP	t_H	-	4.5	5	-	-	5	-	5	-	ns
Hold Time, TE or PE to CP	t_H	-	4.5	3	-	-	3	-	3	-	ns

Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Hold Time, $\overline{SPE}$ to CP	t_H	-	4.5	3	-	-	3	-	3	-	ns
Recovery Time, $\overline{MR}$ to CP (161)	t_{REC}	-	4.5	15	-	-	19	-	22	-	ns

NOTE:

7. Applies to non-cascaded operation only. With cascaded counters clock to terminal count propagation delays, count enables (PE or TE)-to-clock setup times, and count enables (PE or TE)-to-clock hold times determine maximum clock frequency. For example with these HC devices:

$$f_{MAX}\ (CP) = \frac{1}{\text{CP-to-TC prop. delay} + \text{TE-to-CP setup} + \text{TE-to-CP Hold}} = \frac{1}{37 + 10 + 0} \approx 21\,\text{MHz(min)}$$

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CP to TC	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C_L = 15pF	5	-	15	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	31	-	39	-	48	ns
CP to Qn	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C_L = 15pF	5	-	15	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	31	-	39	-	48	ns
TE to TC	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	120	-	150	-	180	ns
			4.5	-	-	24	-	30	-	36	ns
		C_L = 15pF	5	-	9	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	20	-	26	-	31	ns
$\overline{MR}$ to Qn (161)	t_{PHL}	C_L = 50pF	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	36	-	45	-	54	ns
$\overline{MR}$ to TC (161)	t_{PHL}	C_L = 50pF	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		C_L = 50pF	6	-	-	36	-	45	-	54	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance (Notes 8, 9)	C_{PD}	-	5	-	60	-	-	-	-	-	pF

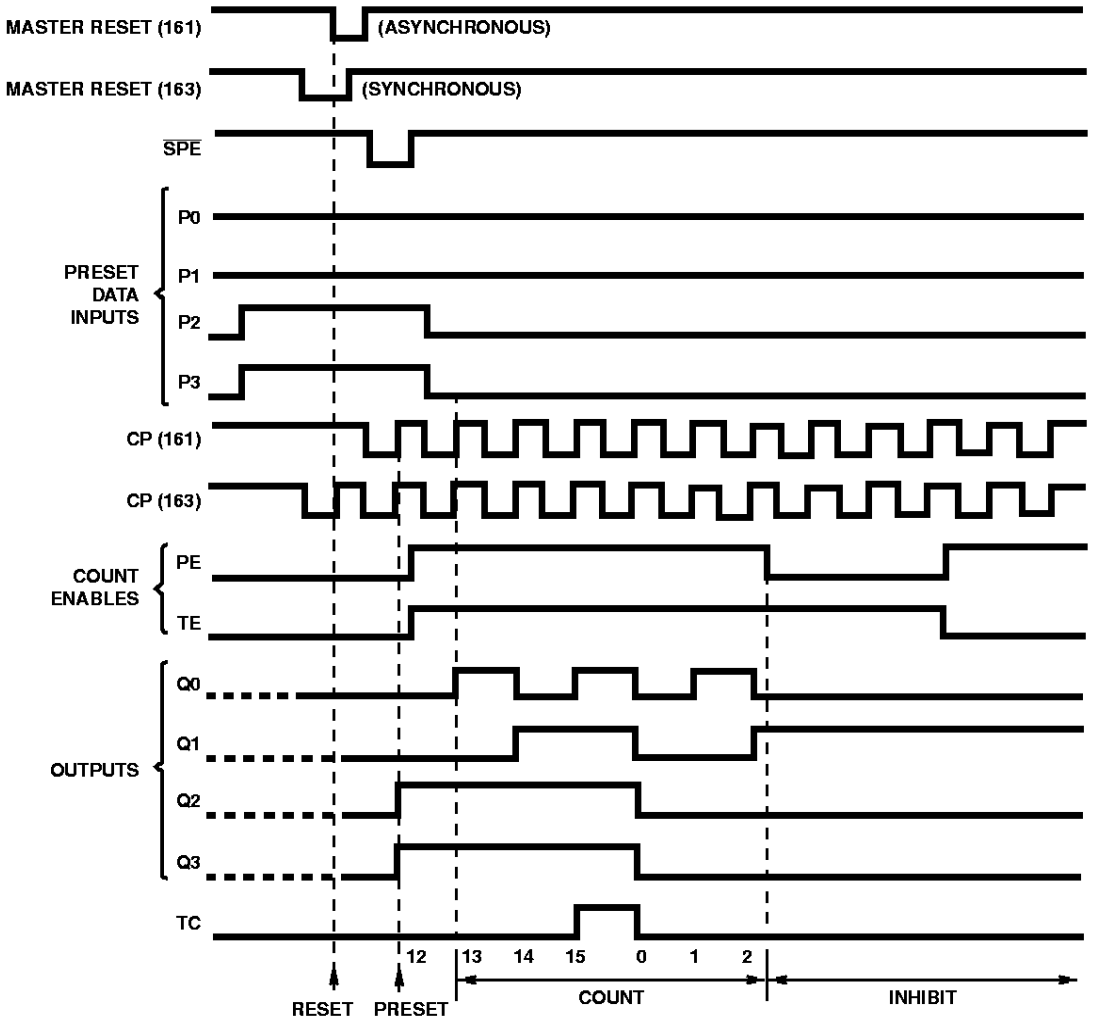
Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	C_L = 50pF	-	10	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay CP to TC	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
CP to Qn	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	39	-	49	-	59	ns
		C_L = 15pF	5	-	16	-	-	-	-	-	ns
TE to TC	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	32	-	40	-	48	ns
		C_L = 15pF	5	-	13	-	-	-	-	-	ns
$\overline{MR}$ to Qn (161)	t_{PHL}	C_L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
$\overline{MR}$ to TC (161)	t_{PHL}	C_L = 50pF	4.5	-	-	50	-	63	-	75	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance (Notes 6, 7)	C_{PD}	-	5	-	63	-	-	-	-	-	pF
Input Capacitance	C_{IN}	C_L = 50pF	-	10	-	10	-	10	-	10	pF

NOTES:

8. C_{PD} is used to determine the dynamic power consumption, per package.
9. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

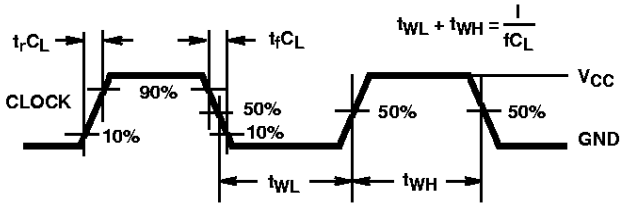
Timing Diagram



Sequence illustrated on waveforms:

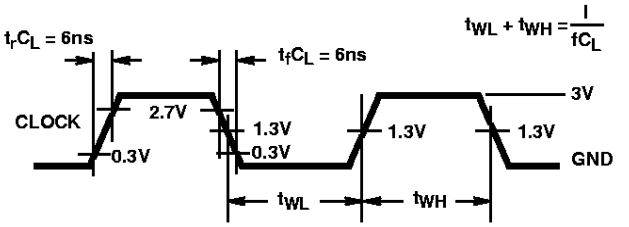
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

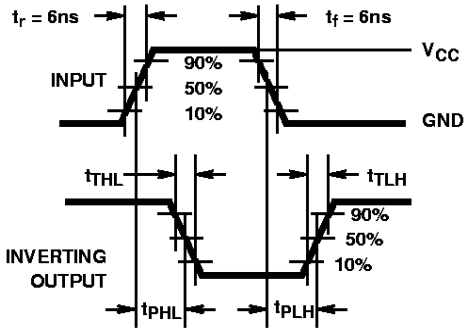


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

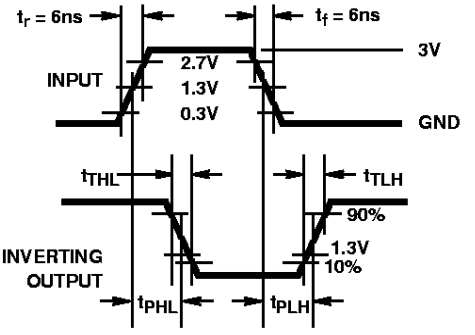


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

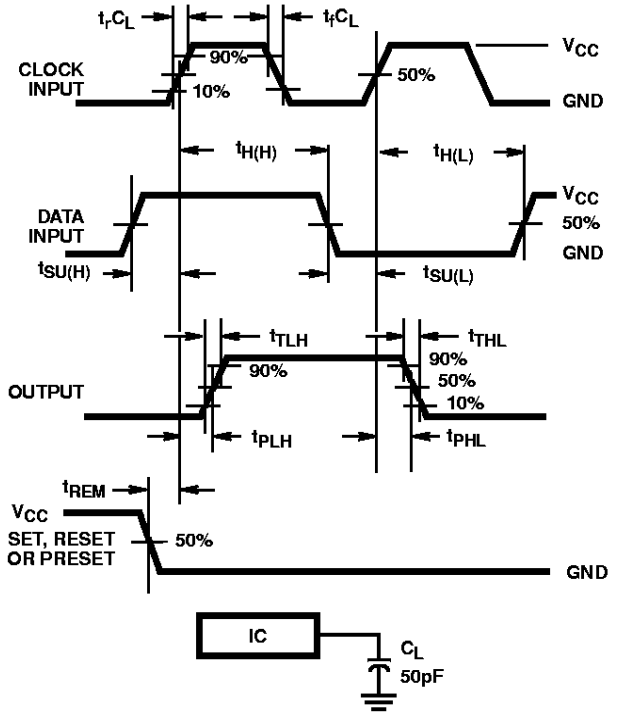


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

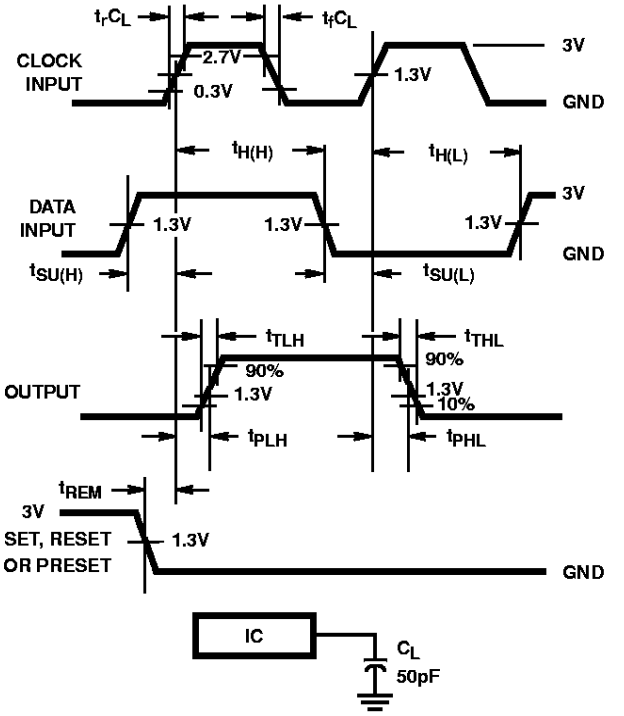


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS