

August 2014

# FQPF5P20

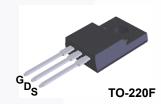
# P-Channel QFET<sup>®</sup> MOSFET -200 V, -3.4 A, 1.4 $\Omega$

### Description

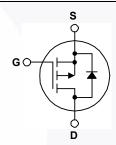
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### **Features**

- -3.4 A, -200 V, R<sub>DS(on)</sub> = 1.4  $\Omega$  (Max.) @ V<sub>GS</sub> = -10 V, I<sub>D</sub> = -1.7 A
- Low Gate Charge (Typ. 10 nC)
- Low C<sub>rss</sub> (Typ. 12 pF)
- · 100% Avalanche Tested







# **Absolute Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQPF5P20 FQPF5P20RDTU	Unit
$V_{DSS}$	Drain-Source Voltage		-200	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		-3.4	Α
	- Continuous (T <sub>C</sub> = 100°C)		-2.15	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	-13.6	Α
$V_{GSS}$	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		330	mJ
I <sub>AR</sub>	Avalanche Current		-3.4	Α
E <sub>AR</sub>	Repetitive Avalanche Energy		3.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		-5.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)		38	W
	- Derate Above 25°C		0.3	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.		300	°C

### **Thermal Characteristics**

Symbol	Parameter	FQPF5P20 FQPF5P20RDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max. 3.29		°C/W
R <sub>θJA</sub> Thermal Resistance, Junction-to-Ambient, Max.		62.5	C/VV

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQPF5P20	FQPF5P20	TO-220F	Tube	N/A	N/A	50 units
FQPF5P20RDTU	FQPF5P20	TO-220F (LG-formed)	Tube	N/A	N/A	50 units

# **Elerical Characteristics** $T_C = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-200			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 μA, Referenced to 25°C		-0.17		V/°C
I <sub>DSS</sub>	Zoro Cata Valtaga Prain Current	V <sub>DS</sub> = -200 V, V <sub>GS</sub> = 0 V		-	-1	μΑ
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -160 V, T <sub>C</sub> = 125°C		-	-10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V		-	-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V		-	100	nA
On Cha	aracteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-3.0		-5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.7 A		1.1	1.4	Ω
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -40 \text{ V}, I_{D} = -1.7 \text{ A}$		2.15		S
Dynam C <sub>iss</sub>	ic Characteristics Input Capacitance			220	420	
Uice	Input Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V},$		330		C
	<u>'</u>	DO 7 00 7		7.	430	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		75	98	pF
	<u>'</u>	DO 7 00 7		75 12		pF pF pF
C <sub>oss</sub> C <sub>rss</sub>	Output Capacitance	DO 7 00 7			98	pF
C <sub>oss</sub> C <sub>rss</sub> Switch	Output Capacitance Reverse Transfer Capacitance	f = 1.0 MHz			98	pF
C <sub>oss</sub> C <sub>rss</sub>	Output Capacitance Reverse Transfer Capacitance ing Characteristics	f = 1.0 MHz V <sub>DD</sub> = -100 V, I <sub>D</sub> = -4.8 A,		12	98 15	pF pF
$C_{oss}$ $C_{rss}$ Switch $t_{d(on)}$ $t_r$	Output Capacitance Reverse Transfer Capacitance  ing Characteristics  Turn-On Delay Time	f = 1.0 MHz		12	98 15 28	pF pF
$C_{oss}$ $C_{rss}$ Switch $t_{d(on)}$ $t_r$ $t_{d(off)}$	Output Capacitance Reverse Transfer Capacitance  ing Characteristics Turn-On Delay Time Turn-On Rise Time	f = 1.0 MHz V <sub>DD</sub> = -100 V, I <sub>D</sub> = -4.8 A,		9 70	98 15 28 150	pF pF
$C_{oss}$ $C_{rss}$ Switch	Output Capacitance Reverse Transfer Capacitance  ing Characteristics Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time	$f$ = 1.0 MHz $V_{DD}$ = -100 V, $I_{D}$ = -4.8 A, $R_{G}$ = 25 $\Omega$ (Note 4)		9 70 12	98 15 28 150 35	pF pF ns ns
$egin{array}{l} C_{oss} \\ C_{rss} \\ \hline {f Switch} \\ t_{d(on)} \\ t_{r} \\ t_{d(off)} \\ t_{f} \\ \hline \end{array}$	Output Capacitance Reverse Transfer Capacitance  ing Characteristics Turn-On Delay Time Turn-On Rise Time Turn-Off Delay Time Turn-Off Fall Time	f = 1.0  MHz $V_{DD} = -100 \text{ V}, I_{D} = -4.8 \text{ A},$ $R_{G} = 25 \Omega$	  	9 70 12 25	98 15 28 150 35 60	pF pF ns ns

## **Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-3.4	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				-13.6	Α
$V_{SD}$	Drain-Source Diode Forward Voltage V <sub>GS</sub> = 0 V, I <sub>S</sub> = -3.4 A				-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = -4.8 \text{ A},$		175		ns
Q <sub>rr</sub>	Reverse Recovery Charge dI <sub>F</sub> / dt = 100 A/μs			1.07		μС

- **Notes:**1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 42.8 mH,  $I_{AS}$  = -3.4 A,  $V_{DD}$  = -50 V,  $R_G$  = 25  $\Omega$ , starting  $T_J$  = 25°C. 3.  $I_{SD} \le$  -4.8 A, di/dt  $\le$  300 A/µs,  $V_{DD} \le$  BV $_{DSS}$ , starting  $T_J$  = 25°C. 4. Essentially independent of operating temperature.

# **Typical Characteristics**

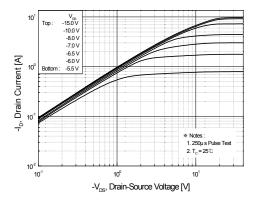


Figure 1. On-Region Characteristics

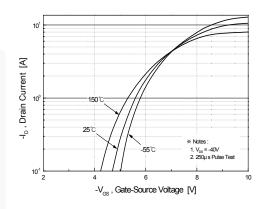


Figure 2. Transfer Characteristics

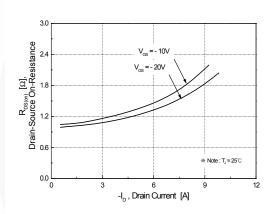


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

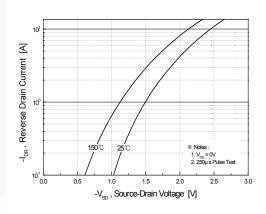


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

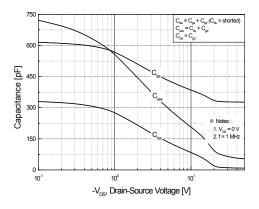


Figure 5. Capacitance Characteristics

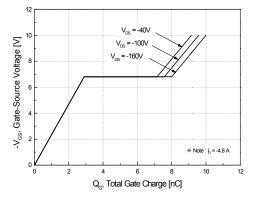
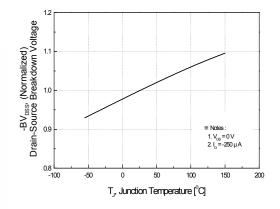


Figure 6. Gate Charge Characteristics

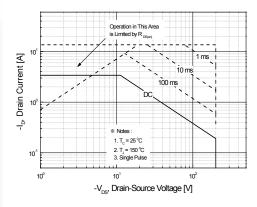
# Typical Characteristics (Continued)



25 (Notes: 1.7 (No

Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



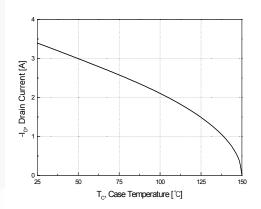


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

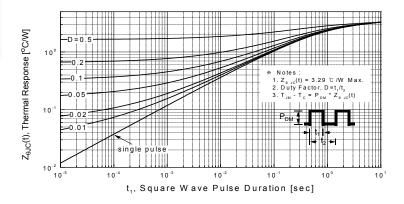


Figure 11. Transient Thermal Response Curve

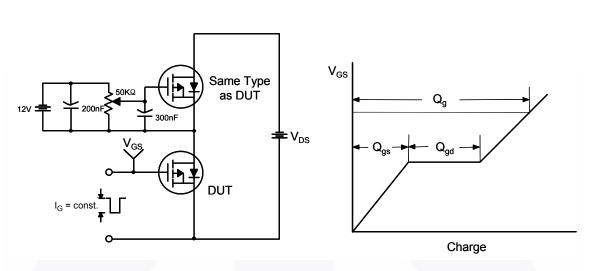


Figure 12. Gate Charge Test Circuit & Waveform

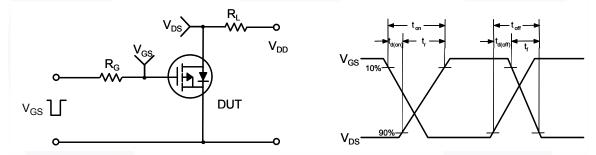


Figure 13. Resistive Switching Test Circuit & Waveforms

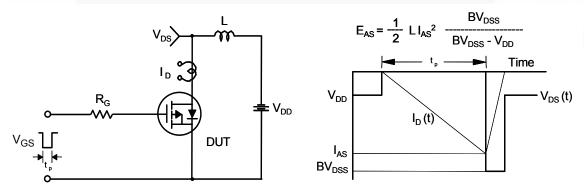
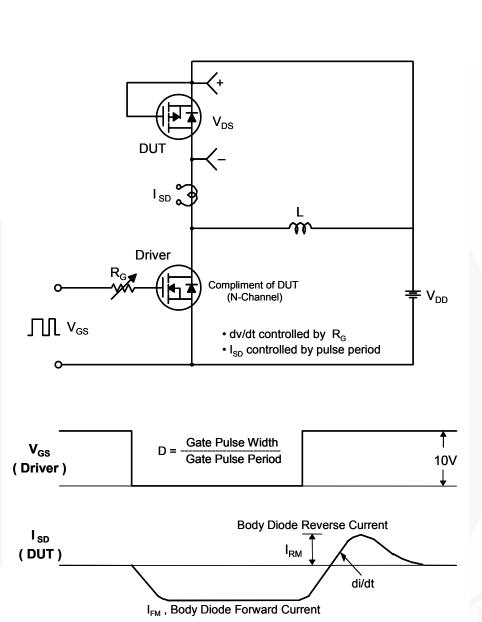


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



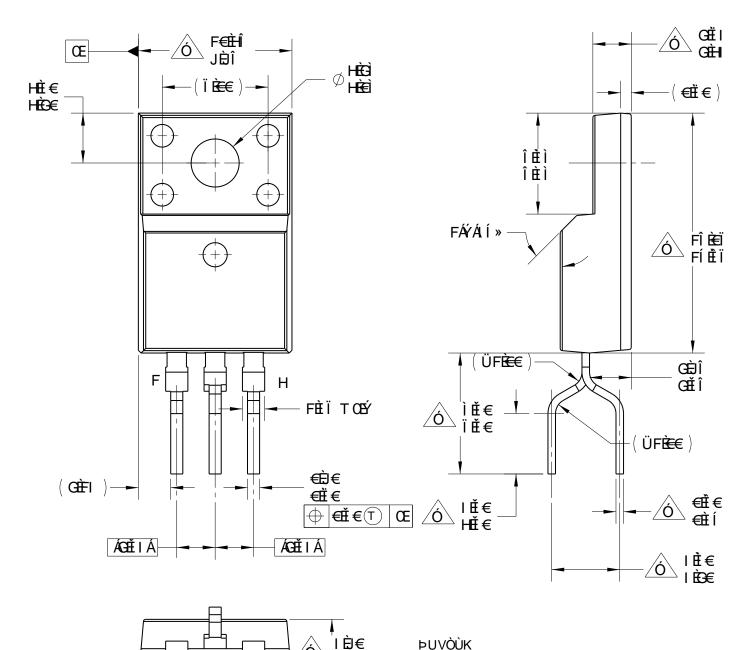
V<sub>DS</sub>
(DUT)

Body Diode
Forward Voltage Drop

Body Diode Recovery dv/dt

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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ĺ	PÓÜ ÖÖVÖÜ ÞÓ ÖÖÐÓ ÞÓ					
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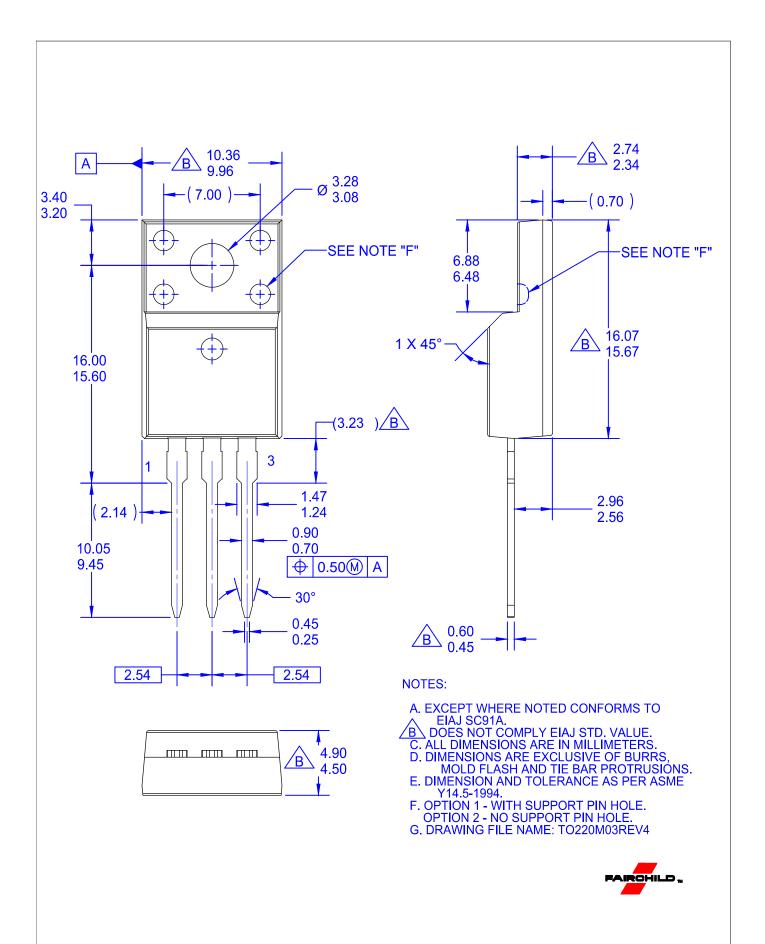
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ÁMEÓYÓÒÚVÁY PÒÜÒÁÞUVÒÖÁÔUÞØUÜT ÙÁVUÁ ÒORÂJÔJFŒ ÖŲÒVÁQUVÁÔUT, ÝŠIÝ,ÔOORÁÚV,ÖBÁ(ŒŠŅÒĖ, AKÔFÁCIŠŠÁÖCT ÒÞÙQUÞÙÁCIÐ ÒÁÐÁT (ŠŠÇT ÒVÒÜÙÈ Á UŠO POD PŮÁJE OÁ PÔÝ ÔŠÝ VÝ OŽ ÔÁ PÁ Ó WŮ Ü DÊ Á UŠO ÁZŠQE PÁJE OÁ OBO AÚ Ú Ú VÝ VŮ WÙ OD ÞÚ È AKÒ ĐÁ CỰ CHU ỦO PÁCH CÁ VU SỐ U CƠ ĐÔ CÁC LÁU ÔU ÁCH T CÁ MÁ ŸFIĚLËJJIÈ ÁKONĚÖÜCEY OÞŐÁKOSÖÁÞCET ÒKÁVUGG€Þ€HÜÒXF

ŒÚÚÜUXŒŠÙ	ÖŒ/Ò			
<sup>ŎŬŒ∕ ÞK</sup> ÓUÓUŸÁTŒŠÖU	€ RWÞ€Ì	FAIRCHILE	<b>)</b>	
<sup>ÔPÒÓSÒŌK</sup> ÙÖÆSÒÒ		SEMICONDUCTO	Rтм	
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ŒŰŰŰŰXÖŐK PUYŒŰÖÁŒŠŠÒÞ		ÚŒĈSĒŒŒŒÂÛĈJFĒŠÕÆUÜT		
ÚŬURÔÔVQIÞ Ži T á		TSVË/UGG€Þ€H F		
Q-ÔP		ØUÜT ÒÜŠŸK ÞÆŒ	ÙPÒÒVÁK FÁUØÁF	







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Definition of Terms					
Datasheet Identification	Product Status	Definition			
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.			
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.			
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