ANALOG DEVICES

Dual Channel, 12-Bit, 65 MSPS A/D Converter with Analog Input Signal Conditioning

AD10265

FEATURES

- **Dual, 65 MSPS Minimum Sample Rate**
  - **Channel-Channel Matching, ±0.1% Gain Error**
  - **Channel-Channel Isolation, >80 dB**
  - **AC-Coupled Signal Conditioning Included**
- **Selectable Bipolar Input Voltage Range (±0.5 V, ±1.0 V, ±2.0 V)**
- **Gain Flatness up to Nyquist: < 0.5 dB**
- **80 dB Spurious-Free Dynamic Range**
- **Two's Complement Output Format**
- **3.3 V or 5 V CMOS-Compatible Output Levels**
- **1.05 W Per Channel**
- **Industrial and Military Grade**

APPLICATIONS

- **Phased Array Receivers**
- **Communications Receivers**
- **FLIR Processing**
- **Secure Communications**
- **GPS Anti-Jamming Receivers**
- **Multichannel, Multimode Receivers**

PRODUCT DESCRIPTION

The AD10265 is a full channel ADC solution with on-module signal conditioning for improved dynamic performance and fully matched channel-to-channel performance. The module includes two wide dynamic range AD6640 ADCs. Each AD6640 has an AD9631/AD9632 ac-coupled amplifier front end. The AD6640s have on-chip track-and-hold circuitry, and utilize an innovative multipass architecture, to achieve 12-bit, 65 MSPS performance. The AD10265 uses innovative high-density circuit design and laser-trimmed thin-film resistor networks to achieve exceptional matching and performance while still maintaining excellent isolation, and providing for significant board area savings.

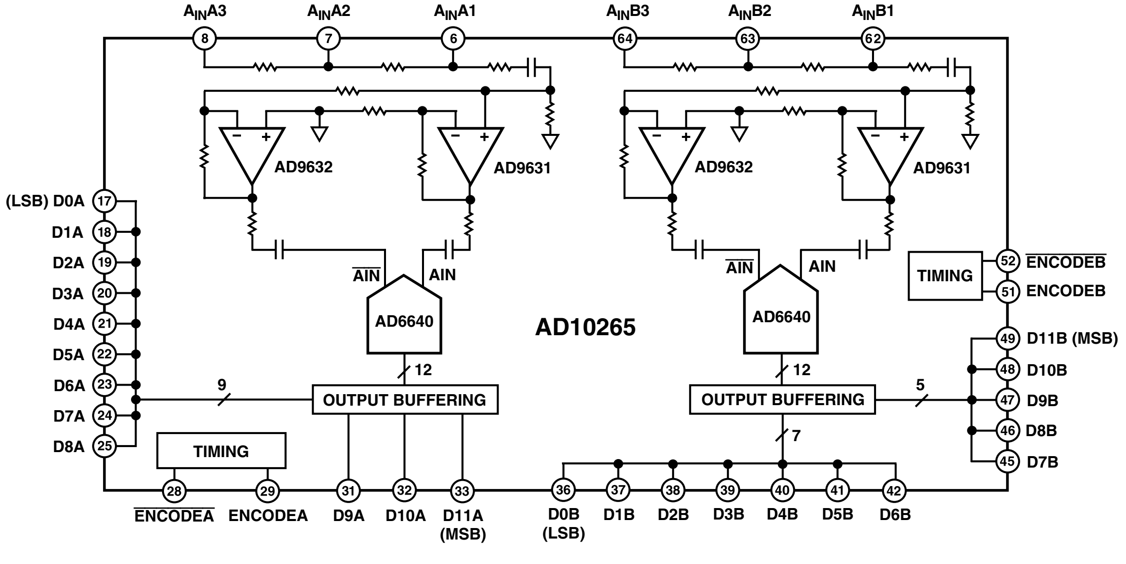
The AD10265 operates with ±5.0 V for the analog signal conditioning with a separate +3.3 V supply for the analog-to-digital conversion. Each channel is completely independent allowing operation with independent Encode and Analog inputs. The AD10265 also offers the user a choice of Analog Input Signal ranges to further minimize additional external signal conditioning, while still remaining general-purpose.

The AD10265 is packaged in a 68-lead ceramic gull wing package, footprint compatible with the earlier generation AD10242 (12-bit, 40 MSPS). Manufacturing is done on Analog Devices' MIL-38534 Qualified Manufacturers Line (QML) and components are available up to Class-T (–25°C to +125°C). The AD6640 internal components are manufactured on Analog Devices' high-speed complementary bipolar process (XFCB).

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 65 MSPS.
2. Input amplitude options, user configurable.
3. Input signal conditioning included; both channels matched for gain.
4. Fully tested/characterized performance for full channel.
5. Footprint compatible family; 68-lead LCCC.

FUNCTIONAL BLOCK DIAGRAM



REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700
www.analog.com
Fax: 781/326-8703

AD10265–SPECIFICATIONS

Electrical Characteristics (AV$_{CC}$ = +5 V; AV$_{EE}$ = –5.0 V; DV$_{CC}$ = +3.3 V; applies to each ADC unless otherwise noted.)

Parameter	Temp	Test Level	Mil Subgroup	AD10265AZ Min	AD10265AZ Typ	AD10265AZ Max	Unit
RESOLUTION					12		Bits
ACCURACY							
No Missing Codes	Full	IV	12		Guaranteed		
Offset Error	Full	IV	2, 3	–10	+3.5	+10	mV
Gain Error[1]	25°C	I	1	–1.5	±0.5	+1.5	% FS
	Full	VI	2, 3	–2.5	±0.8	+2.5	% FS
Gain Error Channel Match	Full	V			±0.2		%
Pass Band Ripple to Nyquist	Full	IV	12		0.2	0.5	dB
ANALOG INPUT (A_{IN})							
Input Voltage Range							
A_{IN}1	Full	V			±0.5		V
A_{IN}2	Full	V			±1.0		V
A_{IN}3	Full	V			±2		V
Input Resistance							
A_{IN}1	Full	IV	12	99	100	101	Ω
A_{IN}2	Full	IV	12	198	200	202	Ω
A_{IN}3	Full	IV	12	396	400	404	Ω
Input Capacitance[2]	25°C	IV	12	0	4.0	7.0	pF
Analog Input Bandwidth High[3]	25°C	V			160		MHz
Analog Input Bandwidth Low[3]	25°C	V			50		kHz
ENCODE INPUT[4, 5]							
Logic Compatibility		IV			TTL/CMOS		
Logic "1" Voltage	Full	IV		2.0		5.0	V
Logic "0" Voltage	Full	IV		0		0.8	V
Logic "1" Current (V_{INH} = 5 V)	Full	IV		500	650	800	µA
Logic "0" Current (V_{INL} = 0 V)	Full	IV		–400	–320	–200	µA
Input Capacitance	25°C	IV	12		4.5	7.0	pF
SWITCHING PERFORMANCE							
Maximum Conversion Rate[6]	Full	VI	4, 5, 6	65			MSPS
Minimum Conversion Rate[6]	Full	IV	12			6.5	MSPS
Aperture Delay (t_A)	25°C	V			400		ps
Aperture Delay Matching	25°C	V			±2.0		ns
Aperture Uncertainty (Jitter)	25°C	V			0.3		ps rms
ENCODE Pulsewidth High	25°C	IV	12	6.5			ns
ENCODE Pulsewidth Low	25°C	IV	12	6.5			ns
Output Delay (t_{OD})	Full	IV	12	7.0	9.0	12.5	ns
SNR[7]							
Analog Input @ 1.24 MHz	25°C	I	4	62	66		dB
	Full	II	5, 6	60.5	66		dB
@ 17 MHz	25°C	I	4	61	65		dB
	Full	II	5, 6	60	65		dB
@ 32 MHz	25°C	I	4	61	63		dB
	Full	II	5, 6	59.5	62		dB
SINAD[8]							
Analog Input @ 1.24 MHz	25°C	I	4	61	65		dB
	Full	II	5, 6	60	64		dB
@ 17 MHz	25°C	I	4	61	64		dB
	Full	II	5, 6	59.5	63		dB
@ 32 MHz	25°C	I	4	61	62		dB
	Full	II	5, 6	59	62		dB

Parameter	Temp	Test Level	Mil Subgroup	AD10265AZ			Unit
				Min	Typ	Max	
SPURIOUS-FREE DYNAMIC RANGE[9]							
Analog Input @ 1.24 MHz	25°C	I	4	75	80		dBFS
	Full	II	5, 6	74	80		dBFS
@ 17 MHz	25°C	I	4	71	80		dBFS
	Full	II	5, 6	70	79		dBFS
@ 32 MHz	25°C	V			79		dBFS
	Full	V			79		dBFS
TWO-TONE IMD REJECTION[10]							
f1, f2 @ –7 dBFS	Full	V	4, 5, 6	66	77		dBc
CHANNEL-TO-CHANNEL ISOLATION[11]	25°C	IV	12	80			dB
LINEARITY							
Differential Nonlinearity (Encode = 20 MHz)	25°C	IV	12	–1.0	±0.5	+1.5	LSB
Integral Nonlinearity (Encode = 20 MHz)	Full	V			±1.25		LSB
DIGITAL OUTPUTS							
Logic Compatibility					CMOS		
Logic "1" Voltage	Full	I	1, 2, 3	2.8	DV_{CC} – 0.2		V
Logic "0" Voltage	Full	I	1, 2, 3		0.2	0.5	V
Output Coding					Two's Complement		
POWER SUPPLY							
AV_{CC} Supply Voltage	Full	V			+5.0		V
I (AV_{CC}) Current	Full	V			336		mA
AV_{EE} Supply Voltage	Full	V			–5.0		V
I (AV_{EE}) Current	Full	V			66		mA
DV_{CC} Supply Voltage	Full	V			+3.3		V
I (DV_{CC}) Current	Full	V			20		mA
I_{CC} (Total) Supply Current	Full	I	1, 2, 3		422	520	mA
Power Dissipation (Total)	Full	I	1, 2, 3		2.1	2.4	W
Power Supply Rejection Ratio (PSRR)	Full	IV	12		0.01	0.02	% FSR/% V_S

NOTES

[1] Gain tests are performed on $A_{IN}1$ over specified input voltage range.

[2] Input capacitance specifications show only ceramic package capacitance.

[3] Full power bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

[4] ENCODE driven by single-ended source; $\overline{\text{ENCODE}}$ bypassed to ground through 0.01 μF capacitor.

[5] ENCODE may also be driven differentially in conjunction with $\overline{\text{ENCODE}}$; see "Encoding the AD10265" for details.

[6] Minimum and maximum conversion rates allow for variation in Encode Duty Cycle of 50% ± 5%.

[7] Analog Input signal power at –1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first 5 harmonics removed). Encode = 65 MSPS.

[8] Analog Input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 65 MSPS.

[9] Analog Input signal equal –1 dBFS; SFDR is ratio of converter full scale to worst spur.

[10] Both input tones at –7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product. f1 = 17.0 MHz ± 100 kHz, f2 = 18.0 MHz ± 100 kHz.

[11] Channel-to-channel isolation tested with A channel/50 ohm terminated <$A_{IN}2$ grounded, and a full-scale signal applied to B channel ($A_{IN}1$).

All specifications guaranteed within 100 ms of initial power-up, regardless of sequencing.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Unit
ELECTRICAL			
V_{CC} Voltage	0	+7	V
V_{EE} Voltage	–7	0	V
Analog Input Voltage	V_{EE}	V_{CC}	V
Analog Input Current	–10	+10	mA
Digital Input Voltage (ENCODE)	0	AV_{CC}	V
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage		4	V
Digital Output Current	–10	+10	mA
ENVIRONMENTAL[2]			
Operating Temperature (Case)	–55	+125	°C
Maximum Junction Temperature		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Typical thermal impedances for "Z" package: θ_{JC} = 11°C/W; θ_{JA} = 30°C/W.

Table I. Output Coding

MSB LSB	Base 10	Input
0111111111111	2047	+FS
0000000000001	+1	
0000000000000	0	0.0 V
1111111111111	–1	
1000000000000	2048	–FS

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C; sample tested at temperature extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD10265AZ	–25°C to +85°C (Case)	68-Lead Ceramic Leaded Chip Carrier	ES-68C
AD10265/PCB	+25°C	Evaluation Board with AD10265AZ	
5962-9865901 HXA	–25°C to +125°C (Case)	68-Lead Ceramic Leaded Chip Carrier	ES-68C
5962R0151901 TXA	–25°C to +125°C (Case)	68-Lead Ceramic Leaded Chip Carrier	ES-68C

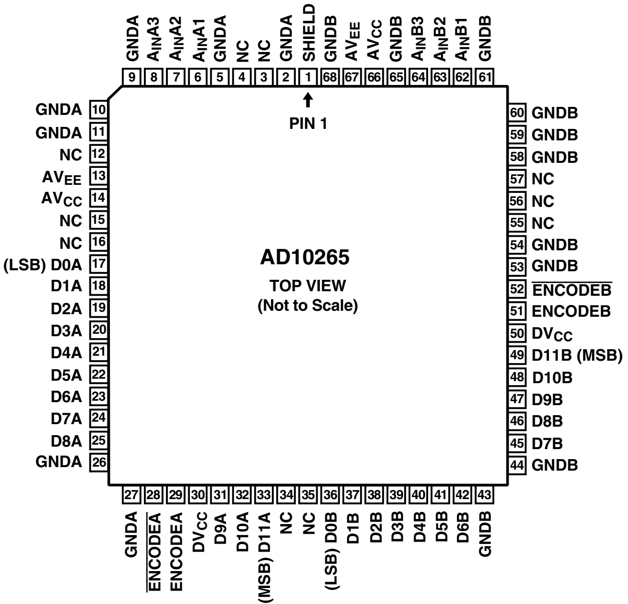
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD10265 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	SHIELD	Internal Ground Shield between channels.
2, 5, 9–11, 26, 27	GNDA	A Channel Ground. A and B grounds should be connected as close to the device as possible.
3, 4, 12, 15, 16, 34, 35, 55–57	NC	No Connect. Pins 15 and 16 are internal test pins: it is recommended to connect them to GND.
6	A_{IN}A1	Analog Input for A side ADC (nominally ±0.5 V).
7	A_{IN}A2	Analog Input for A side ADC (nominally ±1.0 V).
8	A_{IN}A3	Analog Input for A side ADC (nominally ±2.0 V).
13	AV_{EE}	Analog Negative Supply Voltage (nominally –5.0 V). For A side ADC.
14	AV_{CC}	Analog Positive Supply Voltage (nominally +5.0 V). For A side ADC.
17–25, 31–33	D0A–D11A	Digital Outputs for ADC A. D0 (LSB).
28	$\overline{\text{ENCODEA}}$	$\overline{\text{ENCODE}}$ is complement of ENCODE.
29	ENCODEA	Data conversion initiated on rising edge of ENCODE input.
30	DV_{CC}	Digital positive supply voltage (nominally 3.3 V) for A side ADC.
36–42, 45–49	D0B–D11B	Digital Outputs for ADC B. D0 (LSB).
43, 44, 53, 54, 58–61, 65, 68	GNDB	B Channel Ground. A and B grounds should be connected as close to the device as possible.
50	DV_{CC}	Digital Positive Supply Voltage (nominally 3.3 V) for B side ADC.
51	ENCODEB	Data conversion initiated on rising edge of $\overline{\text{ENCODE}}$ input.
52	$\overline{\text{ENCODEB}}$	$\overline{\text{ENCODE}}$ is complement of ENCODE.
62	A_{IN}B1	Analog Input for B side ADC (nominally ±0.5 V).
63	A_{IN}B2	Analog Input for B side ADC (nominally ±1.0 V).
64	A_{IN}B3	Analog Input for B side ADC (nominally ±2.0 V).
66	AV_{CC}	Analog Positive Supply Voltage (nominally +5.0 V). For B side ADC.
67	AV_{EE}	Analog Negative Supply Voltage (nominally –5.0 V). For B side ADC.

PIN CONFIGURATION
68-Lead Ceramic Leaded Chip Carrier



NC = NO CONNECT

DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in logic “1” state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of ENCODE command and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

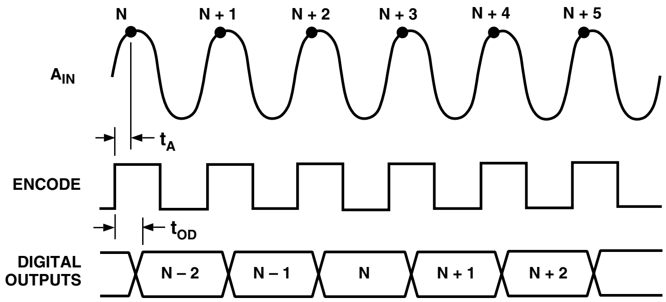


Figure 1. Timing Diagram

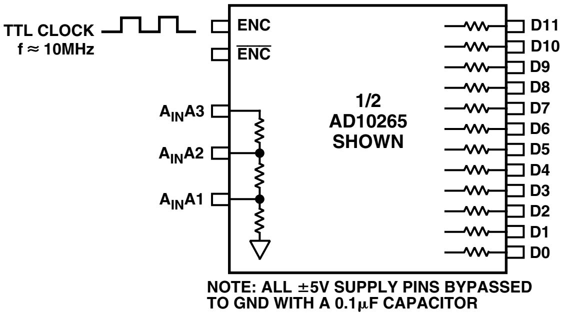


Figure 2. Equivalent Burn-In Circuit

EQUIVALENT CIRCUITS

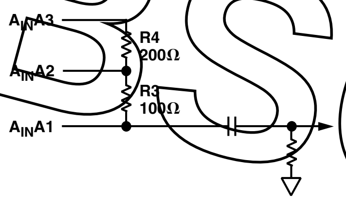


Figure 3. Analog Input Stage

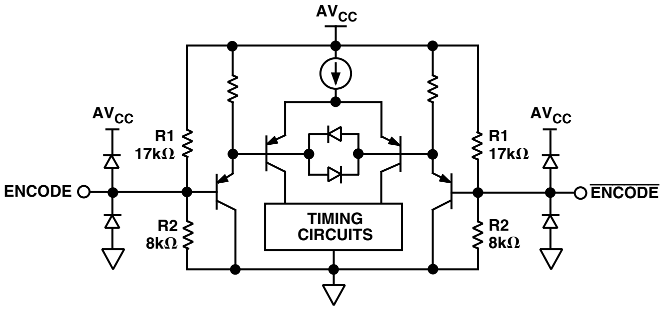


Figure 4. Encode Inputs

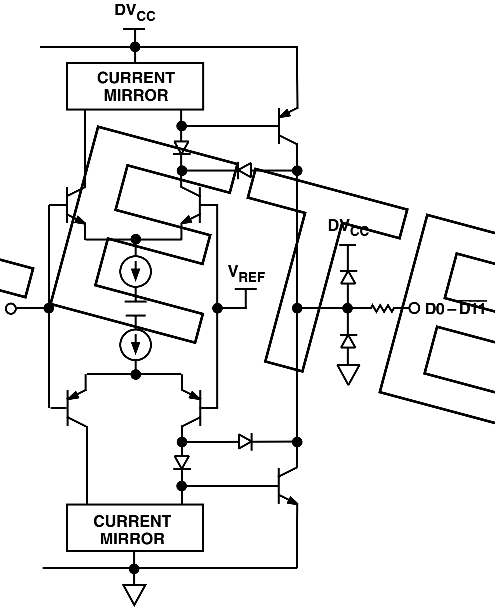
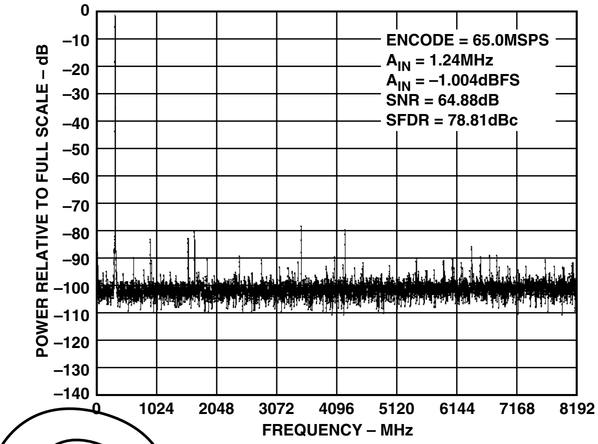
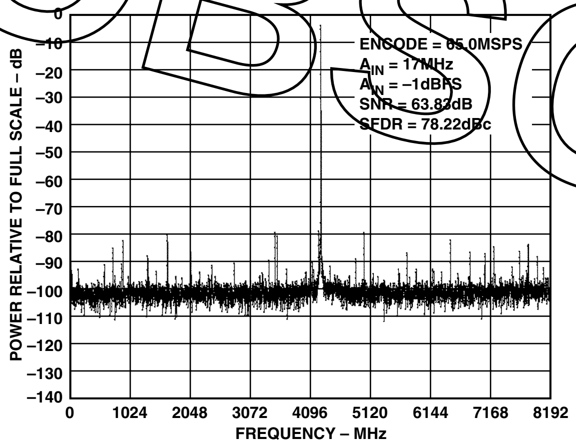


Figure 5. Digital Output Stage

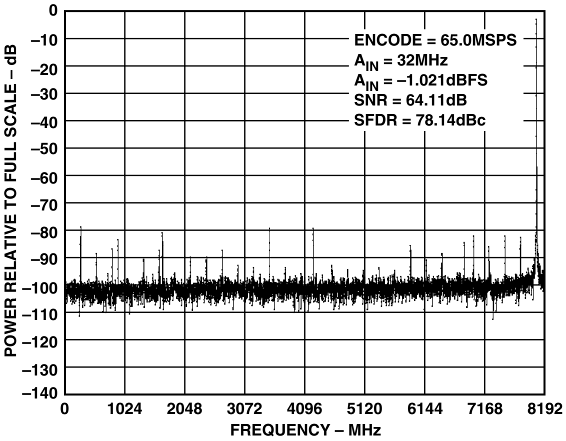
AD10265–Typical Performance Characteristics



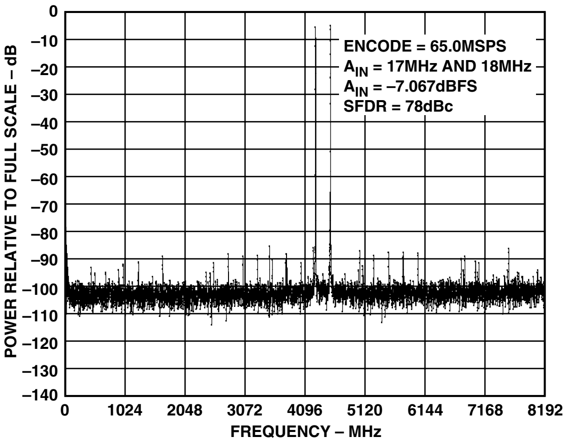
TPC 1. Single Tone @ 1.24 MHz



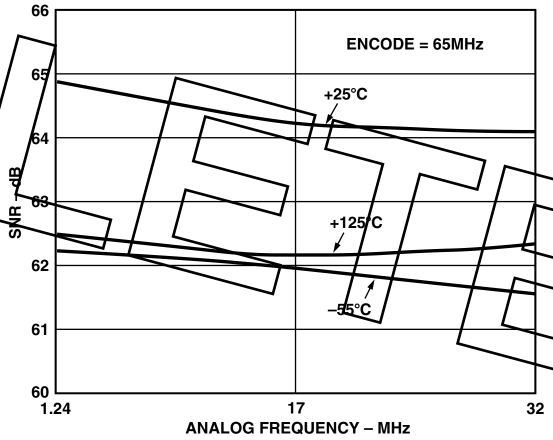
TPC 2. Single Tone @ 17 MHz



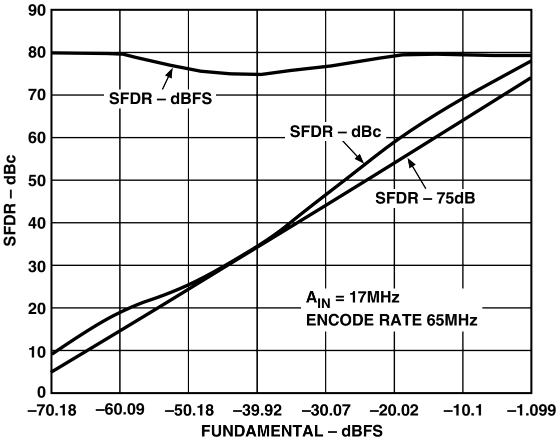
TPC 3. Single Tone @ 32 MHz



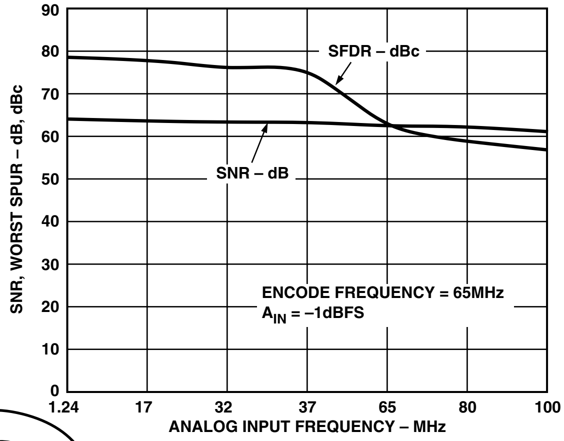
TPC 4. Two-Tone FFT @ 17 MHz/18 MHz



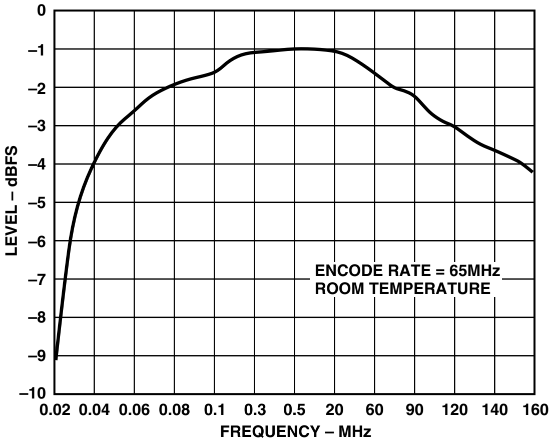
TPC 5. SNR vs. A_{IN}



TPC 6. Single-Tone SFDR (A_{IN} @ 17 MHz) vs. Power Level



TPC 7. SNR/Harmonics to A_{IN} > Nyquist MSPS



TPC 8. Gain Flatness vs. Input Frequency

THEORY OF OPERATION

Refer to the Functional Block Diagram. The AD10265 employs three monolithic ADI components per channel (AD9631, AD9632, and AD6640), along with multiple passive resistor networks and decoupling capacitors to fully integrate a complete 12-bit analog-to-digital converter.

The input signal is first passed through a precision laser-trimmed resistor divider, allowing the user to externally select operation with a full-scale signal of ±0.5 V, ±1.0 V, or ±2.0 V by choosing the proper input terminal for the application.

Since the AD6640 implements a true differential analog input, the AD9631/AD9632 have been configured to provide a differential input for the AD6640 ADC through ac-coupling. The ac signal gain of the AD9631/AD9632 can be trimmed to provide a constant differential input to the AD6640. This allows the converter to be used in multiple system applications without the need for external gain circuit normally requiring trim. The AD9631/AD9632 were chosen for their superior ac performance and input drive capabilities, which have limited the ability of many amplifiers to drive high-performance ADCs. As new amplifiers are developed, pin-compatible improvements are planned to incorporate the latest operational amplifier technology.

APPLYING THE AD10265

Encoding the AD10265

Best performance is obtained by driving the encode pins differentially. However, the AD10265 is also designed to interface with TTL and CMOS logic families. The source used to drive the ENCODE pin(s) must be clean and free from jitter. Sources with excessive jitter will limit SNR and overall performance.

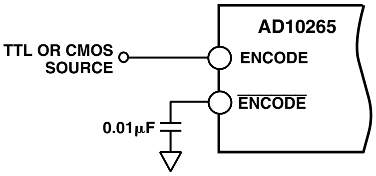


Figure 6. Single-Ended TTL/CMOS Encode

The AD10265 encode inputs are connected to a differential input stage (see Figure 4 under Equivalent Circuits). With no input connected to either ENCODE pin, the voltage divider biases the inputs to 1.6 V. For TTL or CMOS usage, the encode source should be connected to ENCODE. $\overline{\text{ENCODE}}$ should be decoupled using a low inductance or microwave chip capacitor to ground.

If a logic threshold other than the nominal 1.6 V is required, the following equations show how to use an external resistor, Rx, to raise or lower the trip point (see Figure 4, R1 = 17 kΩ, R2 = 8 kΩ).

$$V_1 = \frac{5R2Rx}{R1R2 + R1Rx + R2Rx} \text{ to lower logic threshold.}$$

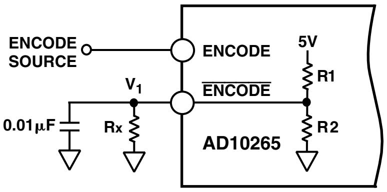


Figure 7. Lower Threshold for Encode

$$V_1 = \frac{5R2}{R2 + \dfrac{R1Rx}{R1 + Rx}} \text{ to raise logic threshold.}$$

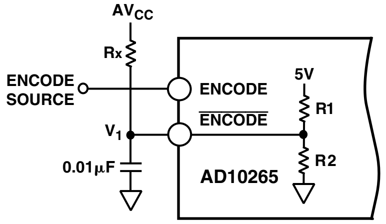


Figure 8. Raise Logic Threshold for Encode

While the single-ended encode will work well for many applications, driving the encode differentially will provide increased performance. Depending on circuit layout and system noise, a 1 dB to 3 dB improvement in SNR can be realized. It is recommended that differential TTL logic be used, however, because most TTL families that support complementary outputs are not delay or slew rate matched. Instead, it is recommended that the encode signal be ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins.

The simplest option is shown below. The low jitter TTL signal is coupled with a limiting resistor, typically 100 Ω, to the primary side of an RF transformer (these transformers are inexpensive and readily available; part number in Figure 9 is from Mini-Circuits). The secondary side is connected to the ENCODE and $\overline{\text{ENCODE}}$ pins of the converter. Since both encode inputs are self-biased, no additional components are required.

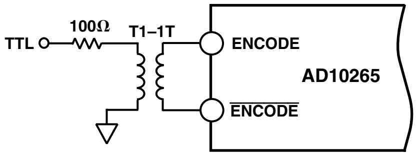


Figure 9. TTL Source—Differential Encode

A clean sine wave may be substituted for a TTL clock. In this case, the matching network is shown below. Select a transformer ratio to match source and load impedances. The input impedance of the AD10265 encode is approximately 11 kΩ differentially. Therefore "R," shown in Figure 10, may be any value that is convenient for available drive power.

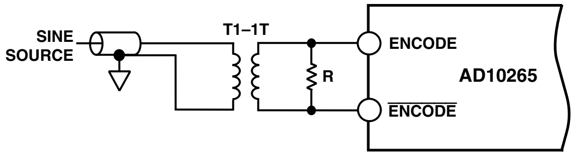


Figure 10. Sine Source—Differential Encode

If a low jitter ECL clock is available, another option is to ac-couple a differential ECL signal to the encode input pins as shown below. The capacitors shown here should be chip capacitors, but do not need to be of the low inductance variety.

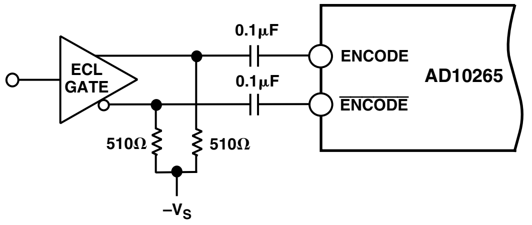


Figure 11. Differential ECL for Encode

As a final alternative, the ECL gate may be replaced by an ECL comparator. The input to the comparator could then be a logic signal or a sine signal.

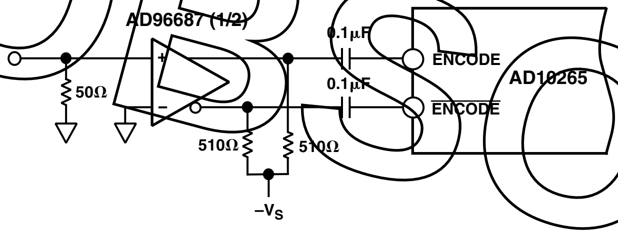


Figure 12. ECL Comparator for Encode

USING THE FLEXIBLE INPUT

The AD10265 has been designed with the user's ease of operation in mind. Multiple input configurations have been included on board to allow the user a choice of input signal levels and input impedance. While the standard inputs are ±0.5 V, ±1.0 V, and ±2.0 V, the user can select the input impedance of the AD10265 on any input by using the other inputs as alternate locations for GND or an external resistor. The following chart summarizes the impedance options available at each input location:

$A_{IN}1$ = 100 Ω when $A_{IN}2$ and $A_{IN}3$ Are Open.
$A_{IN}1$ = 75 Ω when $A_{IN}3$ Is Shorted to GND.
$A_{IN}1$ = 50 Ω when $A_{IN}2$ Is Shorted to GND.

$A_{IN}2$ = 200 Ω when $A_{IN}3$ Is Open.
$A_{IN}2$ = 100 Ω when $A_{IN}3$ Is Shorted to GND.
$A_{IN}2$ = 75 Ω when $A_{IN}2$ to $A_{IN}3$ Has an External Resistor of 300 Ω, with A_{IN} 3 Shorted to GND.
$A_{IN}2$ = 50 Ω when $A_{IN}2$ to $A_{IN}3$ Has an External Resistor of 100 Ω, with $A_{IN}3$ Shorted to GND.

$A_{IN}3$ = 400 Ω.
$A_{IN}3$ = 100 Ω when $A_{IN}3$ Has an External Resistor of 133 Ω to GND.
$A_{IN}3$ = 75 Ω when $A_{IN}3$ Has an External Resistor of 92 Ω to GND.
$A_{IN}3$ = 50 Ω when $A_{IN}3$ Has an External Resistor of 57 Ω to GND.

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

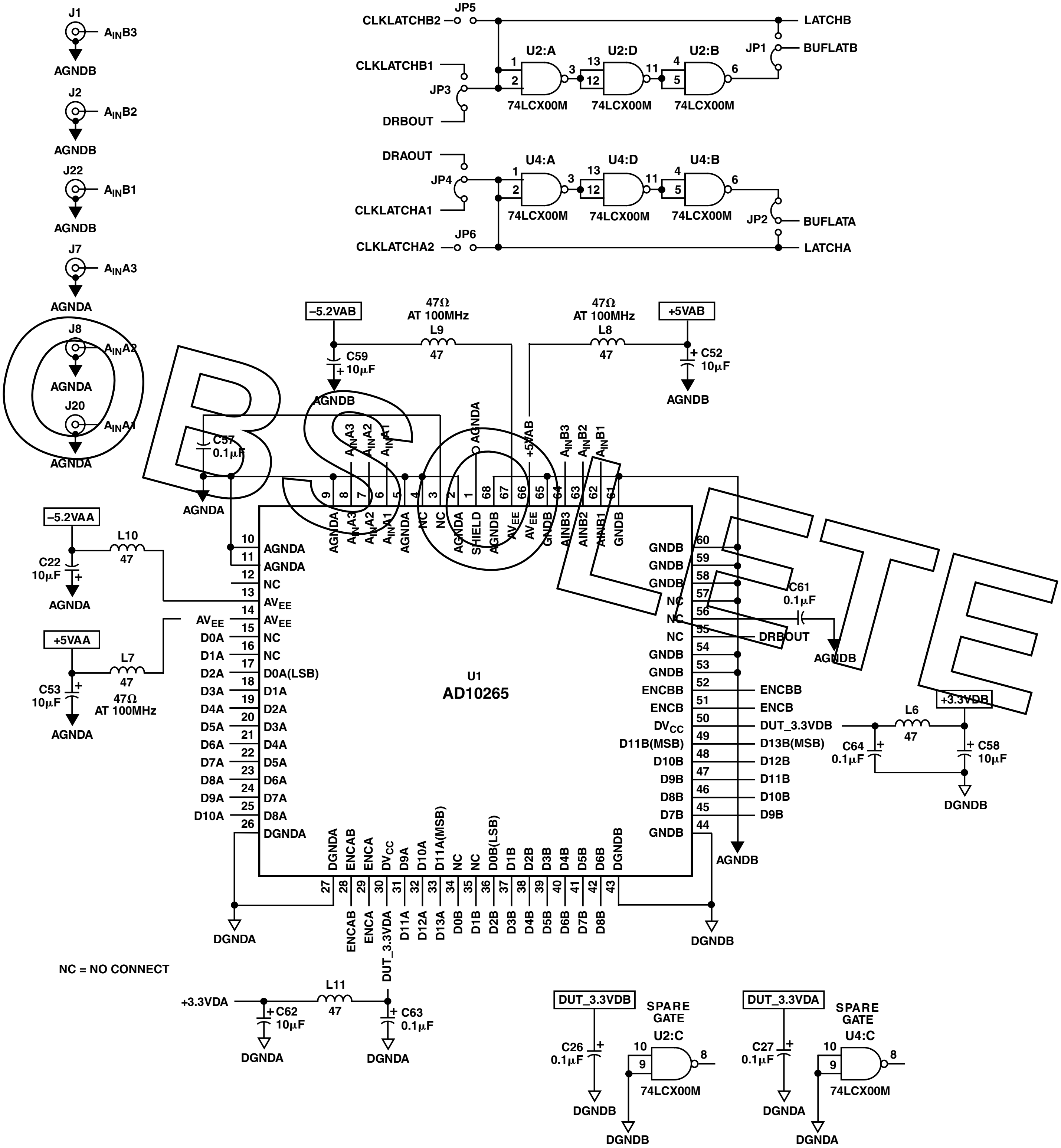
These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling to the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. The AD10265 does not distinguish between analog and digital ground pins as the AD10265 should always be treated as an analog component. All ground pins should be connected together directly under the AD10265. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path and manage the power and ground currents. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

LAYOUT INFORMATION

The schematic of the evaluation board (Figure 13) represents a typical implementation of the AD10265. The pinout of the AD10265 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the AD6640 ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.



NC = NO CONNECT

Figure 13a. Evaluation Board Schematic

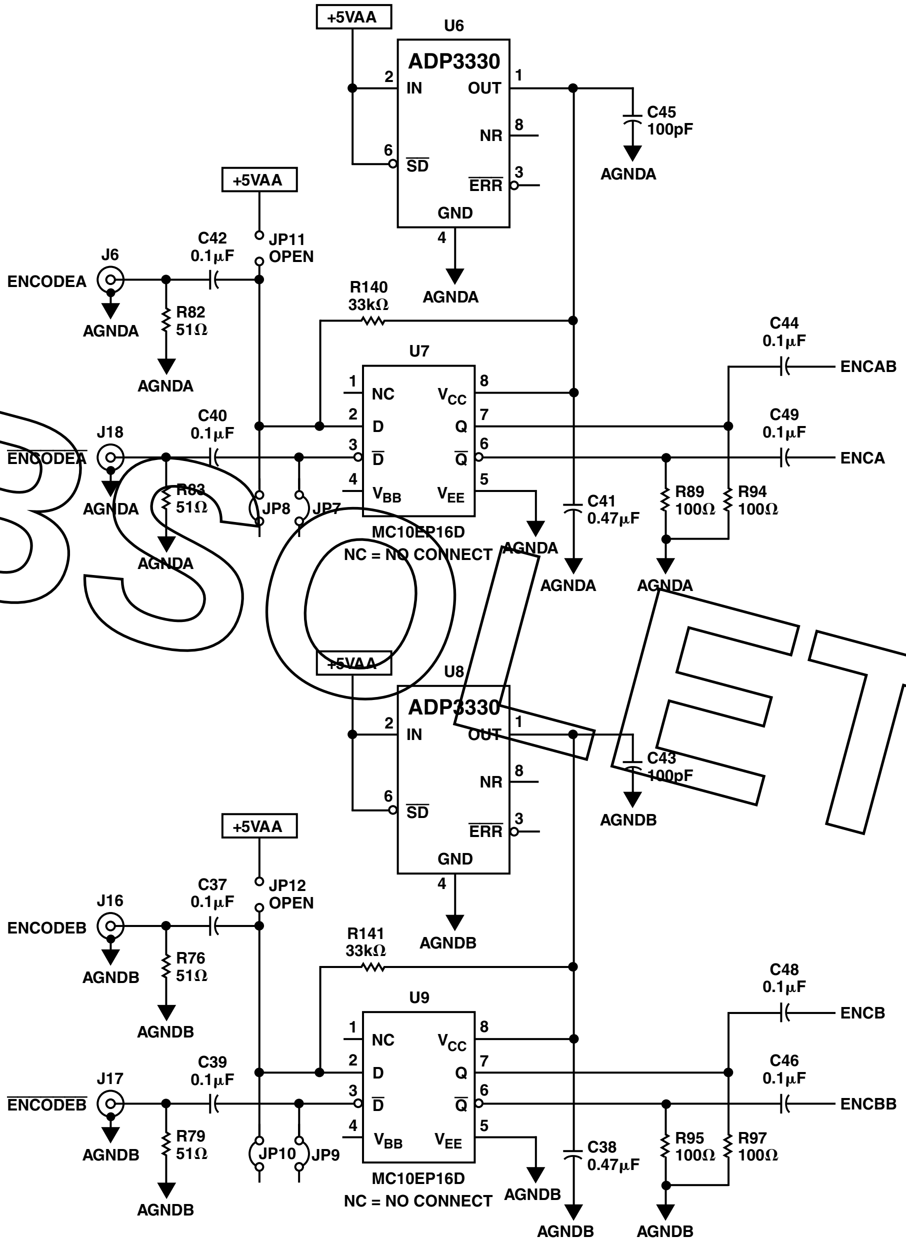


Figure 13b. Evaluation Board Schematic

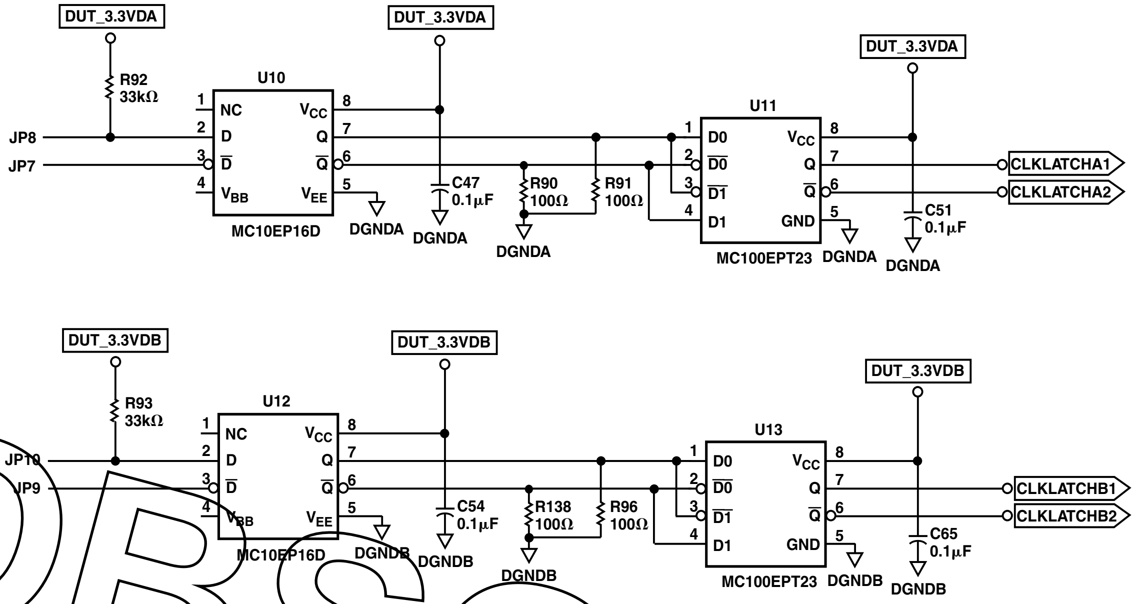


Figure 13c. Evaluation Board Schematic

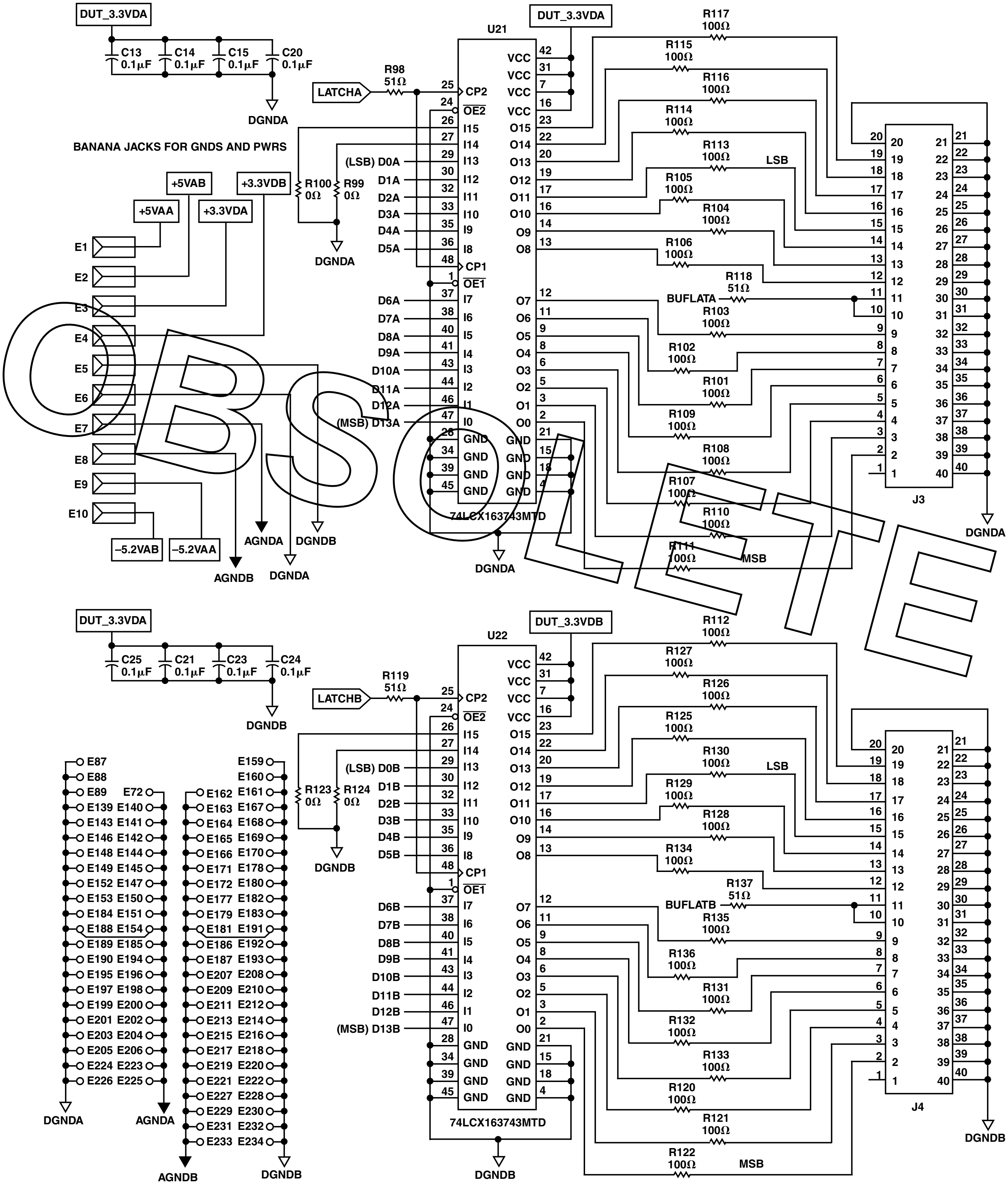


Figure 13d. Evaluation Board Schematic

EVALUATION BOARD

The AD10265 evaluation board (Figure 14) is designed to provide optimal performance for evaluation of the AD10265 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD10265.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the crystal oscillator, the associated components and amplifiers, and the analog section of the AD10265. The digital outputs of the AD10265 are powered via Pin 1 of either J1 or J2 found on the digital interface connector with 3.3 V. Contact the factory if additional layout or applications assistance is required.

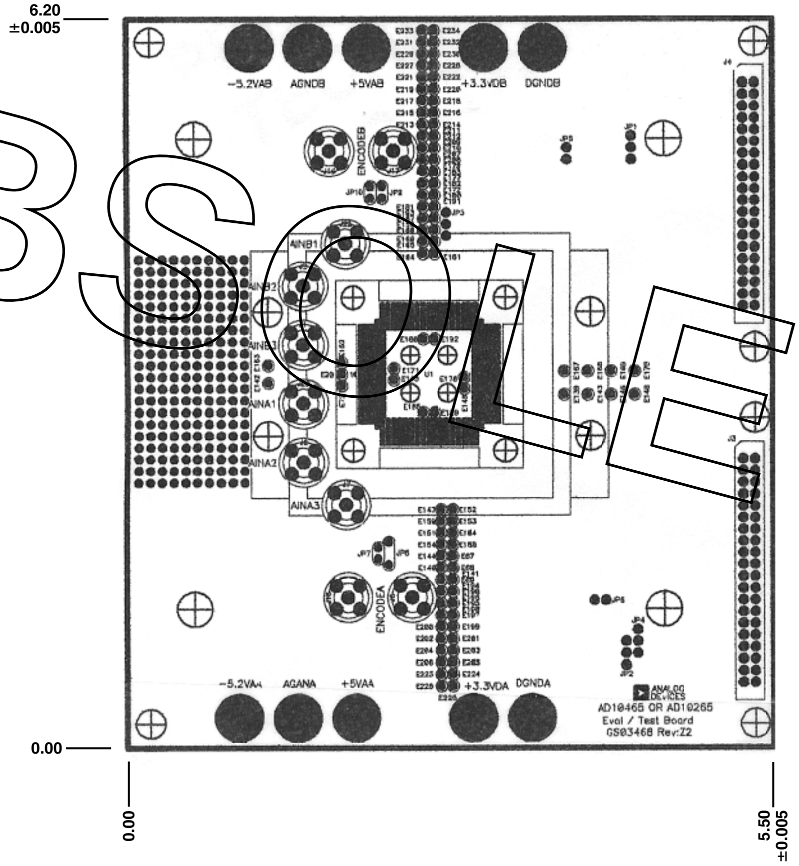


Figure 14. Evaluation Board Mechanical Layout

Bill of Materials List for AD10265 Evaluation Board

Qty	Reference Designator	Value	Description	Manufacturer and Part Number	Component Name
2	U2, U4		IC, Low-Voltage Quad 2-Input Nand, SOIC-14	Toshiba/TC74LCX00FN	74LCX00M
2	U21, U22		IC, 16-Bit Transparent Latch with Three-State Outputs, TSSOP-48	Fairchild/74LCX163743MTD	74LCX163743MTD
1	U1		DUT, IC 14-Bit Analog-to-Digital Converter	ADI/AD10265AZ	ADI/AD10465AZ
2	U6, U8		IC, Voltage Regulator 3.3 V, RT-6	Analog Devices/ADP3330ART-3, 3-RLT	ADP3330
10	E1–E10		Banana Jack, Socket	Johnson Components/08-0740-001	Banana Hole
30	C13–C15, C20, C21, C23–C27, C37, C39, C40, C41, C42, C44, C46, C47, C48, C49, C54–C58, C60, C61, C63, C64, C65	0.1 µF	Capacitor, 0.1 µF, 20%, 12 V dc, 0805	Mena/GRM40X7R104K025BL	CAP 0805
2	C38, C41	0.47 µF	Capacitor, 0.47 µF, 5%, 12 V dc, 1206	Vitramon/VJ1206U474MFXMB	CAP 1206
2	C43, C45	100 pF	Capacitor, 100 pF, 10%, 12 V dc, 0805	Johansen/500R15N101JV4	CAP 0805
2	J3, J4		Connector, 40-pin Header Male St.	Samtec/TSW-120-08-G-D	HD40M
6	L6–L11	47 µH	Inductor, 47 µH @ 100 MHz, 20%, IND2	Fair-Rite/2743019447	IND2
4	U7, U9, U10, U11		IC, Differential Receiver, SOIC-8	Motorola/MC10EP16D	MC10EP16D
6	C22, C50, C52, C53, C59, C62	10 µF	Capacitor, 10 µF, 20%, 16 V dc, 1812POL	Kemet/T491C106M016A57280	POLCAP 1812
4	R99, R100, R123, R124	0.0 Ω	Resistor, 0.0 Ω, 0805	Panasonic/ERJ-6GEY0R00V	RES2 0805
4	R92, R93, R140, R141	33,000 Ω	Resistor, 33,000 Ω, 5%, 0.10 Watt, 0805	Panasonic/ERJ-6GEYJ333V	RES2 0805
8	R76, R79, R82, R83, R98, R118, R119, R137	51 Ω	Resistor, 51 Ω, 5%, 0.10 Watt, 0805	Panasonic/ERJ-6GEYJ510V	RES2 0805, RES 0805
40	R89, R90, R91, R94, R95, R97, R101–R117, R120–R122, R125–R136, R138	100 Ω	Resistor, 100 Ω, 5%, 0.10 Watt, 0805	Panasonic/ERJ-6GEYJ101V	RES2 0805, RES 0805
8	J1, J2, J6–J8, J16–J18, J20, J22		Connector, SMA Female St.	Johnson Components/142-0701-201	SMA
2	U11, U13		IC Op Amp, SOIC-8	Motorola/MC100EPT23	MC100EPT23

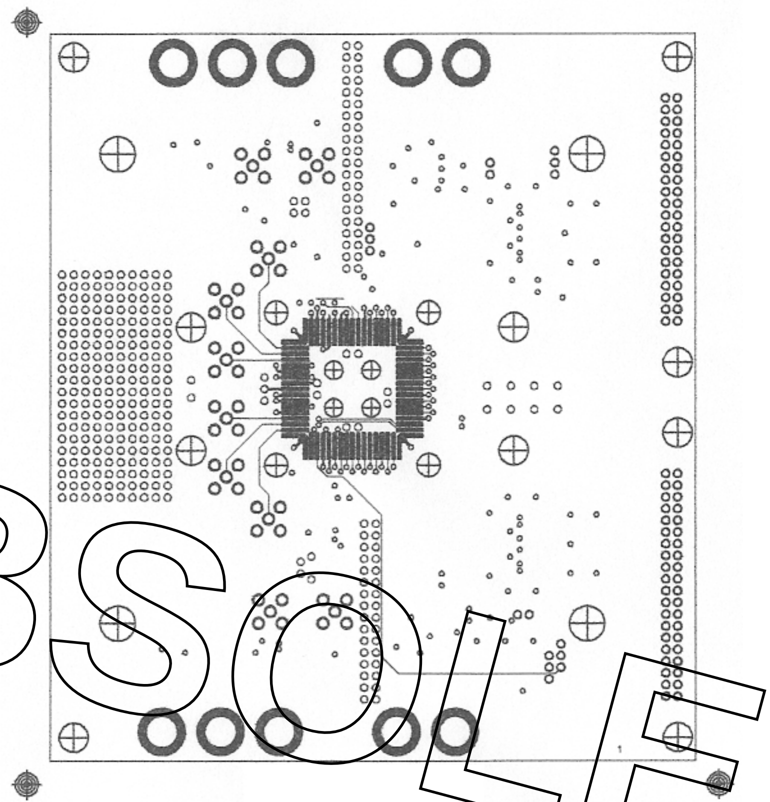


Figure 15. Top Layer Copper

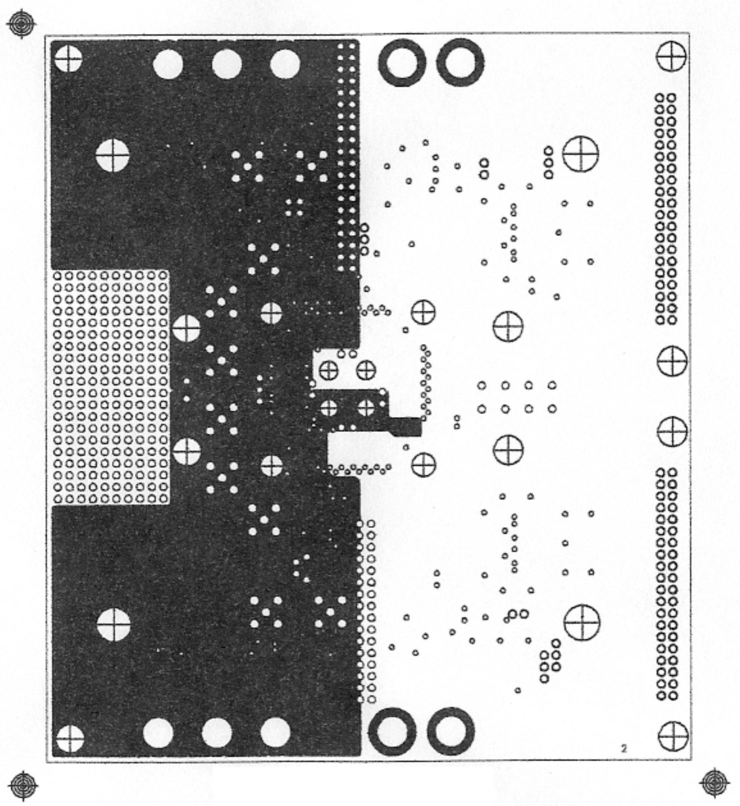


Figure 16. Second Layer Copper

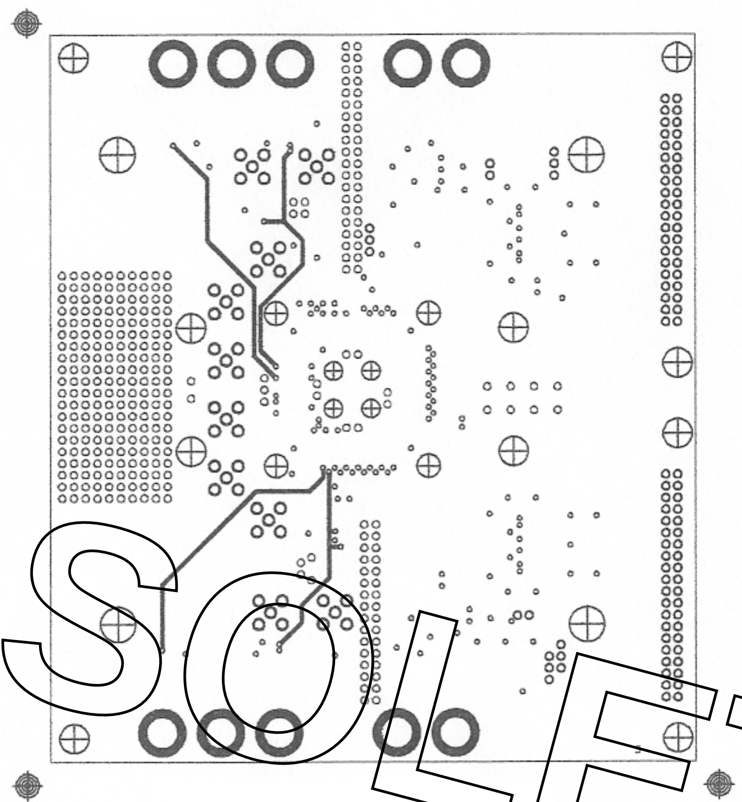


Figure 17. Third Layer Copper

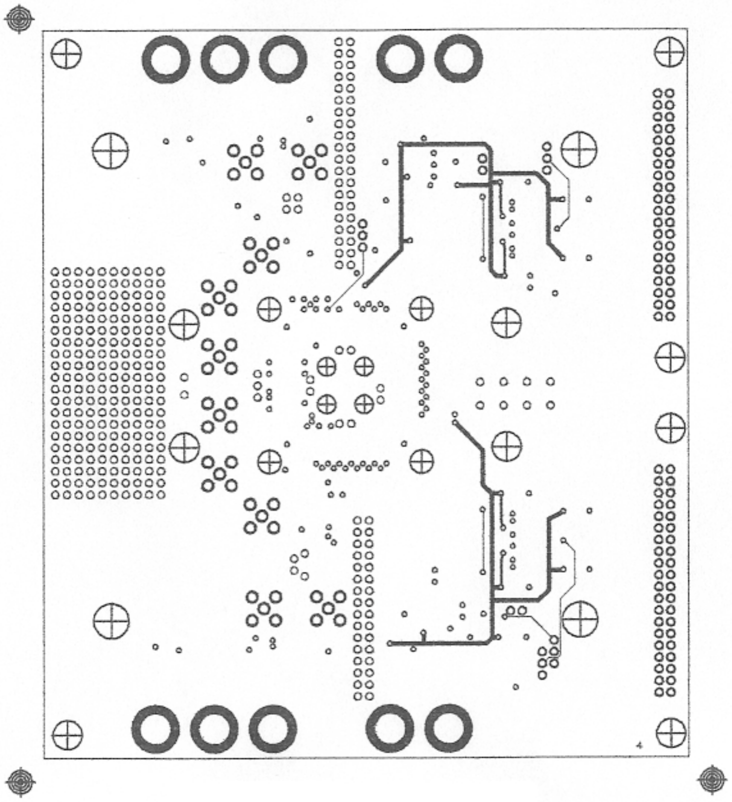


Figure 18. Fourth Layer Copper

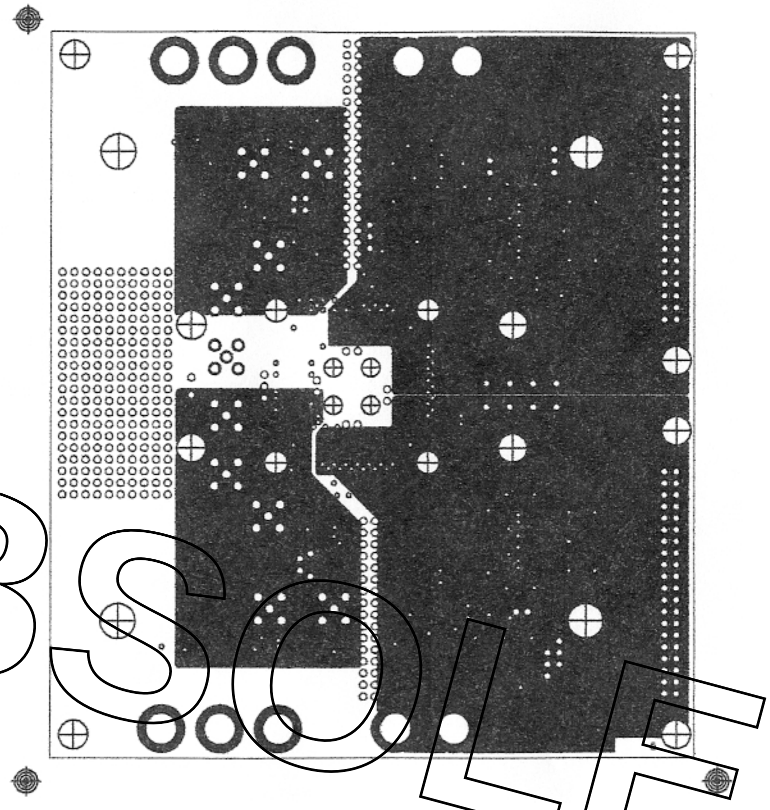


Figure 19. Fifth Layer Copper

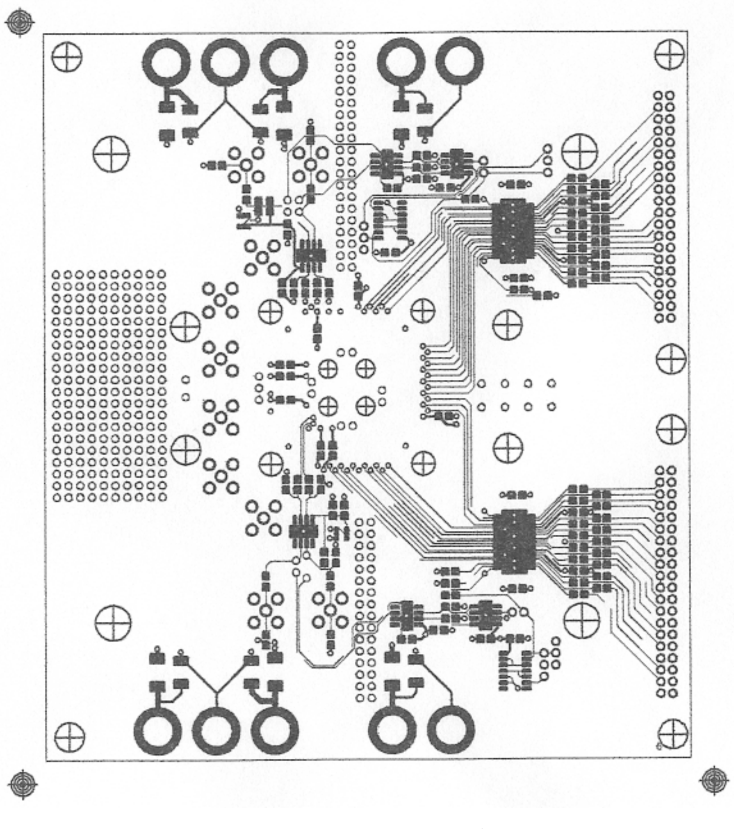


Figure 20. Bottom Layer Copper

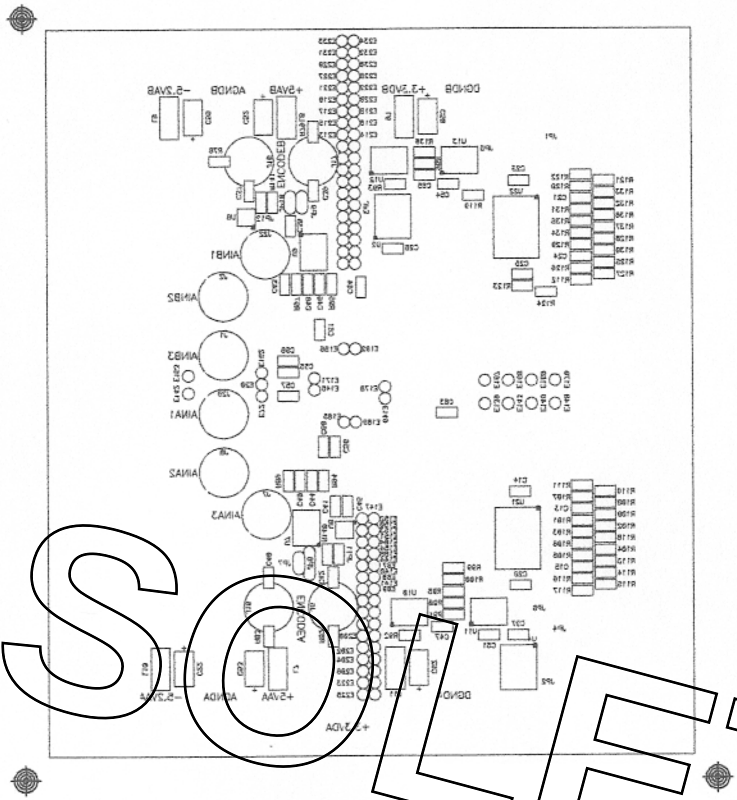


Figure 21. Bottom Silkscreen

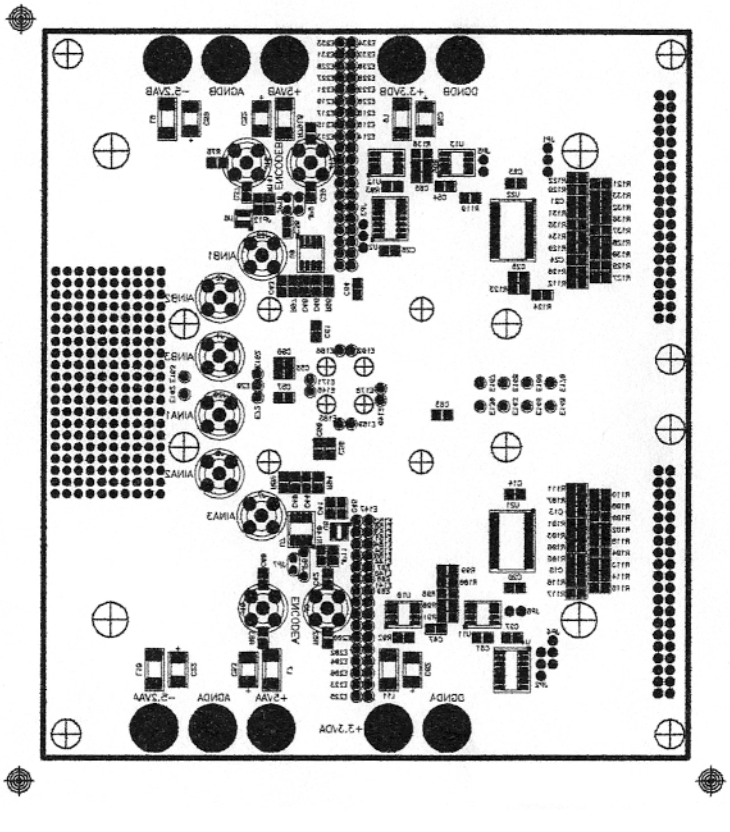
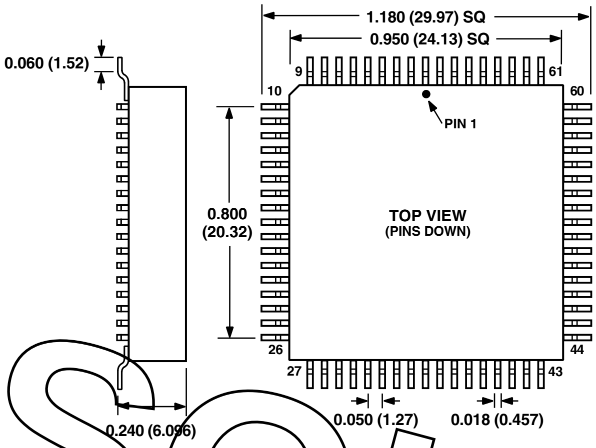


Figure 22. Bottom Assembly

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

68-Lead Ceramic Leaded Chip Carrier (ES-68C)



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