1.6 GBPS QUAD SERIAL BACKPLANE DEVICE S2009

FEATURES

- CMOS Technology
- Broad operating rate range (1.3 - 1.6 Gbps)
  - 1.6 Gbps
  - 1/2 Rate Operation
- Quad Transmitter with Phase-Lock Loop (PLL) clock synthesis from low speed reference
- Quad Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- On-chip 8B/10B line encoding and decoding for four separate parallel 8-bit channels
- 32-bit parallel TTL interface with internal series terminated outputs
- Low-jitter serial PECL interface
- Individual local loopback control
- JTAG 1149.1 Boundary scan on low speed I/O signals
- Interfaces with coax, twinax, or fiber optics
- Single +3.3 V supply, 2.65 W power dissipation
- Compact 23 mm x 23 mm 208 pin TBGA package

APPLICATIONS

- Ethernet Backbones
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2009 facilitates high-speed serial transmission of data in a variety of applications including Gigabit Ethernet, serial backplanes, and proprietary point to point links. The chip provides four separate transceivers which can be operated individually or locked together for an aggregate data capacity of >5 Gbps.

Each bi-directional channel provides 8B/10B coding/decoding, parallel-to-serial and serial-to-parallel conversion, clock generation/recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip quad receive PLL is used for clock recovery and data retiming on the four independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a +3.3 V power supply and dissipates 2.65 watts.

Figure 1 shows the S2009 and S2204 in a Gigabit Ethernet application. Figure 2 combines the S2009 with a crosspoint switch to demonstrate a serial backplane application. Figure 3 is the input/output diagram. Figures 4 and 5 show the transmit and receive block diagrams, respectively.

Figure 1. Typical Quad Gigabit Ethernet Application

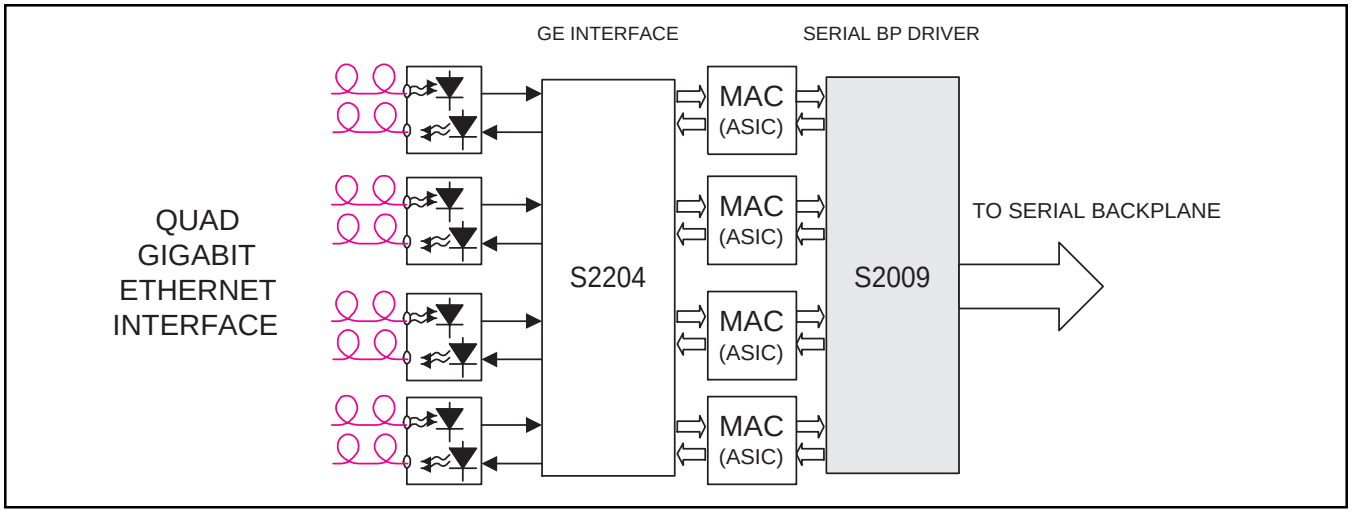


Figure 2. Typical Serial Backplane Application

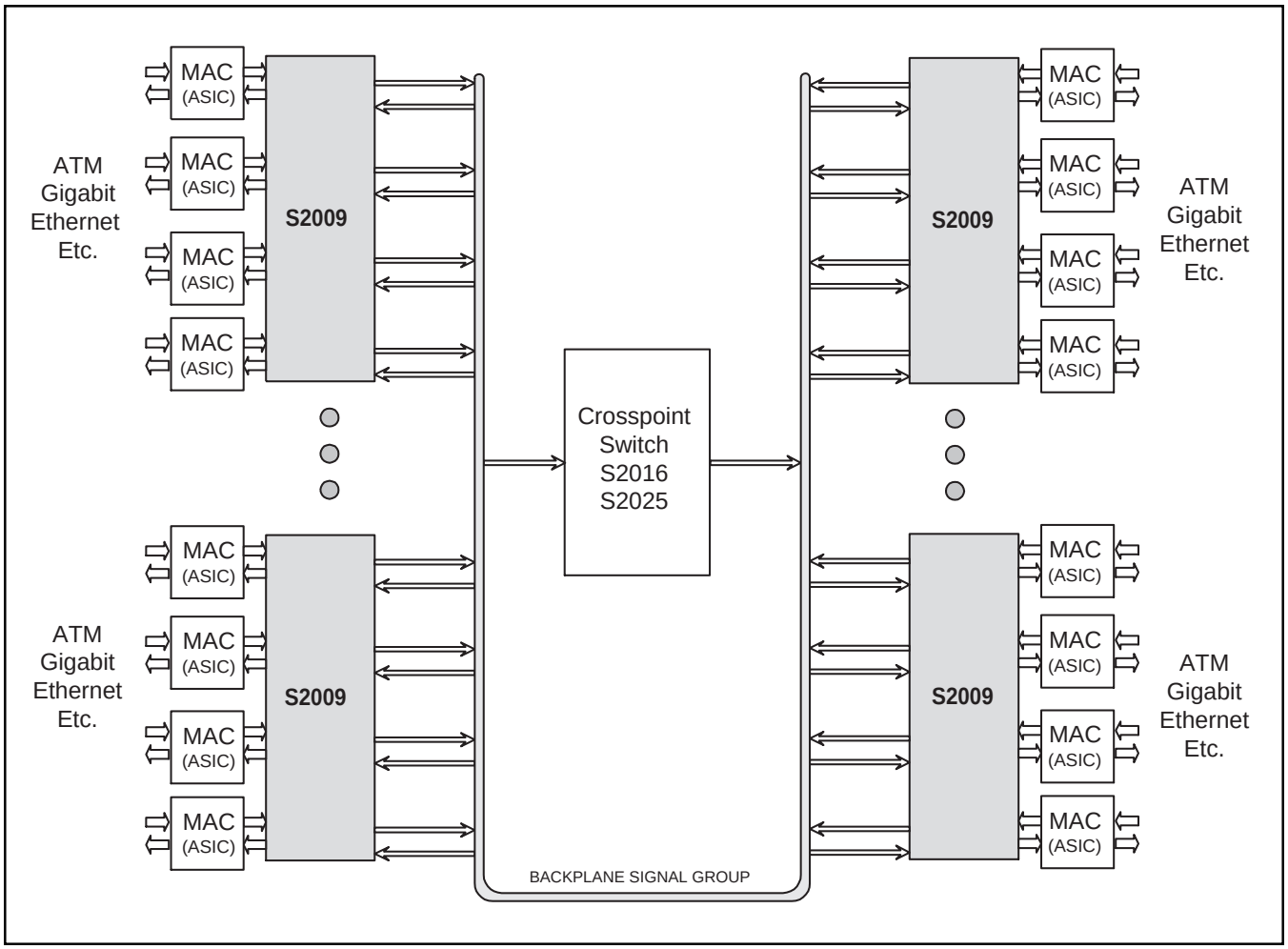


Figure 3. S2009 Input/Output Diagram

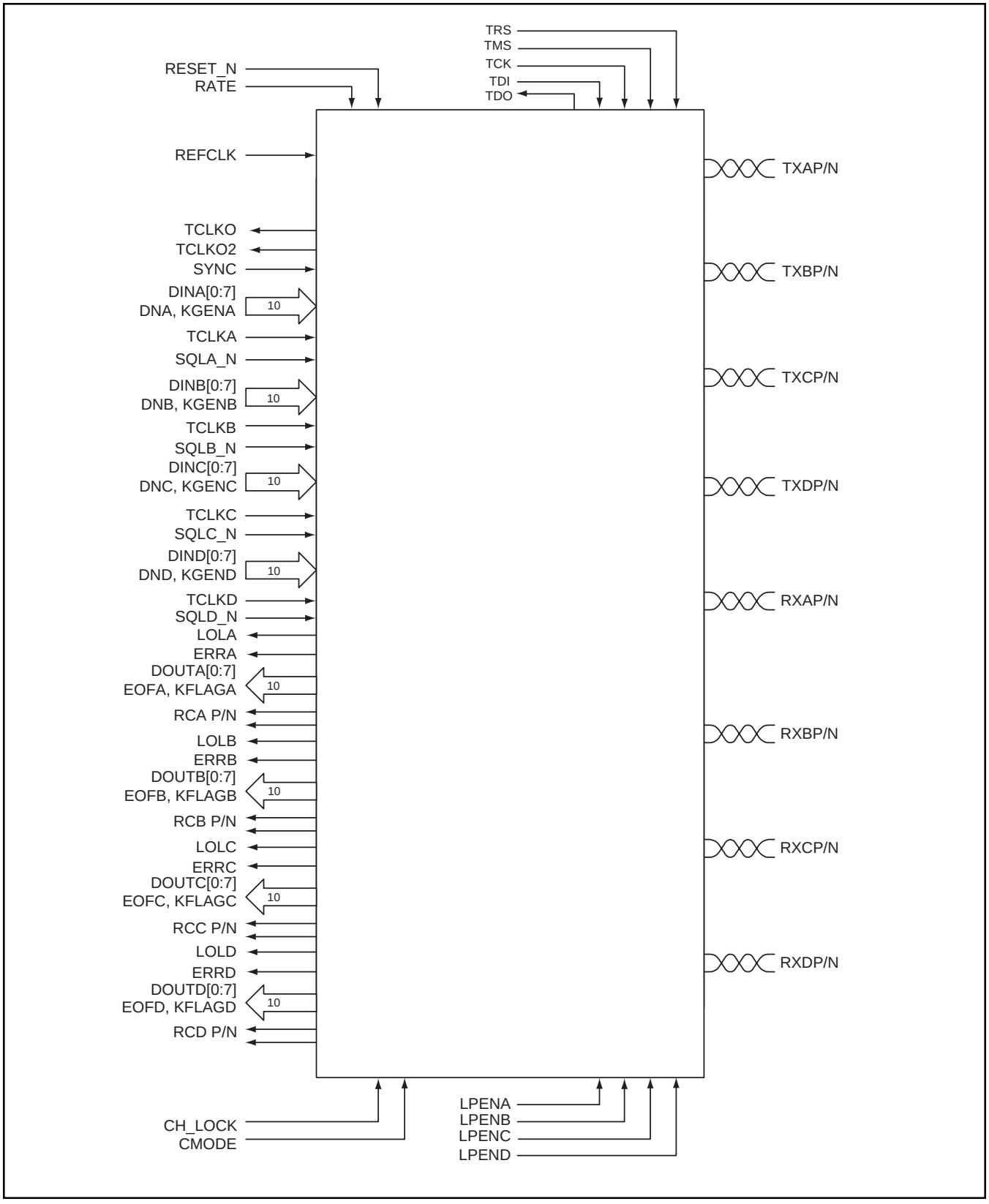


Figure 4. Transmitter Block Diagram

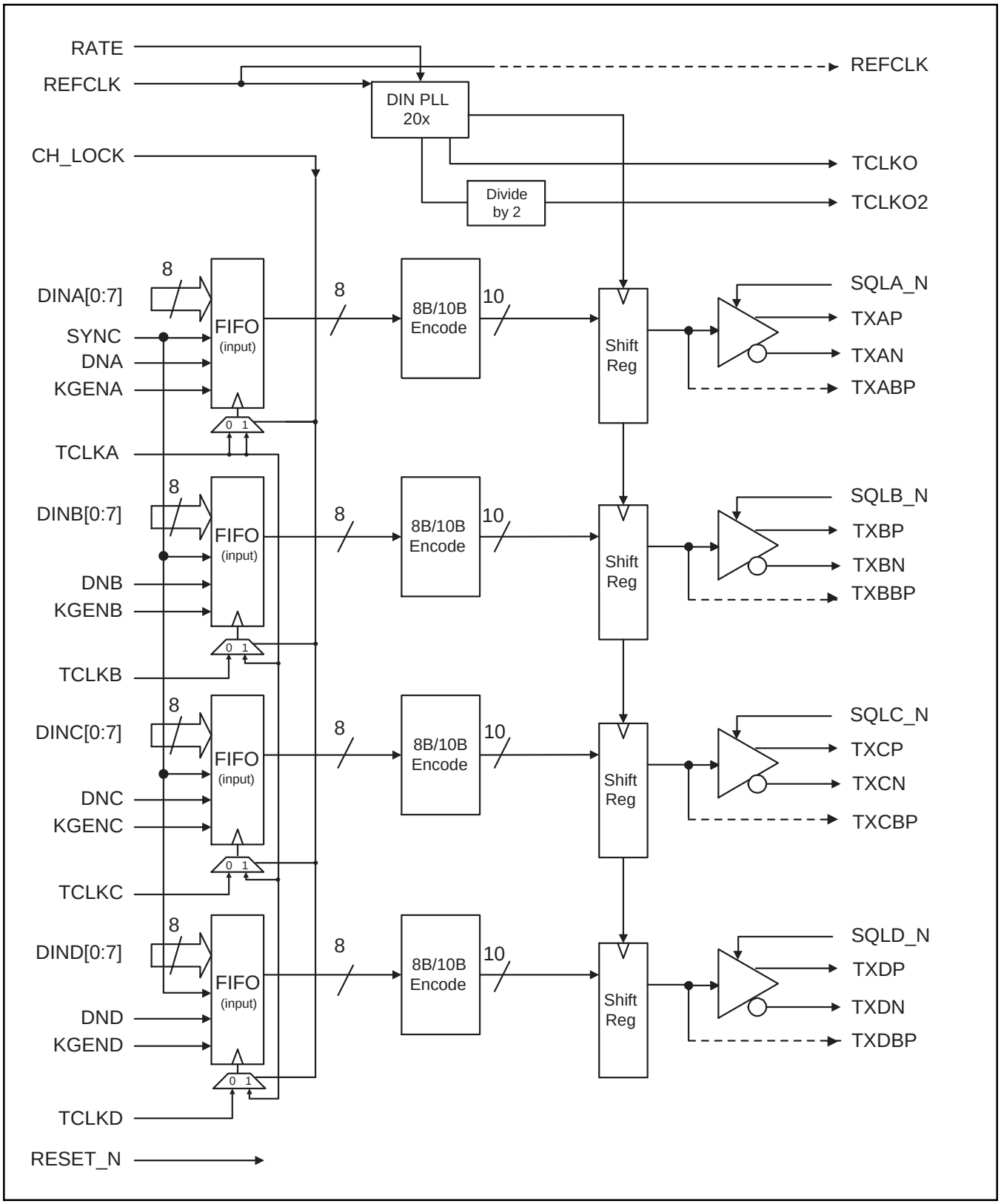
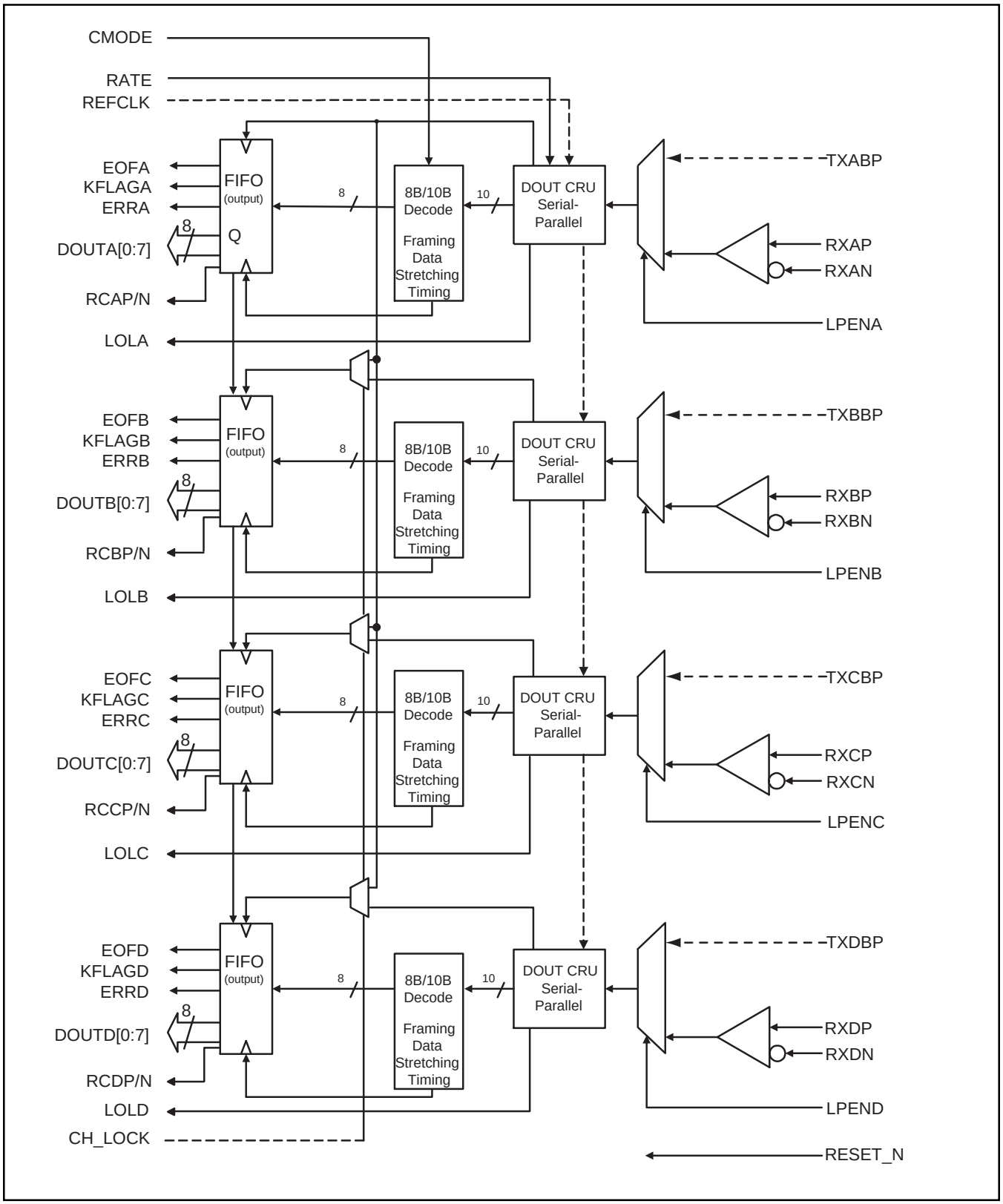


Figure 5. Receiver Block Diagram



TRANSMITTER DESCRIPTION

The transmitter section of the S2009 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Four channels are provided with a variety of options regarding input clocking and loopback. The transmitters can operate in the range of 1.3 to 1.6 GHz, 20 times the reference clock frequency.

Data Input

The S2009 has been designed to simplify the parallel interface data transfer and provides the utmost in flexibility regarding clocking of parallel data. The S2009 incorporates a unique FIFO structure on both the parallel inputs and the parallel outputs which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device.

Data is input to each channel of the S2009 nominally as 10-bit parallel data. This consists of eight data bits of user data, KGEN, and DN. An input FIFO and a clock input, TCLKx, are provided for each channel of the S2009. The device can operate in two different modes. In Channel Lock Mode, all four bytes of input data are clocked into their respective FIFOs using the TCLKA clock. In Independent Mode, each byte of data is clocked into its FIFO with the TCLKx provided with each byte. Table 1 provides a summary of the input modes for the S2009.

Operation in the TCLK Mode makes it easier for users to meet the relatively narrow setup and hold time window required by the parallel 10-bit interface. The TCLKx signal is used to clock the data into an internal holding register and the S2009 synchronizes its internal data flow to insure stable operation. However, regardless of the clock mode, REFCLK is always the VCO reference clock. This facilitates the provision of a clean reference clock resulting in minimum jitter on the serial output. The TCLKx must be frequency locked to REFCLK, but may have an arbitrary phase relationship. Adjustment of internal timing of the S2009 is performed during reset. Once synchronized, the user must insure that the timing of the TCLKx signal does not change by more than ± 3 ns relative to the REFCLK.

Table 1. Input Modes

CH_LOCK	Operation
0	INDEPENDENT MODE. TCLKx MODE. TCLKx used to clock data into FIFOs for all channels. (No receiver byte de-skew.)
1	CHANNEL LOCK MODE. TCLKA MODE. TCLKA used to clock data into FIFOs for all channels. (Receiver byte de-skew active.)

1. Note that internal synchronization of FIFOs is performed upon de-assertion of RESET_N or when the synchronization pattern is generated (SYNC = 1 DNx = 1).

Figure 6. DINx Data Clocking with TCLK

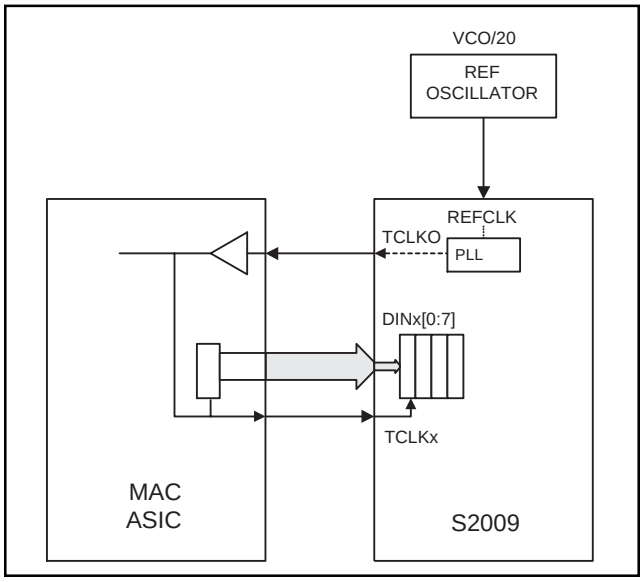


Figure 6 demonstrates the flexibility afforded by the S2009. A low jitter reference is provided directly to the S2009 at 1/20 the serial data rate. Two system clock outputs are provided from the S2009 at both the parallel word rate (TCLKO) and the parallel word rate divided by two (TCLKO2). These two outputs are derived from the PLL and are provided to the upstream circuit as system clocks. The frequency of the TCLKO output is constant at the parallel word rate, 1/10 the serial data rate. The TCLKO2 frequency is constant at the parallel word rate divided by two, 1/20 the serial data rate. These clocks can be buffered as required without concern about added delay. There is no phase requirement between TCLKO or TCLKO2 and TCLKx, which are provided back to the S2009, other than that the output clock that is chosen and TCLKx remain within ± 3 ns of the phase relationship established at reset.

Half Rate Operation

The S2009 supports full and 1/2 rate operation for all modes of operation. When RATE is Low, the S2009 serial data rate equals the VCO frequency. When RATE is High, the VCO is divided by 2 before being provided to the chip. The half rate range for the serial data will be between 650 and 800 MHz. Thus the S2009 can support serial backplane functions at both full and 1/2 the VCO rate. See Table 5.

8B/10B Coding

The S2009 provides 8B/10B line coding for each channel. The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10-bit transmission character. The characters defined by this code ensure that enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

The 8B/10B transmission code includes D-characters, used for data transmission, and K-characters, used for control or protocol functions. Each D-character and K-character has a positive and a negative parity version. The parity of each codeword is selected by the encoder to control the running disparity of the data stream. K-character generation is controlled individually for each channel using the KGENx input. When KGEN is asserted the data on the parallel input is mapped into the corresponding control character. The parity of the K-character is selected to minimize running disparity in the serial data stream. Table 3 lists the K characters supported by the S2009 and identifies the mapping of the DIN[7:0] bits to each character.

[1] 1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

In order to provide interface compatibility to non-AMCC serial backplane transceivers, the S2009 can also generate a unique sync character consisting of 16 consecutive K28.5 characters. This event is initiated by the simultaneous assertion of SYNC and DN. The SYNC character may start with either a positive or negative parity K28.5. (Depending on the current running disparity.) The parity of the second and third K28.5 are inverse with respect to a valid 8B/10B sequence. Parity of the remaining K28.5 are 8B/10B compliant. Thus the parity of the K28.5 pattern consists of + + - - + - + - + - + - + - or - - + + - + - + - + - + - + -.

When operating in the Channel Lock Mode, the KGENx and DNx inputs must be driven for each channel. The SYNC input is common to all four channels. Table 2 identifies the S2009 transmit control signals.

The special SYNC generation commences on the first cycle in which SYNC and DN=1 and continues for 16 cycles. During this period, the SYNC, KGEN, and DN inputs are ignored (assertion of DN and SYNC during this period will not prolong or re-initialize the special sync character generation).

Frequency Synthesizer (PLL)

The S2009 synthesizes a serial transmit clock from the reference signal. Upon startup, the S2009 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

Table 2. Transmitter Control Signals

SYNC	KGENx	DNx	S2009 Output
0	0	0	Encoded Parallel Data.
0	0	1	K28.5 Character.
0	1	1	K Character as defined by Table 3 and DIN[7:0].
1	X	1	Special 16 word SYNC character generated and resets the transmit FIFO.

Note: ‘010’, ‘100’, and ‘110’ are reserved states.

Table 3. K Character Generation (DNx = 1 KGENx =1 SYNC = 0)

K Character	DIN[7:0]	KGEN	Current RD+	Current RD-	Comments
			abcdei fghj	abcdei fghj	
K28.0	000 11100	1	110000 1011	001111 0100	
K28.1	001 11100	1	110000 0110	001111 1001	
K28.2	010 11100	1	110000 1010	001111 0101	
K28.3	011 11100	1	110000 1100	001111 0011	
K28.4	100 11100	1	110000 1101	001111 0010	
K28.5	101 11100	1	110000 0101	001111 1010	Sync Character
K28.6	110 11100	1	110000 1001	001111 0110	
K28.7	111 11100	1	110000 0111	001111 1000	
K23.7	111 10111	1	000101 0111	111010 1000	
K27.7	111 11011	1	001001 0111	110110 1000	
K29.7	111 11101	1	010001 0111	101110 1000	
K30.7	111 11110	1	100001 0111	011110 1000	

Table 4. Data to 8B/10B Alphabetic Representation

	Data Byte									
DIN[0:9] or DOUT[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphanumeric Representation	a	b	c	d	e	i	f	g	h	j

Table 5. Operating Rates

REFCLK Frequency	Serial Output Rate	TCLKO Frequency	TCLKO2 Frequency
SDR/20	1.3-1.6 GHz	SDR/10	SDR/20

Note: SDR = Serial Data Rate.

Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within ±100 ppm of each other to ensure that the clock recovery units can lock to the serial data.

The frequency of the reference clock is 1/20 the serial data rate. The frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate, while the TCLKO2 output is constant at 1/20 the serial data rate. See Table 5.

Serial Data Outputs

The S2009 provides LVPECL level serial outputs. The serial ouputs do not require output pulldown resistors. Outputs are designed to perform optimally when AC-coupled.

When operating in the Channel Lock Mode, the user must insure that the path length of the four high speed serial data signals are matched to within 50 bit times of delay. Failure to meet this requirement may result in bit errors in the received data or in byte misalignment.

In addition to path length induced timing skew, the S2009 can tolerate up to ±3 ns of phase drift between channels after deskewing the outputs.

Test Functions

The S2009 can be configured for factory test to aid in functional testing of the device. When in the test mode, the internal transmit and receive Voltage Controlled Oscillator (VCO) is bypassed and the reference clock substituted. This allows full functional testing of the digital portion of the chip or bypassing the internal synthesized clock with an external clock source. (See Other Operating Modes section.)

Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TCLK to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET_N signal. The transmit FIFO is also reset when the special synchronization pattern (SYNC=1, DN=1) is generated. TCLKO and TCLKO2 will operate normally regardless of the state of RESET_N.

RECEIVER DESCRIPTION

Each receiver channel is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 5.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2009 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

The S2009 provides the capability to operate with all four channels locked together (Channel Lock Mode). Channel lock process and status reporting is described below.

Data Input

A differential input receiver is provided for each channel of the S2009. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for each channel is enabled by its respective LPEN input.

The high speed serial inputs to the S2009 are internally biased to V_{DD}-1.3 V. All that is required externally is AC-coupling and line-to-line differential termination.

Clock Recovery Function

Clock recovery is performed on the input data stream for each channel of the S2009. The receiver PLL has been optimized for the anticipated needs of Serial Backplane systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs. If at any time the frequency or run length checks are violated, the state machine forces the receive PLL to lock to the reference clock. This allows the PLL to maintain the correct frequency in the absence of data.

The 'lock to reference' frequency criteria insure that the S2009 will respond to variations in the serial data input frequency (compared to the reference frequency). The New Lock State is dependent upon the current lock state, as shown in Table 6.

The run length criteria ensure that the S2009 will respond appropriately and quickly to a loss of signal. The run length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus 119 or less consecutive ones or zeros does not cause signal loss, 160 or more causes signal loss, and 120 through 159 may or may not, depending on how the data aligns across the four clock byte boundaries. When the run length checker criterion is exceeded, "Loss of Sync" will report independently on each channel until the consecutive ones or zeros stream sees a change in polarity and the receive PLL has locked to the serial data input.

If both the off-frequency detect circuitry test and the run length test are satisfied, the CRU will attempt to lock to the incoming data. When lock is achieved, "Loss of Lock" is removed on the ERRx, EOFx, and KFLAGx status lines. LOLx will report a logic 0 when lock is achieved (LOLx is an asynchronous, unfiltered signal). The unfiltered LOLx pins will have a tendency to pulse High and Low between PLL lock and unlock. When the PLL is trying to acquire lock, it tends to drift in and out of lock. This is due to the PLL always trying to lock to data until it finally achieves lock to the receive data stream, therefore, during this situation you can have rapid High and Low changes on the LOLx outputs. When the receive PLL locks to data, the LOLx signal is stable. It is possible for the run length test to be satisfied due to noise on the inputs, even if no signal is present. In this case the lock detect status may periodically assert as the receive PLL frequency approaches that of the REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RCxP/N outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

Table 6. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. REFCLK)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

When operating in independent mode, PLL "Loss of Lock" status for each channel is indicated by a continuous 1-0-1 on its respective ERR, EOF, and KFLAG outputs. LOLx will report a logic 1 asynchronously when "Loss of Lock" occurs. When operating in the Channel Lock Mode, PLL locking of all four channels must be accomplished before byte-skewing is achieved and "Channel Lock Detected" status can be indicated on the ERR, EOF, KFLAG, and LOL outputs.

Reference Clock Input

A single reference clock, which serves both transmitter and receiver, must be provided from a low jitter clock source. The frequency of the received data stream (divided-by-20) must be within ±100 ppm of the reference clock to insure reliable locking of the receiver PLL.

Serial-to-Parallel Conversion

Once bit synchronization has been attained by the S2009 CRU, the S2009 must synchronize to the 10-bit word boundary. Word synchronization in the S2009 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2009 will detect and byte-align to either polarity of the K28.5. Each channel of the S2009 will detect and align to a K28.5 anywhere in the data stream. Two modes of operation are supported: Normal Mode, in which the channels operate independently and Channel Lock Mode, in which the channels are locked together to form a virtual 32-bit interface.

For Channel Lock operation, the S2009 must provide an additional level of synchronization to insure that differences in delay encountered by the four channels do not result in parallel output data from each channel leading or lagging by one parallel clock cycle. In Channel Lock Mode, assertion of DNA results in the K28.5 being transmitted simultaneously on all four channels. Each receiver provides a FIFO buffer and adjusts the delay through this buffer to ensure that the first data following the K28.5 is output simultaneously from the receiver on the parallel interface. Table 7 details the function of the EOF, KFLAG, ERR, and LOL pins in status reporting. For Channel Lock operation, a single output clock, RCA P/N, is provided synchronous with the data. The other RCx P/N clocks will be frequency locked, but will have an arbitrary phase relationship with the data.

Channel Lock Mode Synchronization

Incidental errors occurring in the received data can transform a normal data character into a K28.5 character. To prevent this occurrence from making the channel locking process unnecessarily vulnerable to bit errors, the S2009 implements a channel lock state machine for each channel with linkage between channels to move to the final deskewed state.

The Channel Lock state diagram is shown in Figure 7. The S2009 powers up in the "No Sync" state. When in the "No Sync" state, each channel of the S2009 is actively searching the received data stream for the occurrence of a K28.5 and will align its demultiplexer to the character when detected, and will enter the "Acquiring Sync" state. K28.5 will be reported on each channel as 0-1-1 (err-eof-kflag). When four or more consecutive K28.5 characters are received on a given channel, the channel will enter the "Re-sync" state as shown in Figure 7. "Re-sync" state status will be reported as 1-1-1 until the S2009 deskewing circuitry has aligned the data output from each channel such that the first valid non-errored codeword (or data character) other than a K28.5 for each channel is output simultaneously[1]. The device will move to the "In Sync" state and indicate channel lock status by each channel as a 0-1-0. See Figure 8. Note that "Re-sync" is reported independently by each channel regardless of the state of the other channels. However, "In Sync" can only be reported when all four channels are in the "In Sync" state and detect a valid data character within the deskew window[2]. The "In Sync" state is reported simultaneously for each channel as 0-1-0.

Once the S2009 has entered the "In Sync" state, it will report status but will not alter the relative skew of the output FIFOs. The S2009 will exit the "In Sync" state and move to the "No Sync" state if one of the four CRUs reports a loss of lock, if the 8B/10B decoder observes five consecutive decoding errors, or if the decoder error rate >50% in a block of 16 codewords. The error rate of greater than 50% in a block of 16 and five or more sequential decoding errors is calculated on a per K28.5 basis. The error counter resets whenever a K28.5 character is received or an unlock condition occurs. The device can also be put in the "No Sync" state by setting TCLKD=Low for at least 16 clocks, or by asserting RESET_N Low.

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1. Note, if the S2009 does not have to delay any of the channels for word alignment, "Re-sync" reporting (1-1-1) will not be seen and Channel Lock status will be reported simultaneously on the four channels as 0-1-0.

2. Note when CMODE = 0, if the deskew window to channel lock is exceeded, indeterminate status will be reported.

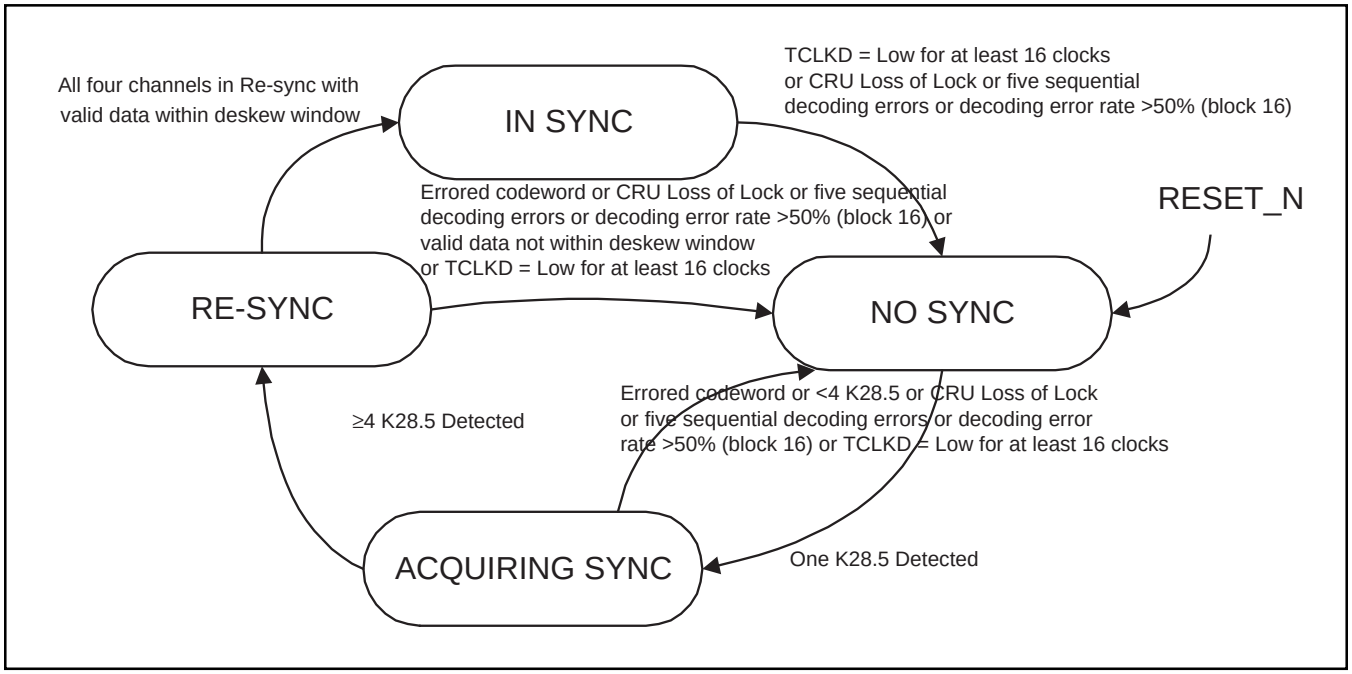
TCLKD is used to reset the Channel Lock state machine and initialize the FIFOs in the receive data path. Assertion of TCLKD Low does not interrupt the transmit data path.

When not in Channel Lock Mode, the linkage between the four state machines is broken and each channel operates independently.

Loss of Channel Lock will be reported as indicated in Table 7 by a 1-0-1 on the ERR, EOF, and KFLAG signals, respectively. This is during the “No Sync” state. The status lines will reflect the status of the individual channels and the device will respond to appropriate channel locking sequences and deskew as necessary. Persistence of 1-0-1 status on any channel or a logic 1 on LOLx is indicative of CRU lock failure, most likely resulting from loss of receiver input signal. The device will then respond to the channel locking sequence.

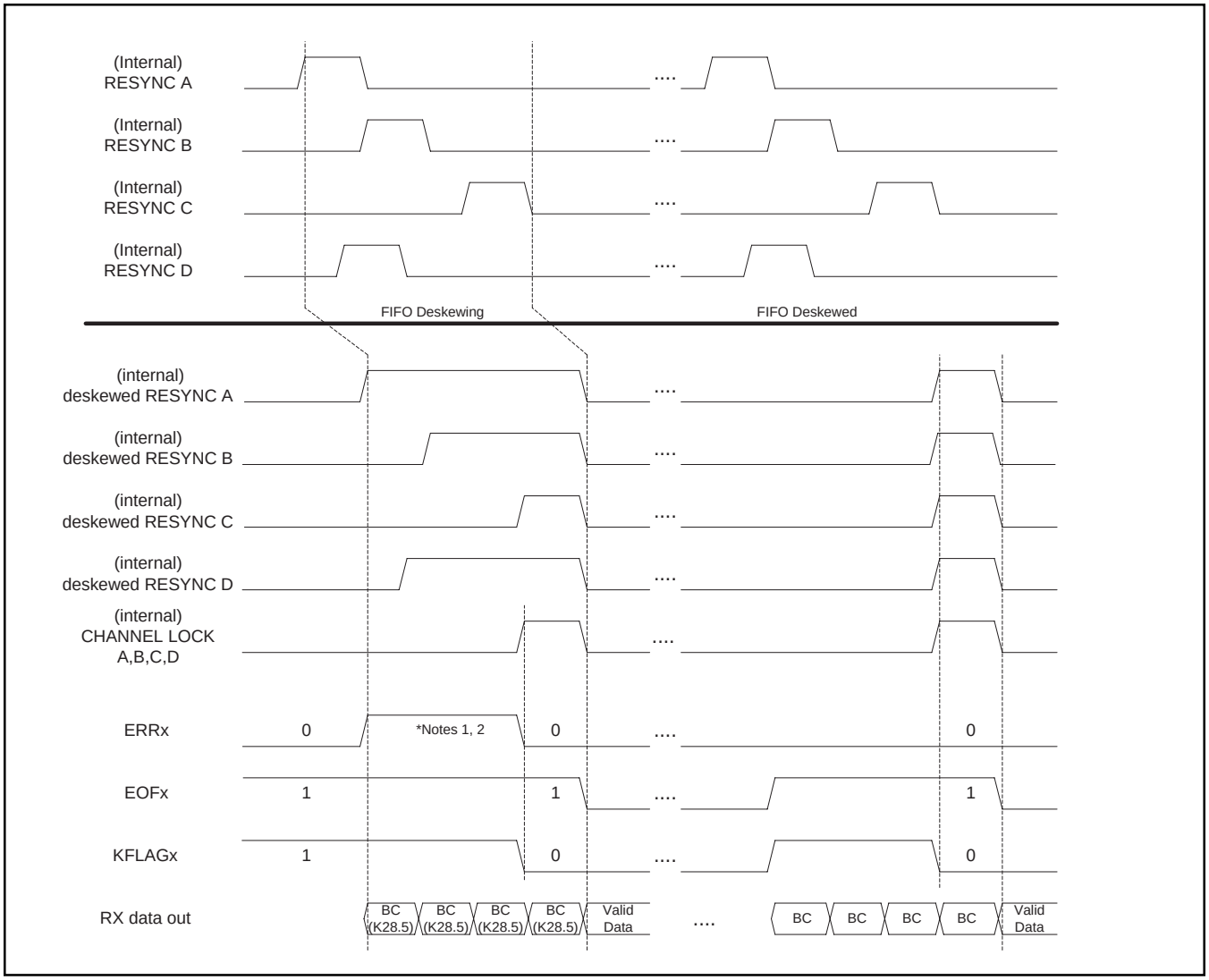
When operating in the Channel Lock Mode, the TCLKB input must be tied Low.

Figure 7. Channel Lock State Machine



Note: Errored codeword means “Codeword violation” or “Parity error.”

Figure 8. Channel Lock Synchronization Timing



1. The first three K28.5's will be reported as "K28.5" (011), subsequent K28.5 will be reported as "Re-sync" or "Channel Lock Detected." See Table 7.
2. "Re-sync(s)" (111 status) may be seen on the parallel outputs during "Re-sync" due to deskewing function.

Table 7. Error and Status Reporting, Channel Lock and Independent Mode

ERR	EOF	KFLAG	Description	Rank
0	0	0	Normal Character. Indicates that a valid data character has been detected.	7
0	0	1	K Character (not K28.5). Indicates that a K Character other than K28.5 has been detected.	7
0	1	0	Channel Lock Detected[1]. Asserts for one parallel word on the ERRx, EOFx, and KFLAGx signals that all four channels have identified the "Re-sync" sequence within the byte deskew window. When in the "In Sync" state, the S2009 will continue to report status, but will not re-deskew the output FIFOs.	2
0	1	1	K28.5+ or K28.5-. Indicates that a K28.5 character of arbitrary parity has been detected.	5
1	0	0	Codeword Violation. Indicates that a word not corresponding to any valid Dx.x or Kx.x mapping has been received.	4
1	0	1	Loss of Sync. Independent Mode (CH_LOCK = 0) In Independent Mode, this status will assert to indicate that loss of CRU bit lock has occured on a specific channel. Individual reporting on ERRx, EOFx, and KFLAGx will indicate which channel's CRU has lost bit lock. This reporting will remain asserted until its CRU has locked to data. "Loss of Sync" will also assert when the run length checker criterion is exceeded. Channel Lock Mode (CH_LOCK = 1) In Channel Lock Mode, this status will assert for at least one parallel word to indicate that a condition has occured on a channel (or channels) which results in loss of channel lock. Note, when channel locked, the user must monitor all four channels' status reporting to know when the Channel Lock link has been broken between the four channels. The non-errored channels will continue to report normal status. "Loss of Sync" status will also be reported for a channel until its CRU has locked to data. Another case in which this status will assert is when the run length checker criterion is exceeded.	1
1	1	0	Parity Error. Indicates that a running disparity error has been observed.	6
1	1	1	Re-sync[1] (K28.5 x 4 + Valid non-errored codeword (or data character) other than a K28.5). If any channel(s) have to be delayed for word alignment, multiple "Re-syncs" (111 status) can occur on these channel(s) having to delay themselves for proper word alignment. This function (deskewing) is performed within the S2009. If the S2009 does not have to delay any of the channels for word alignment, "Re-sync" reporting will not be seen and channel lock status will be reported simultaneously on all four channels. "Re-sync" reporting indicates that four or more consecutive K28.5 characters followed by a valid non-errored codeword (or data character) other than a K28.5 has been received. Each channel reports this condition independently and all four channels must identify the re-sync within the allowed byte deskew time before channel lock can be achieved and be indicated with Channel Lock Detected (see above).	3

LOL	Description
0	Indicates that the CRU is locked to data.
1	Indicates that the CRU has lost bit lock. This reporting will deassert when the CRU has locked to data.

Note: LOL is an asynchronous, unfiltered signal.
1. This status reporting is not available in Independent Mode (CH_LOCK = 0).

CHANNEL LOCKING/RE-LOCKING PROCEDURE

The channel locking/relocking procedures are summarized below. Following these procedures will insure proper Channel Lock operation of the device. When powered up, the S2009 will lock to the received data within approximately 2500 bit times. The CRU must report lock for approximately 32,000 REFCLK periods (320 μs) before channel locking is enabled.

1. Ensure that the S2009 is in the "No Sync" state. This can be accomplished by resetting the device (RESET_N Low) or by asserting TCLKD Low for at least 16 clocks.
2. The transmitter portion of another S2009 device initiates the appropriate synchronization sequence. Four or more K28.5 characters or the 16 word SYNC sequence followed by a valid non-errored codeword (or data character) other than a K28.5 can be used to de-skew the DOUT FIFOs. In the transmitter, the 16 word SYNC character can be generated by asserting SYNC=1 and DN[A:D]=1. See the transmit portion of the specification for a complete description.
3. Wait for "Channel Lock Detected" as defined by Table 7.

While in the "In Sync" state, the S2009 will enter the "No Sync" state if: any CRU loses lock, if five or more consecutive decoder errors are received, if the decoder error rate exceeds 50% in a block of 16 bytes, if RESET_N is asserted Low, or if TCLKD is asserted Low for at least 16 clocks. Note that if any CRU has failed to lock to the incoming data, this will be reported by the appropriate channel as "Loss of Sync" and "Loss of Lock" (LOLx) (see Table 7). To reacquire sync after moving to the "No Sync" state, repeat steps 2 and 3 above.

8B/10B Decoding

After serial to parallel conversion, the S2009 provides 8B/10B decoding of the data. The received 10-bit code word is decoded to recover the original 8-bit data. The decoder reports either invalid code word errors or running disparity errors. Error type is determined by examining Table 7. When more than one reportable condition occurs simultaneously, reporting is in accordance with the rank assigned by Table 7.

Data Output

Data is output on the DOUT[0:7] outputs. K-characters are flagged using the KFLAG signal. The EOF (with KFLAG) is used to indicate the reception of a valid K28.5 character. Invalid codewords and decoding errors are indicated on the ERR output. KFLAG, EOF, and ERR are buffered with the data in the FIFO to insure that all outputs are synchronized at the S2009 outputs. Errors are reported independently for each channel in both Channel Lock Mode and Independent Mode operation.

The S2009 TTL outputs are optimized to drive 65 Ω line impedances. Internal source matching provides good performance on unterminated lines of reasonable length.

Parallel Output Clock Rate

Two output clock modes are supported, as shown in Table 8. When CMODE is High, a complementary TTL clock at the data rate is provided on the RCxP/N outputs. Data should be clocked on the rising edge of RCxP. When CMODE is Low, a complementary TTL clock at 1/2 the data rate is provided. Data should be latched on the rising edge of RCxP and the rising edge of RCxN.

The S2009 follows the Gigabit Ethernet standard which requires that the parallel clock output rate be at half the word rate. In addition, the phase of the RCxP/N clock must be adjusted such that the K28.5 appears on the rising edge of the RCxP signal. To insure compatibility with the Gigabit Ethernet standard, the S2009 will buffer data such that this requirement is met. This concept is referred to as data stretching.

In Gigabit Ethernet applications, multiple consecutive K28.5 characters should not be generated. However, for serial backplane applications this can occur. The S2009 must be able to operate properly when multiple K28.5 characters are received. When CMODE is Low, the S2009 guarantees that the last K28.5 character before a non-K28.5 character will always line up with the rising edge of RCxP. Because of this, the last data character or codeword (including K28.5) prior to a sequence of one or more K28.5 characters may be either duplicated or lost.

Table 8. Output Clock Mode

Mode	CMODE	RCx P/N Freq
Half Clock Mode	0	VCO/20
Full Clock Mode	1	VCO/10

Table 8A. S2009 Data Clocking

CH_LOCK	Input Clock Source	Output Clock Source
0	TCLKx	RCx (derived from CRUx)
1	TCLKA	RCA (derived from CRUA)

OTHER OPERATING MODES

Operating Frequency Range

The S2009 is designed to operate at serial baud rates of 1.3 to 1.6 GHz (1.04 – 1.28 Gbps user data rate).

Loopback Mode

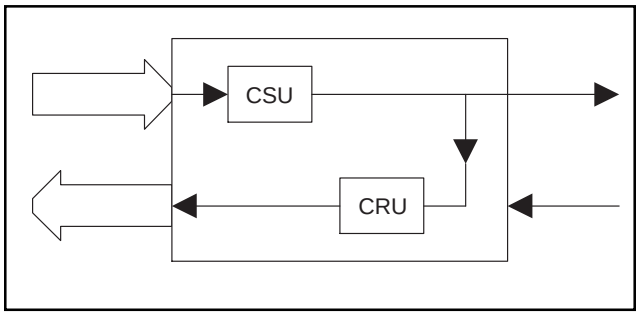
When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver, as shown in Figure 9. This provides the ability to perform system diagnostics and off-line testing of the interface to verify the integrity of the serial channel. Loopback mode is enabled independently for each channel using its respective Loopback Enable input (LPENx).

When squelch is enabled, the transmitter output driver is powered down. The serial outputs (TXP and TXN) will be held at a logic High state due to source followers, which in turn makes the differential state, TXP minus TXN, indeterminate. Squelch is enabled independently for each channel using its respective Squelch input (SQLx_N).

TEST MODES

The S2009 has a testability input to aid in functional testing of the device. The test mode is entered when CH_LOCK is High and TCLKB is High. Thus users must take care to insure that TCLKB is held Low when operating in Channel Lock Mode.

Figure 9. S2009 Diagnostic Loopback Operation



Notes:
1. Serial output data remains active during loopback operation to enable other system tests to be performed.
2. Serial output data will become inactive during squelch operation

JTAG TESTING

The JTAG implementation for the S2009 is compliant with the IEEE1149.1 requirements. JTAG is used to test the connectivity of the pins on the chip. The Test Access Port (TAP) provides access to the test logic of the chip. When Test Reset (TRS) is asserted the TAP is initialized. TAP is a state machine that is controlled by Test Mode Select (TMS). The test instruction and data are loaded through Test Data In (TDI) on the rising edge of Test Clock (TCK). When TMS is High, the test instruction is loaded into the instruction register. When TMS is Low, the test data is loaded into the data register. Test Data Out (TDO) changes on the falling edge of TCK. All input pins, including clocks, that have boundary scan are observe only. They can be sampled in either normal operational or test mode. All output pins that have boundary scan, are observe and control. They can be sampled as they are driven out of the chip in normal operational mode, and they can be driven out of the chip in test mode using the Extest instruction. Since JTAG testing operates only on digital signals there are some pins with analog signals that JTAG does not cover. The JTAG implementation has the three required instruction, Bypass, Extest, and Sample/Preload.

JTAG Instruction Description:

The BYPASS register contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and TDO pins of a component when no test operation of that component is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

The SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instructions.

The IDCODE instruction allows selection of the device identification register to be connected for serial access between Test Data Input (TDI) and Test Data Output (TDO). When the IDCODE instruction of the device is selected, all test data registers perform their system function.

The following table provides a list of the pins that are JTAG tested. Each port has a Boundary Scan Register (BSR), unless otherwise noted. The following features are described: the JTAG mode of each register (input, output2, or internal (refers to an internal package pin)), the direction of the port if it has a boundary scan register (in or out), and the position of this register on the scan chain.

Table 9. JTAG Pin Assignments

S2009 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
SYNC	sync	Input	0	-
CMODE	cmode	Input	1	-
CH_LOCK	chan_lock	Input	2	-
LPEND	lpend	Input	3	-
LPENC	lpenc	Input	4	-
LPENB	lpenb	Input	5	-
LPENA	lpena	Input	6	-
		Internal	7	-
		Internal	8	-
		Internal	9	-
RESET_N	reset	Input	10	-
REFCLK	refclk	Input	11	-
TCLKO	transmit_clk_buf _out	Output2	-	12
DND	dnd	Input	13	-
KGEND	kgend	Input	14	-
DIND7	tdatain_d (7)	Input	15	-
DIND6	tdatain_d (6)	Input	16	-
DIND5	tdatain_d (5)	Input	17	-
DIND4	tdatain_d (4)	Input	18	-
DIND3	tdatain_d (3)	Input	19	-
DIND2	tdatain_d (2)	Input	20	-
DIND1	tdatain_d (1)	Input	21	-
DIND0	tdatain_d (0)	Input	22	-
TCLKD	tclkd	Input	23	-
DNC	dnc	Input	24	-
KGENC	kgenc	Input	25	-
DINC7	tdatain_c (7)	Input	26	-
DINC6	tdatain_c (6)	Input	27	-
DINC5	tdatain_c (5)	Input	28	-
DINC4	tdatain_c (4)	Input	29	-
DINC3	tdatain_c (3)	Input	30	-
DINC2	tdatain_c (2)	Input	31	-
DINC1	tdatain_c (1)	Input	32	-
DINC0	tdatain_c (0)	Input	33	-
TCLKC	tclkc	Input	34	-
KGENB	kgenb	Input	35	-
DNB	dnb	Input	36	-
DINB7	tdatain_b (7)	Input	37	-
DINB6	tdatain_b (6)	Input	38	-
DINB5	tdatain_b (5)	Input	39	-
DINB4	tdatain_b (4)	Input	40	-
DINB3	tdatain_b (3)	Input	41	-
DINB2	tdatain_b (2)	Input	42	-
DINB1	tdatain_b (1)	Input	43	-
DINB0	tdatain_b (0)	Input	44	-
TCLKB	tclkb	Input	45	-
DNA	dna	Input	46	-
KGENA	kgena	Input	47	-
DINA7	tdatain_a (7)	Input	48	-
DINA6	tdatain_a (6)	Input	49	-
DINA5	tdatain_a (5)	Input	50	-
DINA4	tdatain_a (4)	Input	51	-
DINA3	tdatain_a (3)	Input	52	-
DINA2	tdatain_a (2)	Input	53	-
DINA1	tdatain_a (1)	Input	54	-
DINA0	tdatain_a (0)	Input	55	-
TCLKA	tclka	Input	56	-
RCDP	rcdp	Output2	-	57
RCDN	rcdn	Output2	-	58
DOUTD7	rdataout_d (7)	Output2	-	59
DOUTD6	rdataout_d (6)	Output2	-	60
DOUTD5	rdataout_d (5)	Output2	-	61
DOUTD4	rdataout_d (4)	Output2	-	62
DOUTD3	rdataout_d (3)	Output2	-	63
DOUTD2	rdataout_d (2)	Output2	-	64
DOUTD1	rdataout_d (1)	Output2	-	65
DOUTD0	rdataout_d (0)	Output2	-	66
EOFD	eofd_d	Output2	-	67
KFLAGD	kflagd_d	Output2	-	68
ERRD	errd_d	Output2	-	69
RCCP	rccp	Output2	-	70
RCCN	rccn	Output2	-	71
DOUTC7	rdataout_c (7)	Output2	-	72
DOUTC6	rdataout_c (6)	Output2	-	73
DOUTC5	rdataout_c (5)	Output2	-	74
DOUTC4	rdataout_c (4)	Output2	-	75
DOUTC3	rdataout_c (3)	Output2	-	76
DOUTC2	rdataout_c (2)	Output2	-	77
DOUTC1	rdataout_c (1)	Output2	-	78
DOUTC0	rdataout_c (0)	Output2	-	79

Table 9. JTAG Pin Assignments (Continued)

S2009 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
ERRC	errd_c	Output2	-	80
EOFC	eofd_c	Output2	-	81
KFLAGC	kflag_c	Output2	-	82
RCBP	rcbp	Output2	-	83
RCBN	rcbn	Output2	-	84
KFLAGB	kflagd_b	Output2	-	85
DOUTB7	rdataout_b (7)	Output2	-	86
DOUTB6	rdataout_b (6)	Output2	-	87
DOUTB5	rdataout_b (5)	Output2	-	88
DOUTB4	rdataout_b (4)	Output2	-	89
DOUTB3	rdataout_b (3)	Output2	-	90
DOUTB2	rdataout_b (2)	Output2	-	91
DOUTB1	rdataout_b (1)	Output2	-	92
DOUTB0	rdataout_b (0)	Output2	-	93
EOFB	eofd_b	Output2	-	94
ERRB	errd_b	Output2	-	95
RCAP	rcap	Output2	-	96
RCAN	rcan	Output2	-	97
ERRA	errd_a	Output2	-	98
DOUTA7	rdataout_a (7)	Output2	-	99
DOUTA6	rdataout_a (6)	Output2	-	100
DOUTA5	rdataout_a (5)	Output2	-	101
DOUTA4	rdataout_a (4)	Output2	-	102
DOUTA3	rdataout_a (3)	Output2	-	103
DOUTA2	rdataout_a (2)	Output2	-	104
DOUTA1	rdataout_a (1)	Output2	-	105
DOUTA0	rdataout_a (0)	Output2	-	106
EOFA	eofd_a	Output2	-	107
KFLAGA	kflagd_a	Output2	-	108
		Internal	-	109

S2009 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
JTAG Control Pins (Ports that do not have a Boundary Scan Register)				
TCK	jtag_tck	-	-	-
TDI	jtag_tdi	-	-	-
TDO	jtag_tdo	-	-	-
TMS	jtag_tms	-	-	-
TRS	jtag_trs	-	-	-
Pins not JTAG Tested				
TXAP	-	-	-	-
TXAN	-	-	-	-
TXBP	-	-	-	-
TXBN	-	-	-	-
TXCP	-	-	-	-
TXCN	-	-	-	-
TXDP	-	-	-	-
TXDN	-	-	-	-
RATE	-	-	-	-
RXAP	-	-	-	-
RXAN	-	-	-	-
RXBP	-	-	-	-
RXBN	-	-	-	-
RXCP	-	-	-	-
RXCN	-	-	-	-
RXDP	-	-	-	-
RXDN	-	-	-	-
TCLKO2	-	-	-	-
LOLA	-	-	-	-
LOLB	-	-	-	-
LOLC	-	-	-	-
LOLD	-	-	-	-
SQLA_N	-	-	-	-
SQLB_N	-	-	-	-
SQLC_N	-	-	-	-
SQLD_N	-	-	-	-

Table 10. Transmitter Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	P12 R12 T13 T12 U13 P11 R11 T11	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TCLKA. (See Table 1.)
DNA	TTL	I	U15	DATA_NOT for Channel A. When Low, data present on DINA[0:7] is 8B/10B encoded and transmitted serially. When High, special character sequences are generated as indicated in Table 2.
KGENA	TTL	I	U14	K-Character Generation for Channel A. KGENA High causes the data on DINA[0:7] to be encoded into a K-Character. (See Table 2.)
TCLKA	TTL	I	U12	Transmit Data Clock A. When CH_LOCK is Low, this signal is used to clock data on DINA[0:7], KGENA, and DNA into the S2009. When CH_LOCK is High, TCLKA clocks the data into all four transmit FIFOs.
DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	R15 P14 T15 R14 U17 U16 P13 T14	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TCLKA or TCLKB. (See Table 1.)
DNB	TTL	I	R16	DATA_NOT for Channel B. When Low, data present on DINB[0:7] is 8B/10B encoded and transmitted serially. When High, special character sequences are generated as indicated in Table 2.
KGENB	TTL	I	T16	K-Character Generation for Channel B. KGENB High causes the data on DINB[0:7] to be encoded into a K-Character. (See Table 2.)
TCLKB	TTL	I	R13	Transmit Data Clock B. When CH_LOCK is Low, this signal is used to clock data on DINB[0:7], KGENB, and DNB into the S2009. When CH_LOCK = High, TCLKB must be tied Low.
DINC7 DINC6 DINC5 DINC4 DINC3 DINC2 DINC1 DINC0	TTL	I	M15 N16 M14 R17 P16 N15 T17 N14	Transmit Data for Channel C. Parallel data on this bus is clocked in on the rising edge of TCLKA or TCLKC. (See Table 1.)

Table 10. Transmitter Signal Input Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DNC	TTL	I	N17	DATA_NOT for Channel C. When Low, data present on DINC[0:7] is 8B/10B encoded and transmitted serially. When High, special character sequences are generated as indicated in Table 2.
KGENC	TTL	I	P17	K-Character Generation for Channel C . KGENC High causes the data on DINC[0:7] to be encoded into a K-Character. (See Table 2.)
TCLKC	TTL	I	P15	Transmit Data Clock C. When CH_LOCK is Low, this signal is used to clock data on DINC[0:7], KGENC, and DNC into the S2009. When CH_LOCK is High, TCLKC is ignored.
DIND7 DIND6 DIND5 DIND4 DIND3 DIND2 DIND1 DIND0	TTL	I	L17 K16 K15 K14 M17 L16 M16 L15	Transmit Data for Channel D. Parallel data on this bus is clocked in on the rising edge of TCLKA or TCLKD. (See Table 1.)
DND	TTL	I	J16	DATA_NOT for Channel D. When Low, data present on DIND[0:7] is 8B/10B encoded and transmitted serially. When High, special character sequences are generated as indicated in Table 2.
KGEND	TTL	I	K17	K-Character Generation for Channel D. KGEND High causes the data on DIND[0:7] to be encoded into a K-Character. (See Table 2.)
TCLKD	TTL	I	L14	Transmit Data Clock D. When CH_LOCK is Low, this signal is used to clock data on DIND[0:7], KGEND, and DND into the S2009. In Channel Lock Mode, CH_LOCK = High, TCLKD (Low for at least 16 clocks) is used to reset the Channel Lock state machine and RX FIFOs.
SYNC	TTL	I	D4	Sync Character. When High, (See Table 2) used to generate a special sequence of K28.5 charaters. See earlier text.

Table 11. Transmitter Output Signals

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	A17 B17	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	C17 D17	High speed serial outputs for Channel B.
TXCP TXCN	Diff. LVPECL	O	E17 F16	High speed serial outputs for Channel C.
TXDP TXDN	Diff. LVPECL	O	F17 G17	High speed serial outputs for Channel D.
TCLKO	TTL	O	J14	TTL Output Clock at the parallel data rate. This clock is provided for use by up-stream circuitry.
TCLKO2	TTL	O	G4	TTL Output Clock at the parallel data rate divided by 2. This clock is provided for use by up-stream circuitry.

Table 12. Mode Control Signals

Pin Name	Level	I/O	Pin #	Description
CH_LOCK	TTL	I	E4	Channel Lock. Parallel input mode control. CH_LOCK High locks all four channels together. (See Table 1.)
REFCLK	TTL	I	H17	Reference Clock. Used for the transmit VCO and frequency check for the clock recovered from the receiver serial data.
RESET_N	TTL	I	C15	Reset. When Low, the S2009 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET_N. When High, the S2009 operates normally.
RATE	TTL	I	D12	Rate. When Low, the S2009 operates with the serial output rate equal to the VCO frequency. When High, the S2009 operates with the VCO internally divided by 2 for all functions.
SQLA_N	TTL	I	E14	Squelch Control for Channel A. When High, the serial outputs are active. When Low, the transmitter output driver is powered down and the outputs become inactive.
SQLB_N	TTL	I	D16	Squelch Control for Channel B. When High, the serial outputs are active. When Low, the transmitter output driver is powered down and the outputs become inactive.
SQLC_N	TTL	I	F14	Squelch Control for Channel C. When High, the serial outputs are active. When Low, the transmitter output driver is powered down and the outputs become inactive.
SQLD_N	TTL	I	F15	Squelch Control for Channel D. When High, the serial outputs are active. When Low, the transmitter output driver is powered down and the outputs become inactive.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 13. Receiver Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	J1 J3 J2 H1 H2 H3 F1 G2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCAP in full clock mode and valid on rising edge of both RCAP and RCAN in half clock mode.
EOFA	TTL	O	F2	Channel A End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:7]. (See Table 7.)
KFLAGA	TTL	O	G3	Channel A K-Character Flag. A High in KFLAGA indicates that a valid control character has been detected. Data present on the parallel interface DOUTA[0:7] should be used to indicate which character was received. (See Table 7.)
ERRA	TTL	O	G1	Channel A Receive Error. A High on ERRA signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. (See Table 7.)
LOLA	TTL	O	C5	Channel A Loss of Lock Detected. LOLA High indicates that the CRU on channel A has lost bit lock. This signal will deassert when the CRU has locked to data. When in Channel Lock Mode, this signal will assert indicating that the channel A CRU is not bit locked. This will report asynchronously. (See Table 7.)
RCAP RCAN	TTL	O	K2 K1	Receive Data Clock for Channel A. Parallel receive data, DOUTA[0:7], EOFA, KFLAGA, and ERRA are valid on the rising edge of RCAP when in full clock mode and valid on the rising edge of both RCAP and RCAN in half clock mode.
DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	R1 P1 M3 N2 M2 N1 L2 M1	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCBP in full clock mode and valid on rising edge of both RCBP and RCBN in half clock mode.
EOFB	TTL	O	L1	Channel B End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:7]. (See Table 7.)
KFLAGB	TTL	O	P2	Channel B K-Character Flag. A High in KFLAGB indicates that a valid control character has been detected. Data present on the parallel interface DOUTB[0:7] should be used to indicate which character was received. (See Table 7.)

Table 13. Receiver Output Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
ERRB	TTL	O	K3	Channel B Receive Error. A High on ERRB signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. (See Table 7.)
LOLB	TTL	O	D7	Channel B Loss of Lock Detected. LOLB High indicates that the CRU on channel B has lost bit lock. This signal will deassert when the CRU has locked to data. When in Channel Lock Mode, this signal will assert indicating that the channel B CRU is not bit locked. This will report asynchronously. (See Table 7.)
RCBP RCBN	TTL	O	U1 T1	Receive Data Clock for Channel B. Parallel receive data, DOUTB[0:7], EOFB, KFLAGB, and ERRB are valid on the rising edge of RCBP when in full clock mode and valid on the rising edge of both RCBP and RCBN in half clock mode.
DOUTC7 DOUTC6 DOUTC5 DOUTC4 DOUTC3 DOUTC2 DOUTC1 DOUTC0	TTL	O	R7 R6 T5 U3 T4 R5 U2 T3	Channel C Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCCP in full clock mode and valid on the rising edge of both RCCP and RCCN in half clock mode.
EOFC	TTL	O	R2	Channel C End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTC[0:7]. (See Table 7.)
KFLAGC	TTL	O	P3	Channel C K-Character Flag. A High in KFLAGC indicates that a valid control character has been detected. Data present on the parallel interface DOUTC[0:7] should be used to indicate which character was received. (See Table 7.)
ERRC	TTL	O	T2	Channel C Receive Error. A High on ERRC signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. (See Table 7.)
LOLC	TTL	O	C9	Channel C Loss of Lock Detected. LOLC High indicates that the CRU on channel C has lost bit lock. This signal will deassert when the CRU has locked to data. When in Channel Lock Mode, this signal will assert indicating that the channel C CRU is not bit locked. This will report asynchronously. (See Table 7.)
RCCP RCCN	TTL	O	U5 U4	Receive Data Clock for Channel C. Parallel receive data, DOUTC[0:7], EOFC, KFLAGC, and ERRC are valid on the rising edge of RCCP when in full clock mode and valid on the rising edge of both RCCP and RCCN in half clock mode.

Table 13. Receiver Output Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUTD7 DOUTD6 DOUTD5 DOUTD4 DOUTD3 DOUTD2 DOUTD1 DOUTD0	TTL	O	U11 R10 U9 R9 T9 U8 U7 T8	Channel D Receiver Data outputs. Parallel data on this bus is valid on the rising edge of RCDP in full clock mode and valid on rising edge of both RCDP and RCDN in half clock mode.
EOFD	TTL	O	U6	Channel D End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTD[0:7]. (See Table 7.)
KFLAGD	TTL	O	T7	Channel D K-Character Flag. A High in KFLAGD indicates that a valid control character has been detected. Data present on the parallel interface DOUTD[0:7] should be used to indicate which character was received. (See Table 7.)
ERRD	TTL	O	T6	Channel D Receive Error. A High on ERRD signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. (See Table 7.)
LOLD	TTL	O	C11	Channel D Loss of Lock Detected. LOLD High indicates that the CRU on channel D has lost bit lock. This signal will deassert when the CRU has locked to data. When in Channel Lock Mode, this signal will assert indicating that the channel D CRU is not bit locked. This will report asynchronously. (See Table 7.)
RCDP RCDN	TTL	O	T10 U10	Receive Data Clock for Channel D. Parallel receive data, DOUTD[0:7], EOFD, KFLAGD, and ERRD are valid on the rising edge of RCDP when in full clock mode and valid on the rising edge of both RCDP and RCDN in half clock mode.

Table 14. Receiver Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	A2 A3	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to V_{DD} -1.3 V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	A5 B5	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to V_{DD} -1.3 V for AC coupled applications.
RXCP RXCN	Diff. LVPECL	I	A8 A9	Differential LVPECL compatible inputs for channel C. RXCP is the positive input, RXCN is the negative. Internally biased to V_{DD} -1.3 V for AC coupled applications.
RXDP RXDN	Diff. LVPECL	I	B11 B12	Differential LVPECL compatible inputs for channel D. RXDP is the positive input, RXDN is the negative. Internally biased to V_{DD} -1.3 V for AC coupled applications.

Table 15. Receiver Control Signals

Pin Name	Level	I/O	Pin #	Description
LPENA LPENB LPENC LPEND	TTL	I	D14 G14 G15 H14	Loopback Enable. When Low, input source is the high speed serial input for each channel. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RCxP/N) rate is equal to 1/2 the data rate. When High, the parallel output clocks (RCxP/N) rate is equal to the data rate. When CMODE = 0 (data stretching enabled), the last EOF will always be clocked by RCxP, before non EOF.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 16. Power and Ground Signals

Pin Name	Qty.	Pin #	Description
VDDA	5	A1, A6, A13, A16 C8	Analog Power (V_{DD}) low noise.
VSSA	5	B7, B8, B15, C4, D11	Analog Ground (V_{SS}).
VDD	6	A12, A15, B4, B6, C6, D9	Power for High Speed Circuitry (V_{DD}).
VSS	5	A4, A11, B10, B14, D6	Ground for High Speed Circuitry (V_{SS}).
VSSSUB	5	A7, A14, C13, D5, D8	Ground for High Speed Circuitry (V_{SS}).
PECLPWR	4	D15, E15, E16, G16	PECL Power (V_{DD})
PECLGND	2	C16 H16	PECL Ground (V_{SS})
DIGPWR	6	B1, B2, E3, J17, L4, P9	Core Circuitry Power (V_{DD})
DIGGND	8	C1, C3, D2, F4, J15, N4, P10, R3	Core Circuitry Ground (V_{SS})
TTLPWR	7	E1, H4, K4, N3, P5, P7, P8	Power for TTL I/O (V_{DD})
TTLGND	10	D1, E2, F3, J4, L3, M4 P4, P6, R4, R8	Ground for TTL I/O (V_{SS})

Table 16. Power and Ground Signals (Continued)

Pin Name	Qty.	Pin #	Description
PWR	3	B13, B16, C12	Power
GND	1	D3	Ground
CAP1 CAP2	2	D13 C14	Loop Filter pins. The external loop filter capacitor and resistors are connected to these pins.
NC	2	B9, C7	Not Connected. Used as Test Pins. Do Not Connect.

Table 17. JTAG Test Signals

Pin Name	Level	I/O	Pin #	Description
TMS	TTL	I	A10	Test Mode Select. Enables JTAG testing of device.
TCK	TTL	I	C10	Test Clock. JTAG test clock.
TDI	TTL	I	D10	Test Data In. JTAG data input.
TDO	TTL	O TRISTATE	H15	Test Data Out. JTAG data output. Can be high impedance under JTAG controller command.
TRS	TTL	I	B3	Test Reset. Resets JTAG test state machine.

Figure 10. S2009 Pinout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	VDDA	DIGPWR	DIGGND	TTLGND	TTLPWR	DOUTA1	ERRA	DOUTA4	DOUTA7	RCAN	EOFB	DOUTB0	DOUTB2	DOUTB6	DOUTB7	RCBN	RCBP
2	RXAP	DIGPWR	CMODE	DIGGND	TTLGND	EOFA	DOUTA0	DOUTA3	DOUTA5	RCAP	DOUTB1	DOUTB3	DOUTB4	KFLAGB	EOFC	ERRC	DOUTC1
3	RXAN	TRS	DIGGND	GND	DIGPWR	TTLGND	KFLAGA	DOUTA2	DOUTA6	ERRB	TTLGND	DOUTB5	TTLPWR	KFLAGC	DIGGND	DOUTC0	DOUTC4
4	VSS	VDD	VSSA	SYNC	CH_LOCK	DIGGND	TCLKO2	TTLPWR	TTLGND	TTLPWR	DIGPWR	TTLGND	DIGGND	TTLGND	TTLGND	DOUTC3	RCCN
5	RXBP	RXBN	LOLA	VSSSUB										TTLPWR	DOUTC2	DOUTC5	RCCP
6	VDDA	VDD	VDD	VSS										TTLGND	DOUTC6	ERRD	EOFD
7	VSSSUB	VSSA	NC	LOLB										TTLPWR	DOUTC7	KFLAGD	DOUTD1
8	RXCP	VSSA	VDDA	VSSSUB										TTLPWR	TTLGND	DOUTD0	DOUTD2
9	RXCN	NC	LOLC	VDD										DIGPWR	DOUTD4	DOUTD3	DOUTD5
10	TMS	VSS	TCK	TDI										DIGGND	DOUTD6	RCDP	RCDN
11	VSS	RXDP	LOLD	VSSA										DINA2	DINA1	DINA0	DOUTD7
12	VDD	RXDN	PWR	RATE										DINA7	DINA6	DINA4	TCLKA
13	VDDA	PWR	VSSSUB	CAP1										DINB1	TCLKB	DINA5	DINA3
14	VSSSUB	VSS	CAP2	LPENA	SQLA_N	SQLC_N	LPENB	LPEND	TCLKO	DIND4	TCLKD	DINC5	DINC0	DINB6	DINB4	DINB0	KGENA
15	VDD	VSSA	RESET_N	PECL PWR	PECL PWR	SQLD_N	LPENC	TDO	DIGGND	DIND5	DIND0	DINC7	DINC2	TCLKC	DINB7	DINB5	DNA
16	VDDA	PWR	PECLGND	SQLB_N	PECL PWR	TXCN	PECL PWR	PECLGND	DND	DIND6	DIND2	DIND1	DINC6	DINC3	DNB	KGENB	DINB2
17	TXAP	TXAN	TXBP	TXBN	TXCP	TXDP	TXDN	REFCLK	DIGPWR	KGEND	DIND7	DIND3	DNC	KGENC	DINC4	DINC1	DINB3

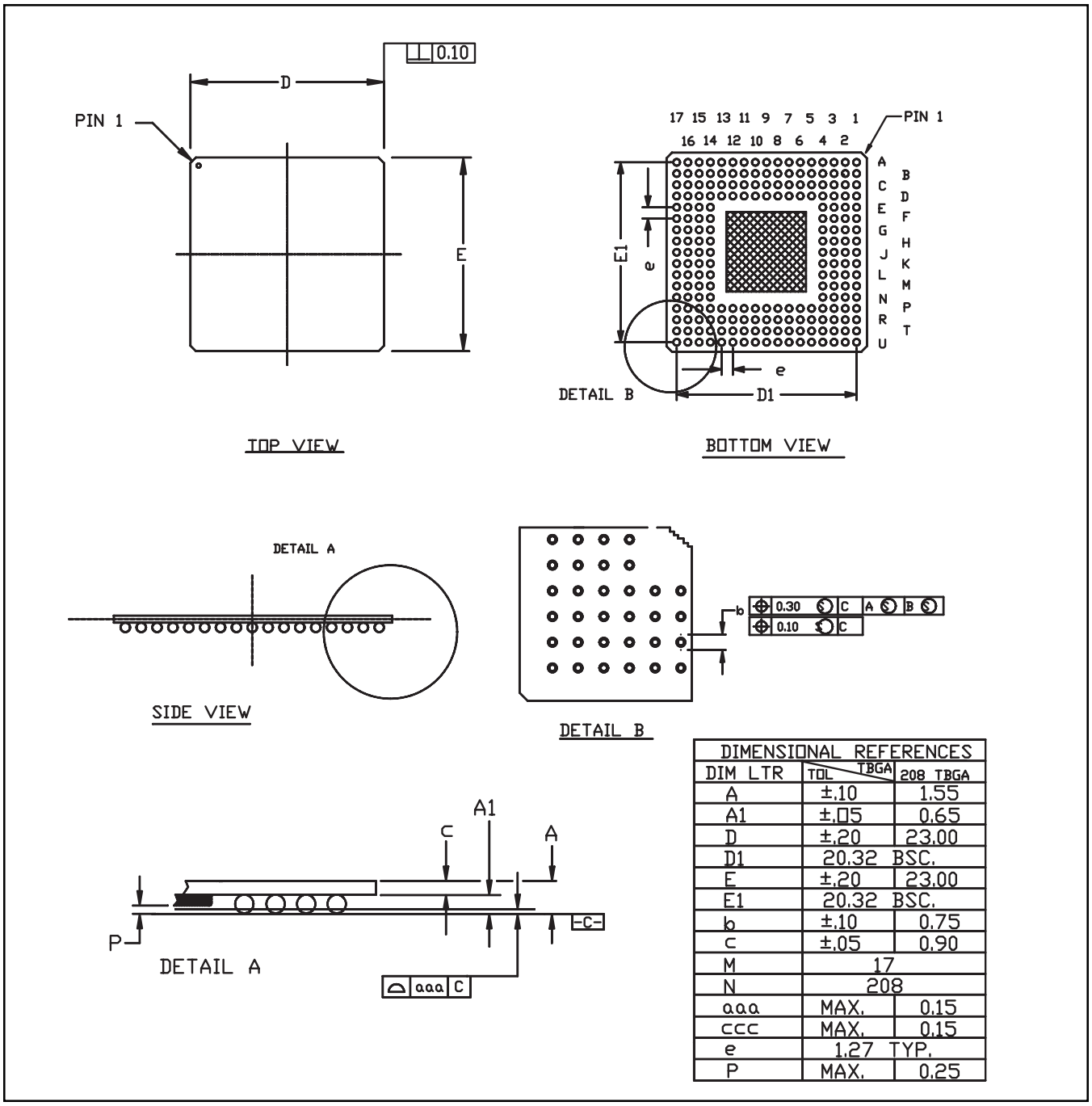
Note: NC used as Test Pins. Do Not Connect.

Figure 11. S2009 Pinout (Top View)

U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
RCBP	RCBN	DOUTB7	DOUTB6	DOUTB2	DOUTB0	EOFB	RCAN	DOUTA7	DOUTA4	ERRA	DOUTA1	TTLPWR	TTLGND	DIGGND	DIGPWR	VDDA	1
DOUTC1	ERRC	EOFC	KFLAGB	DOUTB4	DOUTB3	DOUTB1	RCAP	DOUTA5	DOUTA3	DOUTA0	EOFA	TTLGND	DIGGND	CMODE	DIGPWR	RXAP	2
DOUTC4	DOUTC0	DIGGND	KFLAGC	TTLPWR	DOUTB5	TTLGND	ERRB	DOUTA6	DOUTA2	KFLAGA	TTLGND	DIGPWR	GND	DIGGND	TRS	RXAN	3
RCCN	DOUTC3	TTLGND	TTLGND	DIGGND	TTLGND	DIGPWR	TTLPWR	TTLGND	TTLPWR	TCLKO2	DIGGND	CH_LOCK	SYNC	VSSA	VDD	VSS	4
RCCP	DOUTC5	DOUTC2	TTLPWR										VSSSUB	LOLA	RXBN	RXBP	5
EOFD	ERRD	DOUTC6	TTLGND										VSS	VDD	VDD	VDDA	6
DOUTD1	KFLAGD	DOUTC7	TTLPWR										LOLB	NC	VSSA	VSSSUB	7
DOUTD2	DOUTD0	TTLGND	TTLPWR										VSSSUB	VDDA	VSSA	RXCP	8
DOUTD5	DOUTD3	DOUTD4	DIGPWR										VDD	LOLC	NC	RXCN	9
RCDN	RCDP	DOUTD6	DIGGND										TDI	TCK	VSS	TMS	10
DOUTD7	DINA0	DINA1	DINA2										VSSA	LOLD	RXDP	VSS	11
TCLKA	DINA4	DINA6	DINA7										RATE	PWR	RXDN	VDD	12
DINA3	DINA5	TCLKB	DINB1										CAP1	VSSSUB	PWR	VDDA	13
KGENA	DINB0	DINB4	DINB6	DINC0	DINC5	TCLKD	DIND4	TCLKO	LPEND	LPENB	SQLC_N	SQLA_N	LPENA	CAP2	VSS	VSSSUB	14
DNA	DINB5	DINB7	TCLKC	DINC2	DINC7	DIND0	DIND5	DIGGND	TDO	LPENC	SQLD_N	PECL PWR	PECL PWR	RESET_N	VSSA	VDD	15
DINB2	KGENB	DNB	DINC3	DINC6	DIND1	DIND2	DIND6	DND	PECLGND	PECL PWR	TXCN	PECL PWR	SQLB_N	PECLGND	PWR	VDDA	16
DINB3	DINC1	DINC4	KGENC	DNC	DIND3	DIND7	KGEND	DIGPWR	REFCLK	TXDN	TXDP	TXCP	TXBN	TXBP	TXAN	TXAP	17

Note: NC used as Test Pins. Do Not Connect.

Figure 12. Compact 23 mm x 23 mm 208 Pin TBGA Package



DIMENSIONAL REFERENCES		
DIM LTR	TOL / TBGA	208 TBGA
A	±.10	1.55
A1	±.05	0.65
D	±.20	23.00
D1	20.32 BSC.	
E	±.20	23.00
E1	20.32 BSC.	
b	±.10	0.75
c	±.05	0.90
M	17	
N	208	
aaa	MAX.	0.15
ccc	MAX.	0.15
e	1.27 TYP.	
P	MAX.	0.25

Thermal Management

Max Package Power	Airflow	Θja	Θjc
4.64 W	200 LFPM	12.9 ˚ C/W	3.0 ˚ C/W

Note: The S2009 requires an airflow of 200 Linear Feet Per Minute (LFPM) for proper thermal management. Θja value corresponds to a 200 LFPM environment.

Figure 13. Transmitter Timing (Independent or Channel Lock Mode)

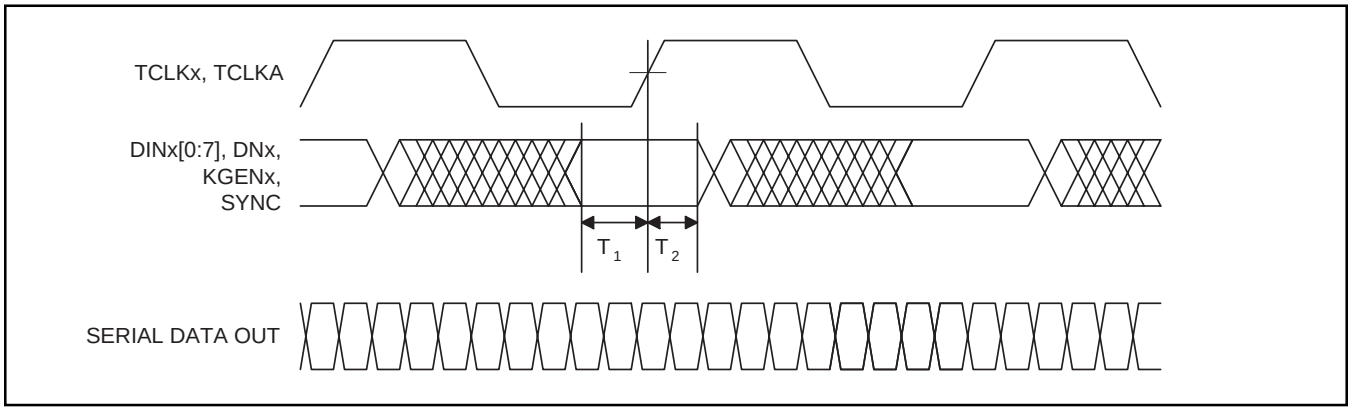


Table 18. S2009 Transmitter Timing (Independent or Channel Lock Mode)

Parameter	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑TCLK	750	-	ps	See Note 1.
T_2	Data Hold w.r.t. ↑TCLK	325	-	ps	
	Phase drift between TCLKx and REFCLK	-3	+3	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4 V) to the valid input or output data levels (0.8 V or 2.0 V).

Table 19. S2009 TCLKO, TCLKO2, and TCLKx Performance Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
$T_{JITTERT}$	Edge to Edge TCLKO Jitter			130	ps	Peak to peak.
T_R , T_F	TCLKO Rise and Fall Times			1.4	ns	See Note 2. See Figure 19.
$T_{JITTERT2}$	Edge to Edge TCLKO2 Jitter			156	ps	Peak to peak.
T_R , T_F	TCLKO2 Rise and Fall Times			1.5	ns	See Note 2. See Figure 19.
$T_{TC2\ to\ TC}$	TCLKO2 to TCLKO Skew	1		2.8	ns	TCLKO2 leads TCLKO, rising edge to rising edge.
Slew Rate	Input Slew Rate			2	ns	See note 1.
Duty Cycle	TCLKO, TCLKO2 Duty Cycle	40		60	%	See note 1.
Duty Cycle	TCLKx Input Duty Cycle	35		65	%	See note 1.

1. Unless otherwise specified, all AC measurements are made from the reference voltage levels of the clock (1.4 V) to the valid input or output data levels (0.8 V or 2.0 V).
2. TTL/CMOS AC timing measurements are assumed to have an output load of 10 pF.

Table 20. S2009 Receiver Timing (Full and Half Clock Mode)

Parameter	Description	Min	Max	Units	Conditions
T_3	Data Setup w.r.t. ↑RCxP/N	2.5 1.5		ns ns	1.3 Gbps 1.5552 Gbps
T_4	Data Hold w.r.t. ↑RCxP/N	1.5		ns	
T_5	Data Setup w.r.t. ↑RCxP/N	2.5 1.0		ns	at 1.3 Gbps at 1.5552 Gbps[1,2]
T_6	Data Hold w.r.t. ↑RCxP/N	1.0		ns	
T_7	Time from RCxP rise to RCxN rise	7.5 5.8	8.5 7.8	ns ns	at 1.3 Gbps at 1.5552 Gbps[1,2]
T_{RP}, T_{FP}	RCxP Rise and Fall Times		900	ps	See note 2. See Figure 19.
T_{RN}, T_{FN}	RCxN Rise and Fall Times		900	ps	See note 2. See Figure 19.
T_{DR}, T_{DF}	DOUTx Rise and Fall Times		2.4	ns	See note 2. See Figure 19.
Duty Cycle	RCxP/N Duty Cycle	40	60	%	See note 1.

1. Measurements made from the reference voltage levels of the clock (1.4 V) to the valid input or output data levels (0.8 V or 2.0 V).
2. TTL/CMOS AC timing measurements are assumed to have an output load of 10 pF.

Figure 14. Receiver Timing (Full Clock Mode, CMODE = 1)

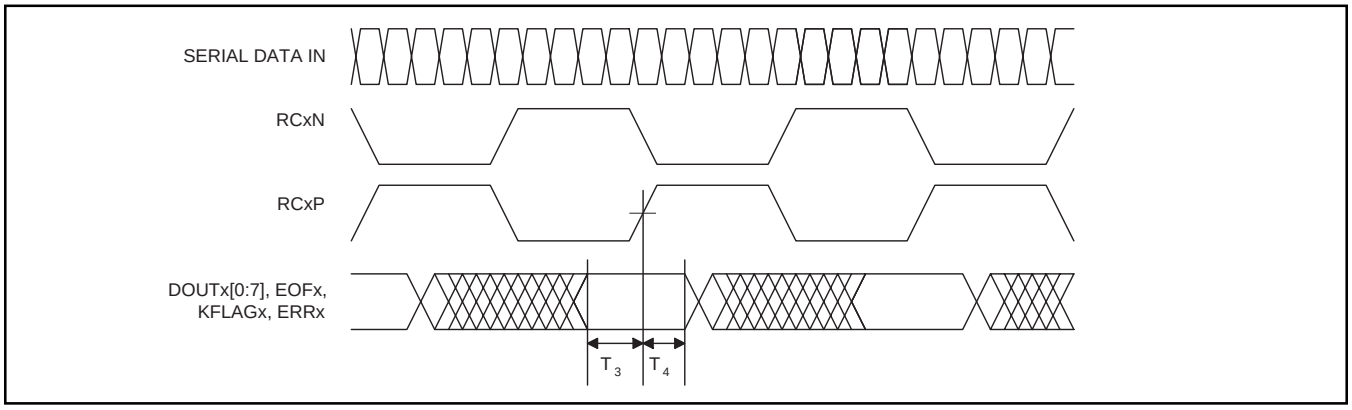


Figure 15. Receiver Timing (Half Clock Mode, CMODE = 0)

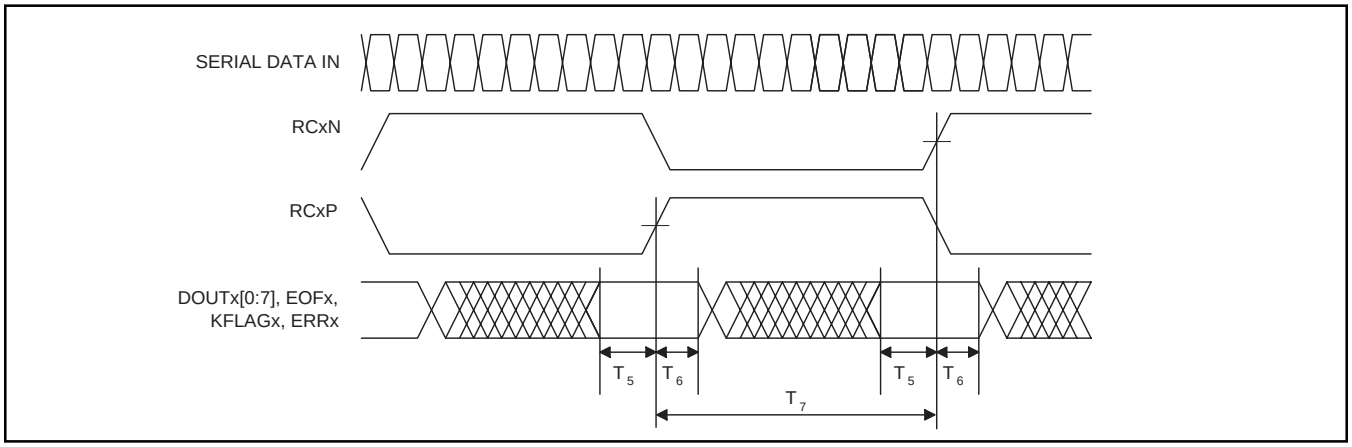


Table 21. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on VDD with Respect to GND	-0.5		+5.1	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any PECL Input Pin	0		V_{DD}	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			25	mA
ESD Sensitivity[1] (All pins)	Over 200 V			

1. Human Body Model.

Table 22. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on any Power Pin with respect to GND/V_{SS}	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	V_{DD}-2		V_{DD}	V

Table 23. Reference Clock Requirements

Parameter	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	| REFCLK frequency – data rate/20 | < 200
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
—	Jitter		80	ps	Peak-to-Peak, to maintain ≥ 77% eye opening.

Table 24. Serial Data Timing, Transmit Outputs[1]

Parameter	Description	Min	Typ	Max	Units	Comments
Total Jitter	Serial Data Output Total Jitter			145	ps	Peak-to-Peak.
T_{DJ}	Serial Data Output Deterministic Jitter		16	40	ps	Peak-to-Peak.
T_{SR}, T_{SF}	Serial Data Output Rise and Fall Time			275	ps	20% - 80%.

1. Output loading is 100 Ω line-to-line.

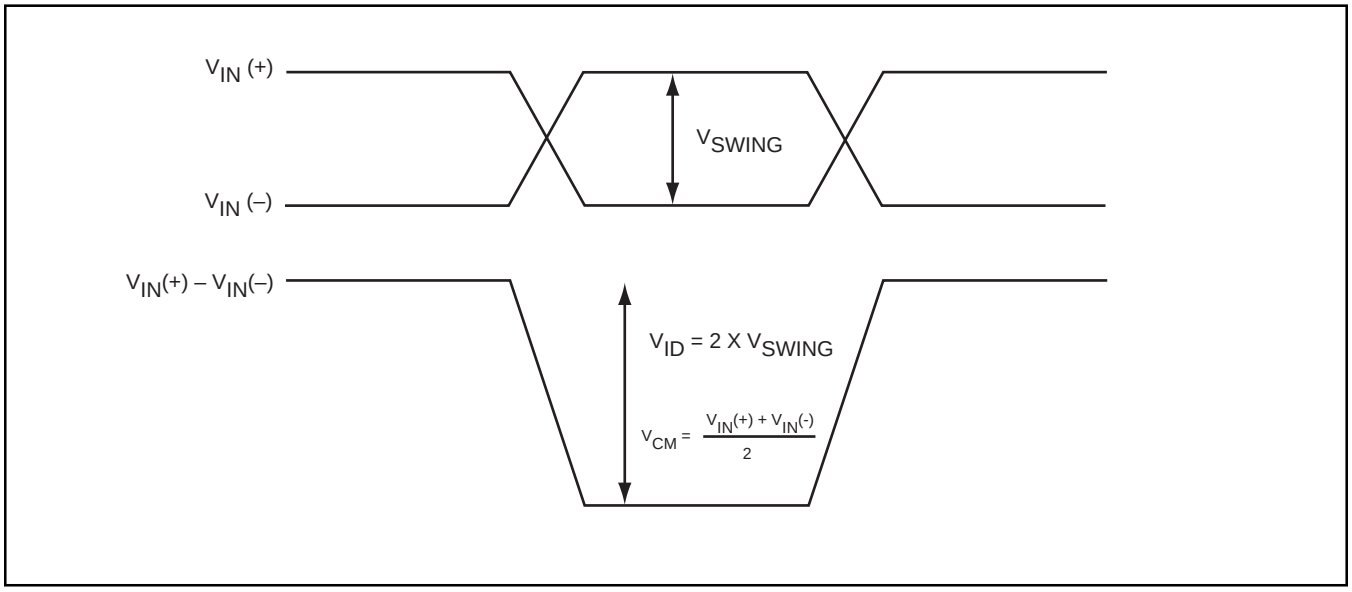
Table 25. Serial Data Timing, Receive Inputs

Parameter	Description	Min	Typ	Max	Units	Comments
T_{LOCK} (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.5552 Gbps)			175	µs	8B/10B idle pattern sample basis, from device start up.
T_{LOCK} (Phase)	Phase Acquisition Lock Time (Phase Discontinuity) (1.5552 Gbps)			150	ns	90% input data eye (see Figure 23).
				180	ns	70% input data eye.
T_{DJ}	Deterministic Input Jitter Tolerance	280			ps	
Input Jitter Tolerance	Serial Data Input Total Jitter Tolerance	462			ps	
R_{SR}, R_{SF}	Serial Data Input Rise and Fall Time			330	ps	20% - 80%.

Table 26. DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.4	2.8	V_{DD}	V	Max I_{OH} = 8 mA, Typ I_{OH} = 12 mA
V_{OL}	Output Low Voltage (TTL)	GND	0.025	0.5	V	Min I_{OL} = –8 mA, Typ I_{OL} = –12 mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4 V, V_{DD} = Max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = 0.8 V, V_{DD} = Max
I_{DD}	Supply Current		800	990	mA	1010 Pattern.
P_D	Power Dissipation		2.65	3.5	W	1010 Pattern.
C_{IN}	Input Capacitance			3	pF	

Figure 16. Differential Input Voltage



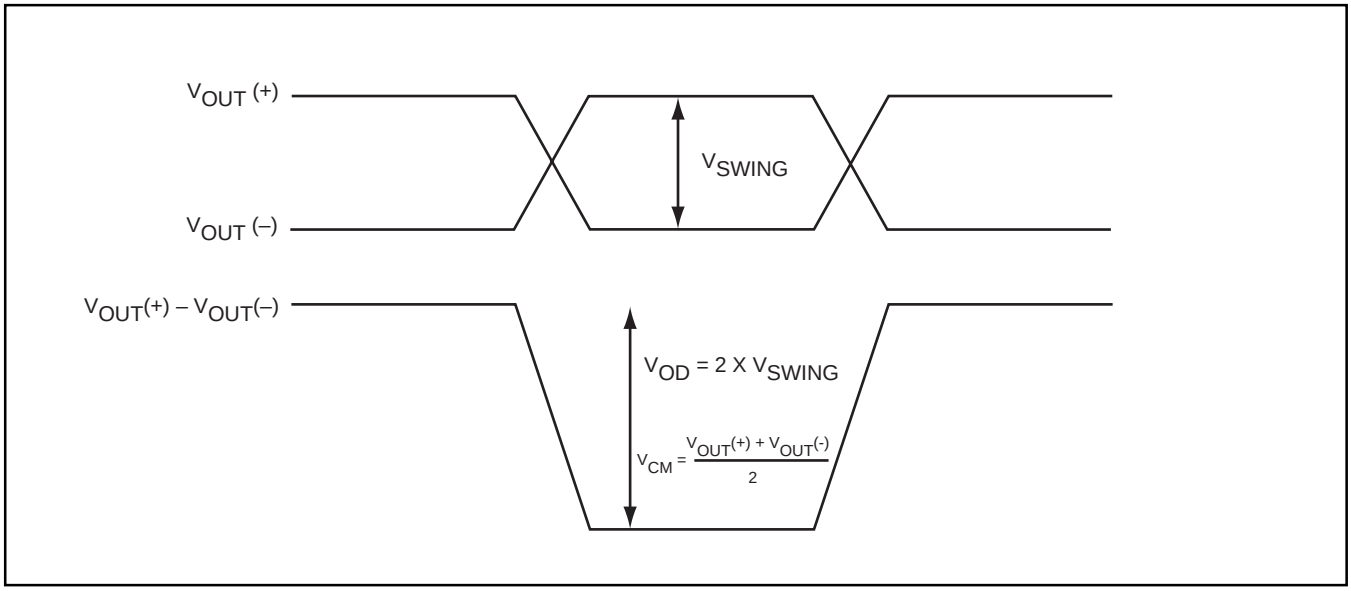
(Note: $V_{IN}(+) – V_{IN}(-)$ is the algebraic difference of the input signals.)

Table 27. Differential LVPECL Characteristics

Symbol	Min	Typ	Max	Units	Conditions
V_{ID} [1]	100	400	2600	mV	See Figure 16 and Figure 21.
V_{CM} [2]		V_{DD}–1.3		V	See Figure 16.

1. Differential input voltage.
2. Common mode range.

Figure 17. Differential Output Voltage



(Note: $V_{OUT}(+) – V_{OUT}(-)$ is the algebraic difference of the input signals.)

Table 28. Differential LVPECL Characteristics

Symbol	Min	Typ	Max	Units	Conditions
V_{OD} [1]	1400	1600	2600	mV	See Figure 17 and Figure 20.
V_{CM} [2]		V_{DD}–2.3		V	See Figure 17.

1. Differential output voltage.
2. Common mode range.

OUTPUT LOAD

The S2009 serial outputs do not require output pulldown resistors.

ACQUISITION TIME

With the input eye diagram shown in Figure 23, the S2009 will recover data with a ≤1E-9 BER within the time specified by T_{LOCK} in Table 25 after an instantaneous phase shift of the incoming data.

Figure 18. Serial Input/Output Rise and Fall Time

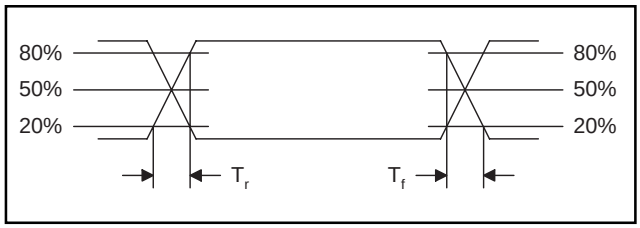


Figure 19. TTL Input/Output Rise and Fall Time

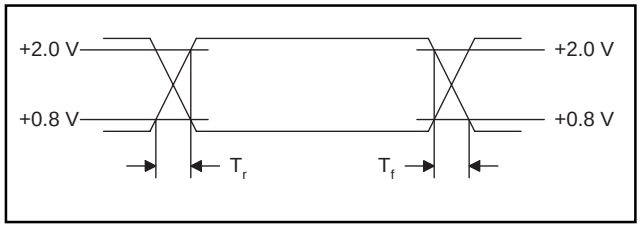


Figure 20. Serial Output Load

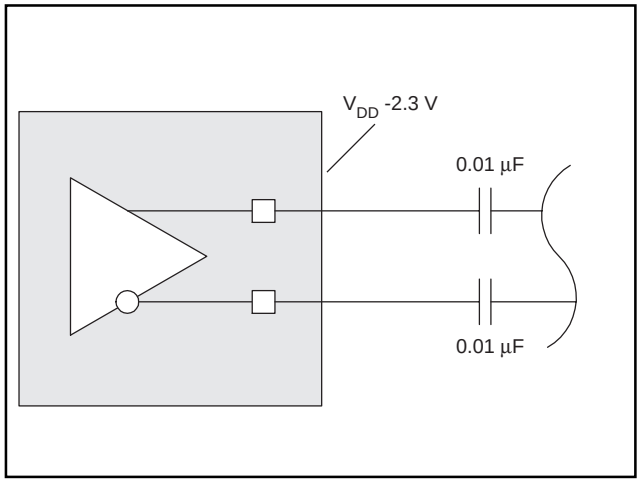


Figure 21. High Speed Differential Inputs

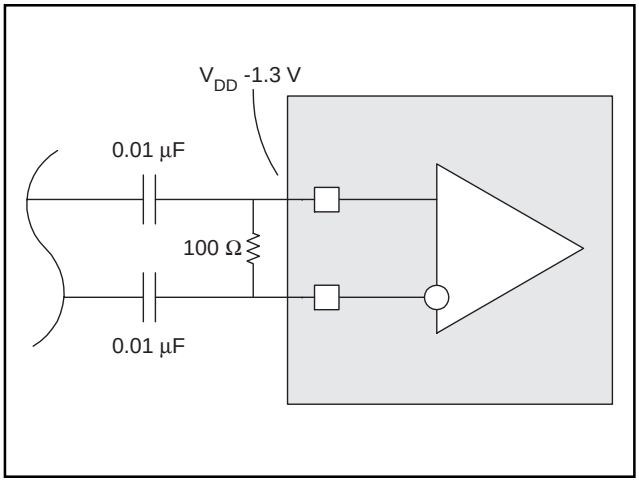


Figure 22. Receiver Input Eye Diagram Jitter Mask

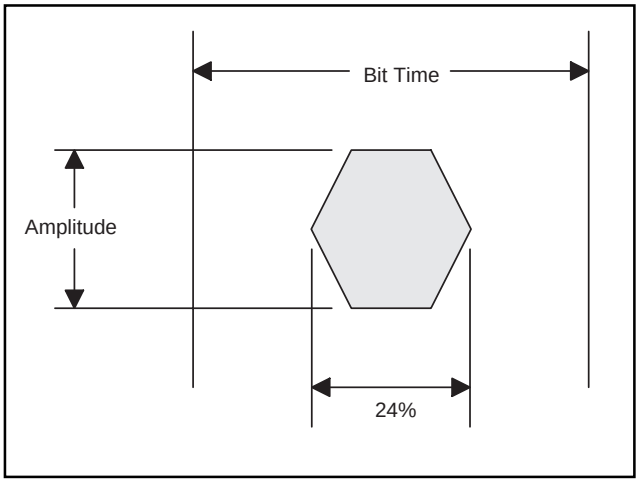


Figure 23. Acquisition Time Eye Diagram

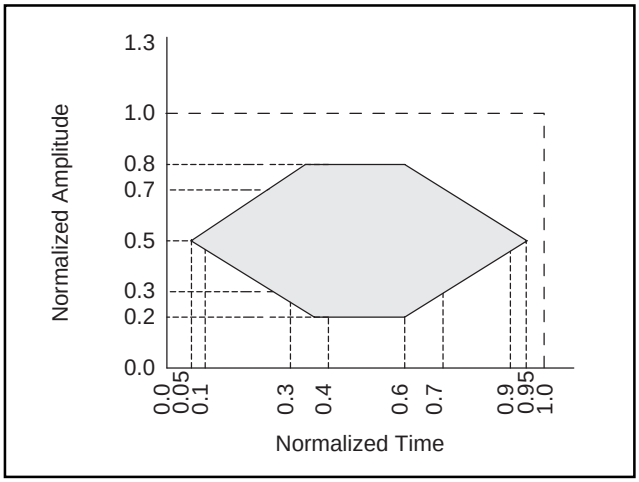
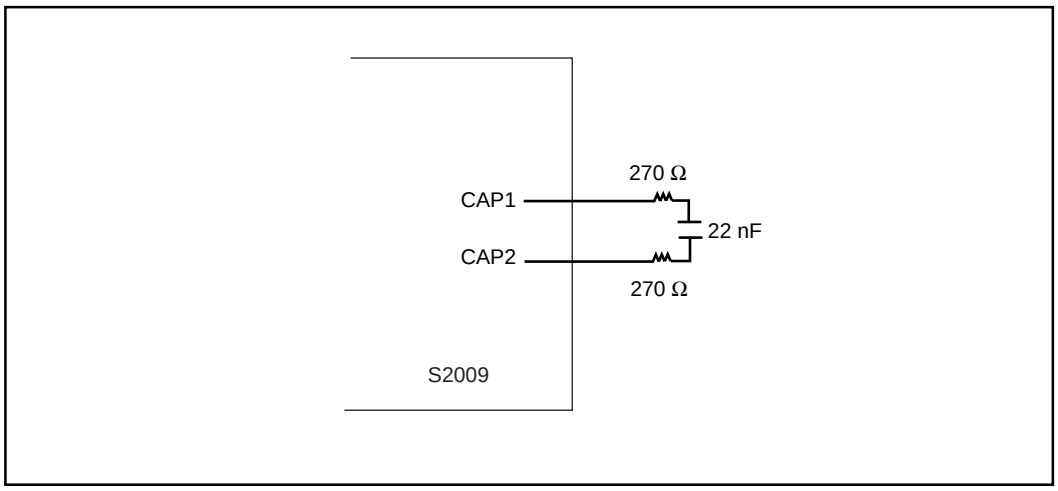
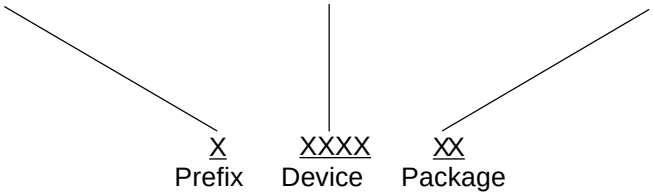


Figure 24. Loop Filter Capacitor Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	2009	TB – 208 TBGA



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