

# CD74HC4066, CD74HCT4066

## High-Speed CMOS Logic Quad Bilateral Switch

### Features

- **Wide Analog-Input-Voltage Range** . . . . . 0V - 10V
- **Low "ON" Resistance**
  - $V_{CC} = 4.5V$  . . . . .  $25\Omega$
  - $V_{CC} = 9V$  . . . . .  $15\Omega$
- **Fast Switching and Propagation Delay Times**
- **Low "OFF" Leakage Current**
- **Wide Operating Temperature Range** . . . -55°C to 125°C
- **HC Types**
  - 2V to 10V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$  and 10V
- **HCT Types**
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC4066 and CD74HCT4066 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear "ON" resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

### Ordering Information

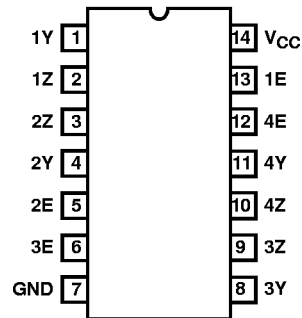
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC4066E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT4066E	-55 to 125	14 Ld PDIP	E14.3
CD74HC4066M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT4066M	-55 to 125	14 Ld SOIC	M14.15

#### NOTES:

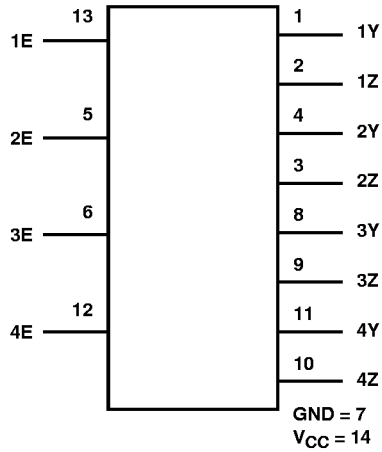
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout

CD74HC4066, CD74HCT4066  
(PDIP, SOIC)  
TOP VIEW



**Functional Diagram**

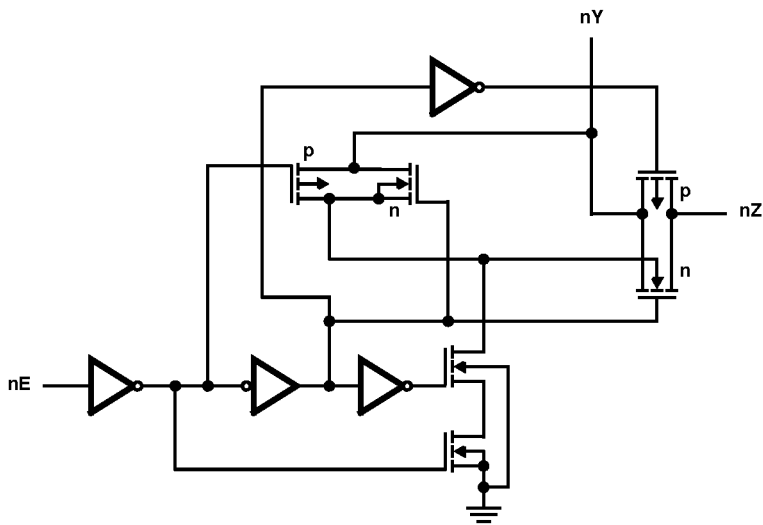


TRUTH TABLE

INPUT nE	SWITCH
L	Off
H	On

NOTE:  
 H = High Level  
 L = Low Level

**Logic Diagram**



# CD74HC4066, CD74HCT4066

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$	
HCT Types	-0.5V to 7V
HC Types	-0.5V to 10.5V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Switch Current, $I_O$ (Note 3)	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	90
SOIC Package	175
Maximum Junction Temperature (Hermetic Package or Die)	175 $^{\circ}C$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range, $T_A$	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types	.2V to 10V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$	0V to $V_{CC}$
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTES:

- In certain applications, the external load-resistor current may include both  $V_{CC}$  and signal-line components. To avoid drawing  $V_{CC}$  current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from  $R_{ON}$  values shown in the DC Electrical Specifications Table). No  $V_{CC}$  current will flow through  $R_L$  if the switch current flows into terminals 2, 3, 9 and 10.
- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$V_{IS}$ (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				9	6.3	-	-	6.3	-	6.3	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				9	-	-	2.7	-	2.7	-	2.7	V
Input Leakage Current (Any Control)	$I_{IL}$	$V_{CC}$ or GND	-	10	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Off-Switch Leakage Current	$I_Z$	$V_{IL}$	$V_{CC}$ or GND	10	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

**CD74HC4066, CD74HCT4066**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	V <sub>IS</sub> (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
"ON" Resistance I <sub>O</sub> = 1mA (Figure 1)	R <sub>ON</sub>	V <sub>CC</sub>	V <sub>CC</sub> or GND	4.5	-	25	80	-	106	-	128	Ω
				6	-	20	75	-	94	-	113	Ω
				9	-	15	60	-	78	-	95	Ω
		V <sub>CC</sub> to GND	4.5	-	35	95	-	118	-	142	Ω	
			6	-	24	84	-	105	-	126	Ω	
			9	-	16	70	-	88	-	105	Ω	
"ON" Resistance Between Any Two Switches	ΔR <sub>ON</sub>	V <sub>CC</sub>	-	4.5	-	1	-	-	-	-	-	Ω
				6	-	0.75	-	-	-	-	-	Ω
				9	-	0.5	-	-	-	-	-	Ω
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	-	6	-	-	2	-	20	-	40	μA
				10	-	-	16	-	160	-	320	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
Input Leakage Current (Any Control)	I <sub>IL</sub>	V <sub>CC</sub> or GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Off-Switch Leakage Current	I <sub>Z</sub>	V <sub>IL</sub>	V <sub>CC</sub> or GND	5.5	-	-	±0.1	-	±1	-	±1	μA
"ON" Resistance I <sub>O</sub> = 1mA (Figure 1)	R <sub>ON</sub>	V <sub>CC</sub>	V <sub>CC</sub> or GND	4.5	-	25	80	-	106	-	128	Ω
			V <sub>CC</sub> to GND	4.5	-	35	95	-	118	-	142	Ω
"ON" Resistance Between Any Two Switches	ΔR <sub>ON</sub>	V <sub>CC</sub>	-	4.5	-	1	-	-	-	-	-	Ω
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	-	5.5	-	-	2	-	20	-	40	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 5)	ΔI <sub>CC</sub>	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

5. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
All	1

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

## CD74HC4066, CD74HCT4066

### Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Time Switch In to Out	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			9	-	-	8	-	11	-	13	ns
		$C_L = 15\text{pF}$	5	-	4	-	-	-	-	-	ns
Propagation Delay Time Switch Turn On Delay	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	2	-	-	100	-	125	-	150	ns
			4.5	-	-	20	-	25	-	30	ns
			9	-	-	12	-	15	-	18	ns
		$C_L = 15\text{pF}$	5	-	8	-	-	-	-	-	ns
Propagation Delay Time Switch Turn Off Delay	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
			9	-	-	24	-	30	-	36	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
Input (Control) Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	-	25	-	-	-	-	pF	
<b>HCT TYPES</b>											
Propagation Delay Time Switch In to Out	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	12	-	15	-	18	ns
		$C_L = 15\text{pF}$	5	-	4	-	-	-	-	-	ns
Propagation Delay Time Switch Turn On Delay	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	4.5	-	-	24	-	30	-	36	ns
		$C_L = 15\text{pF}$	5	-	9	-	-	-	-	-	ns
Propagation Delay Time Switch Turn Off Delay	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Input (Control) Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	-	38	-	-	-	-	pF	

**NOTES:**

6.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
7.  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $C_S$  = switch capacitance,  $V_{CC}$  = supply voltage.

### Analog Channel Specifications $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$ (V)	CD74HC4066	CD74HCT4066	UNITS
Switch Frequency Response Bandwidth at -3dB Figure 2	Figure 5, Notes 8, 9	4.5	200	200	MHz
Cross Talk Between Any Two Switches Figure 3	Figure 4, Notes 9, 10	4.5	-72	-72	dB
Total Harmonic Distortion	Figure 6, 1kHz, $V_{IS} = 4V_{P-P}$	4.5	0.022	0.023	%
	Figure 6, 1kHz, $V_{IS} = 8V_{P-P}$	9	0.008	N/A	%

# CD74HC4066, CD74HCT4066

## Analog Channel Specifications $T_A = 25^\circ\text{C}$ (Continued)

PARAMETER	TEST CONDITIONS	$V_{CC}$ (V)	CD74HC4066	CD74HCT4066	UNITS
Control to Switch Feedthrough Noise	Figure 7	4.5	200	130	mV
		9	550	N/A	mV
Switch "OFF" Signal Feedthrough Figure 3	Figure 8, Notes 9, 10	4.5	-72	-72	dB
Switch Input Capacitance, $C_S$		-	5	5	pF

NOTES:

8. Adjust input level for 0dBm at output,  $f = 1\text{MHz}$ .
9.  $V_{IS}$  is centered at  $V_{CC}/2$ .
10. Adjust input for 0dBm at  $V_{IS}$ .

## Typical Performance Curves

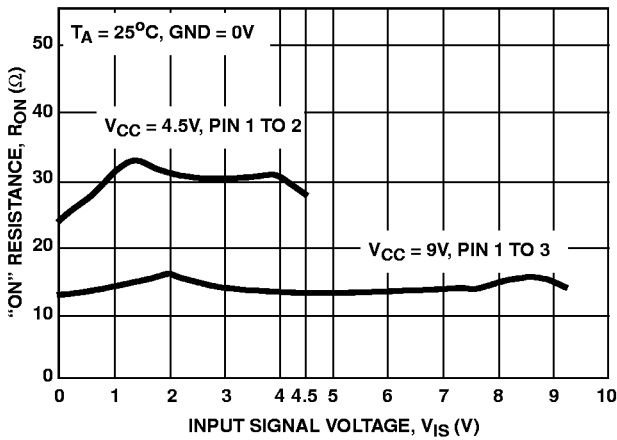


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

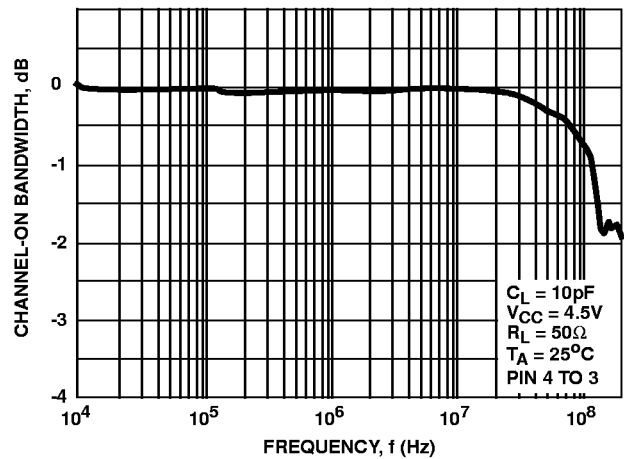


FIGURE 2. SWITCH FREQUENCY RESPONSE,  $V_{CC} = 4.5\text{V}$

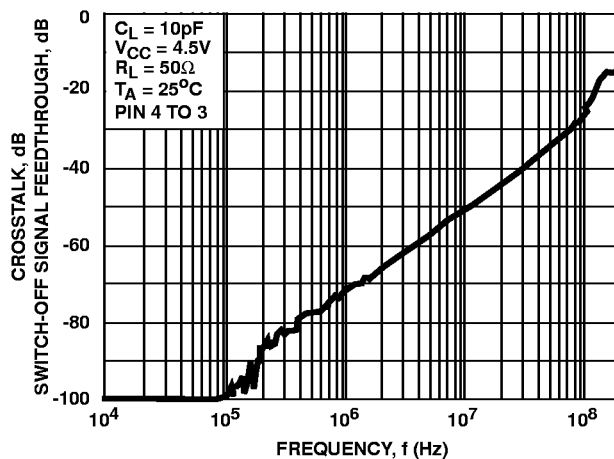


FIGURE 3. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY,  $V_{CC} = 4.5\text{V}$

Analog Test Circuits

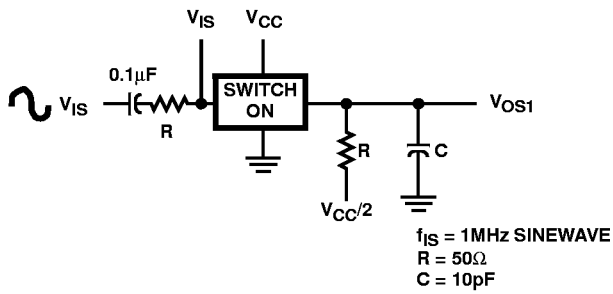


FIGURE 4. CROSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

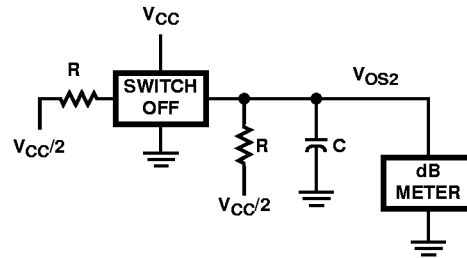


FIGURE 5. FREQUENCY RESPONSE TEST CIRCUIT

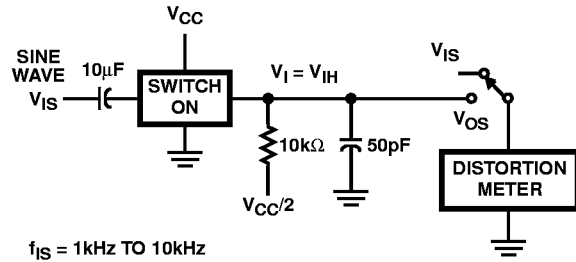


FIGURE 6. TOTAL HARMONIC DISTORTION TEST CIRCUIT

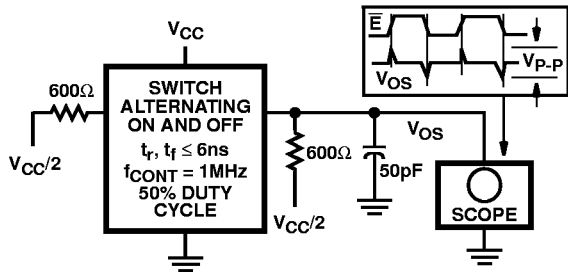


FIGURE 7. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

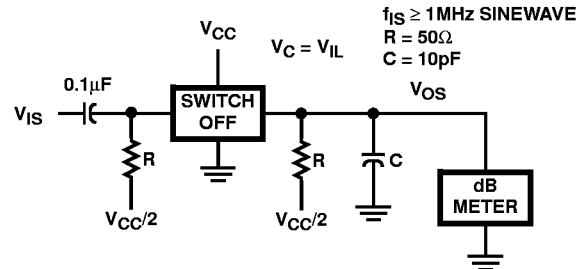


FIGURE 8. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms

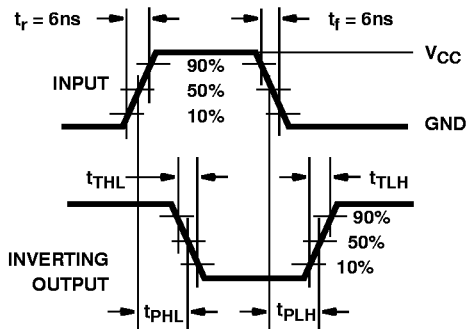


FIGURE 9. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

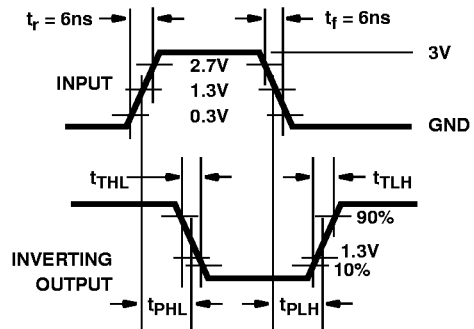


FIGURE 10. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC