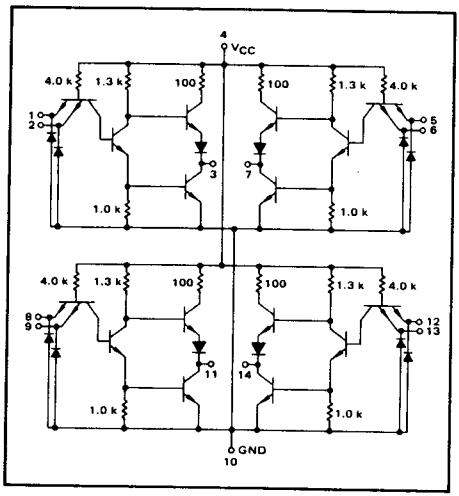
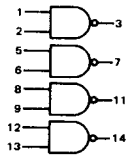
# MC508 · MC558
# MC408 · MC458




This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.

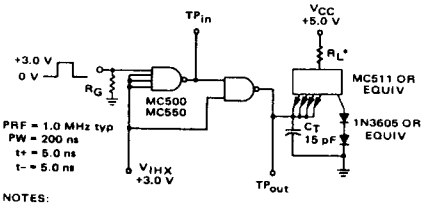



Positive Logic: $3 = \overline{1 \cdot 2}$
Negetive Logic: $3 = \overline{1 + 2}$

Total Power Dissipation = 60 mW typ/pkg
Propegation Delay Time = 10 ns typ

| TYPE NO. | INPUT LOADING FACTOR | ($I_F$) | OUTPUT DRIVE | | ($I_{OL}$) | TEMPERATURE RANGE |
|---|---|---|---|---|---|---|
| MC508<br>MC558 | 1 | (−1.33 mA) | 15<br>7 | MC500 series Gates<br>MC500 series Gates | (20 mA)<br>(10 mA) | −55°C to +125°C |
| MC408<br>MC458 | 1 | (−1.66 mA) | 12<br>6 | MC400 series Gates<br>MC400 series Gates | (20 mA)<br>(10 mA) | 0° to +75°C |

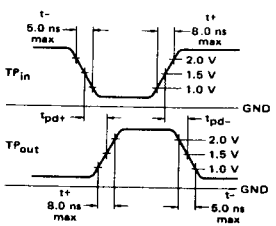
## SWITCHING TIME TEST CIRCUIT




NOTES:
$R_G$ = 50 ohms
$C_T$ = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

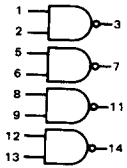
*MC508 – 260Ω
MC558 – 570Ω
MC408 – 330Ω
MC458 – 660Ω

## VOLTAGE WAVEFORMS AND DEFINITIONS



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.




| @ Test Temperature | | $I_{OL}$ mA Pr* | $I_{OL}$ mA Std | $I_{OH}$ mA Pr* | $I_{OH}$ mA Std | $I_{in}$ mA | $V_{IL}$ Volts | $V_{IH}$ Volts | $V_R$ Volts | $V_{th\,1}$ Volts | $V_{th\,0}$ Volts | $V_{out}$ Volts | $V_{CC}$ Volts | $V_{CCH}$ Volts | $V_{IHX}$ Volts |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MC508*, MC558 | −55°C | 20 | 10 | -1.5 | -0.7 | 1.0 | 0.45 | 2.8 | 4.5 | 2.0 | 1.0 | 5.5 | 5.0 | - | - |
| | +25°C | 20 | 10 | -1.5 | -0.7 | 1.0 | 0.45 | 2.8 | 4.5 | 1.7 | 1.2 | 5.5 | 5.0 | 8.0 | 3.0 |
| | +125°C | 20 | 10 | -1.5 | -0.7 | 1.0 | 0.45 | 2.8 | 4.5 | 1.4 | 0.9 | 5.5 | 5.0 | - | - |
| MC408*, MC458 | 0°C | 20 | 10 | -1.2 | -0.6 | 1.0 | 0.45 | 3.0 | 4.5 | 1.9 | 1.1 | 5.5 | 5.0 | - | - |
| | +25°C | 20 | 10 | -1.2 | -0.6 | 1.0 | 0.45 | 3.0 | 4.5 | 1.8 | 1.2 | 5.5 | 5.0 | 7.0 | 3.0 |
| | +75°C | 20 | 10 | -1.2 | -0.6 | 1.0 | 0.45 | 3.0 | 4.5 | 1.7 | 1.1 | 5.5 | 5.0 | - | - |

| Characteristic | Symbol | Pin Under Test | MC508, MC558 Test Limits −55°C Min | −55°C Max | +25°C Min | +25°C Max | +125°C Min | +125°C Max | MC408, MC458 Test Limits 0°C Min | 0°C Max | +25°C Min | +25°C Max | +75°C Min | +75°C Max | Unit | TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL}$ | $I_{OH}$ | $I_{in}$ | $V_{IL}$ | $V_{IH}$ | $V_R$ | $V_{th\,1}$ | $V_{th\,0}$ | $V_{out}$ | $V_{CC}$ | $V_{CCH}$ | $V_{IHX}$ | Gnd† |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Forward Current | $I_F$ | 1 | - | -1.33 | - | -1.33 | - | -1.33 | - | -1.66 | - | -1.66 | - | -1.66 | mAdc | - | - | - | - | - | 2 | - | - | - | 4 | - | - | 1,10 |
| Leakage Current | $I_R$ | 1 | - | 100 | - | 100 | - | 100 | - | 100 | - | 100 | - | 100 | μAdc | - | - | - | - | - | 1 | - | - | - | 4 | - | - | 2,10 |
| Inverse Beta Current | $I_L$ | 1 | - | 100 | - | 100 | - | 100 | - | 100 | - | 100 | - | 100 | μAdc | - | - | - | - | - | 1 | - | - | - | 4 | - | - | 2,10 |
| Breakdown Voltage | $BV_{in}$ "0" | 1 | 5.5 | - | 5.5 | - | 5.5 | - | 5.5 | - | 5.5 | - | 5.5 | - | Vdc | - | - | 1 | - | - | - | - | - | - | 4 | - | - | 10 |
| | $BV_{in}$ "1" | 1 | 5.5 | - | 5.5 | - | 5.5 | - | 5.5 | - | 5.5 | - | 5.5 | - | Vdc | - | - | 1 | - | - | - | - | - | - | 4 | - | - | 2,10 |
| **Output** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Output Voltage | $V_{out}$ "0" | 3 | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | Vdc | 3 | - | - | - | - | - | 1 | - | - | 4 | - | - | 10 |
| | $V_{out}$ "1" | 3 | 2.5 | - | 2.4 | - | 2.7 | - | 2.5 | - | 2.4 | - | 2.5 | - | Vdc | - | 3 | - | - | - | - | - | 1 | - | 4 | - | - | 10 |
| Leakage Current | $I_{OLK}$ | 3 | - | 250 | - | 250 | - | 250 | - | 250 | - | 250 | - | 250 | μAdc | - | - | - | - | - | - | - | - | 3 | 4 | - | - | 1,2,10 |
| Short-Circuit Current | $I_{SC}$ | 3 | -10 | -45 | -10 | -45 | -10 | -45 | -10 | -45 | -10 | -45 | -10 | -45 | mAdc | - | - | - | - | - | - | - | - | - | 4 | - | - | 1,2,3,10 |
| Output Voltage | $V_{OL}$ | 3 | - | 0.40 | - | 0.40 | - | 0.45 | - | 0.40 | - | 0.40 | - | 0.45 | Vdc | 3 | - | - | - | 1 | - | - | - | - | 4 | - | - | 10 |
| | $V_{OH}$ | 3 | 2.8 | - | 3.2 | - | 3.35 | - | 3.0 | - | 3.1 | - | 3.15 | - | Vdc | - | 3 | - | 1 | - | - | - | - | - | 4 | - | - | 10 |
| **Power Requirements (Total Device)** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Maximum Power Supply Current | $I_{max}$ | 4 | - | - | - | 20 | - | - | - | - | - | 20 | - | - | mAdc | - | - | - | - | - | - | - | - | - | - | 4 | - | 1,5,8,10,12 |
| Power Supply Drain | $I_{PDH}$ | 4 | - | 24 | - | 24 | - | 24 | - | 30 | - | 30 | - | 30 | mAdc | - | - | - | - | - | - | - | - | - | 4 | - | - | 10‡ |
| | $I_{PDL}$ | 4 | - | 12 | - | 12 | - | 12 | - | 12 | - | 12 | - | 12 | mAdc | - | - | - | - | - | - | - | - | - | 4 | - | - | 1,5,8,10,12 |
| **Switching Parameters** | | | | | | | | | | | | | | | | Pulse In | Pulse Out | | | | | | | | | | | |
| Turn-On Delay | $t_{pd-}$ | 1,3 | - | - | - | 20 | - | - | - | - | - | 20 | - | - | ns | 1 | 3 | - | - | - | - | - | - | - | 4 | - | 2 | 10 |
| Turn-Off Delay | $t_{pd-}$ | 1,3 | - | - | - | 20 | - | - | - | - | - | 20 | - | - | ns | 1 | 3 | - | - | - | - | - | - | - | 4 | - | 2 | 10 |
| Rise Time | $t_+$ | 1,3 | - | - | - | 8.0 | - | - | - | - | - | 8.0 | - | - | ns | 1 | 3 | - | - | - | - | - | - | - | 4 | - | 2 | 10 |
| Fall Time | $t_-$ | 1,3 | - | - | - | 5.0 | - | - | - | - | - | 5.0 | - | - | ns | 1 | 3 | - | - | - | - | - | - | - | 4 | - | 2 | 10 |

* Prime Fan-Out
† Ground inputs to gates not under test, during ALL tests unless otherwise noted.
‡ The inputs to all gates must be ungrounded.