



4-Bit Binary Counter (with Synchronous Clear)

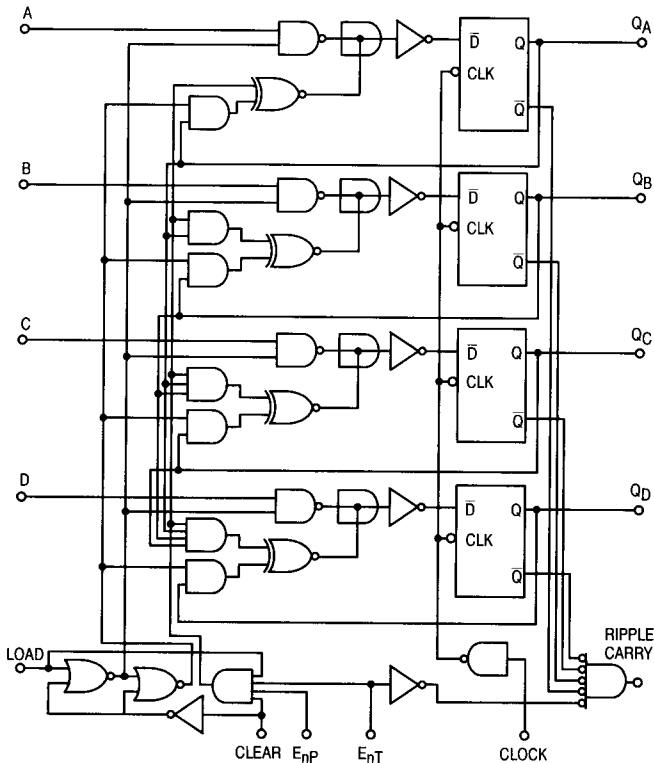
ELECTRICALLY TESTED PER:
MIL-M-38510/31512

The 'LS163A is a high-speed 4-bit synchronous counter. It is edge-triggered, synchronously presettable, and cascadable with MSI building blocks for counting, memory addressing, frequency division and other applications. The 'LS163A can count modulo 16 (binary).

The 'LS163A has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

- Synchronous Counting and Loading
- Two Count Enable Inputs For High-Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Typical Count Rate of 35 MHz

LOGIC DIAGRAM



Military 54LS163A



AVAILABLE AS:

- 1) JAN: JM38510/31512BXA
- 2) SMD: 7603401
- 3) 883: 54LS163A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

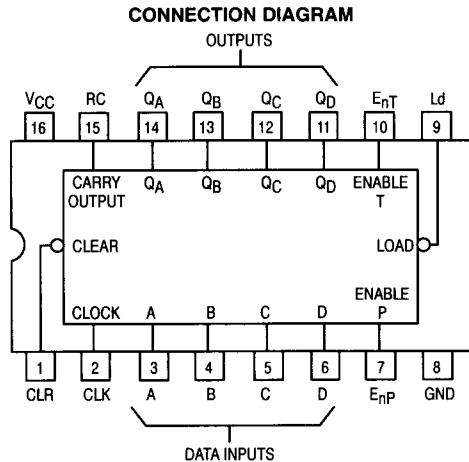
| FUNCT. | DIL 620-09 | FLATS 650-05 | LCC 756A-02 | BURN-IN (COND. A) |
|--------|---------------|-----------------|----------------|----------------------|
| CLR | 1 | 1 | 2 | GND |
| CLK | 2 | 2 | 3 | VCC |
| A | 3 | 3 | 4 | VCC |
| B | 4 | 4 | 5 | VCC |
| C | 5 | 5 | 7 | VCC |
| D | 6 | 6 | 8 | VCC |
| EnP | 7 | 7 | 9 | VCC |
| GND | 8 | 8 | 10 | GND |
| Ld | 9 | 9 | 12 | VCC |
| EnT | 10 | 10 | 13 | VCC |
| QD | 11 | 11 | 14 | VCC |
| QC | 12 | 12 | 15 | VCC |
| QB | 13 | 13 | 17 | VCC |
| QA | 14 | 14 | 18 | VCC |
| RC | 15 | 15 | 19 | VCC |
| VCC | 16 | 16 | 20 | VCC |

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

| CLR | Ld | EnT | EnP | Action on the Rising Clock Edge (↑) |
|-----|----|-----|-----|--|
| L | X | X | X | Reset (Clear) |
| H | L | X | X | Load (D _n -Q _n) |
| H | H | H | H | Count (Increment) |
| H | H | L | X | No Change (Hold) |
| H | H | X | L | No Change (Hold) |

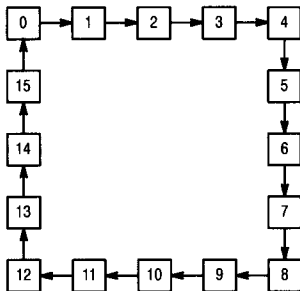
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



| Pin Names | | Loading (Note b) | |
|--------------------------------|---|------------------|-------------|
| | | HIGH | LOW |
| Load | Parallel Enable (Active LOW) | 1.0 U.L. | 0.5 U.L. |
| A-D | Parallel Inputs (Data Inputs) | 0.5 U.L. | 0.25 U.L. |
| E _{nP} | Count Enable Parallel Input | 0.5 U.L. | 0.25 U.L. |
| E _{nT} | Count Enable Trickle Input | 1.0 U.L. | 0.5 U.L. |
| CLK | Clock (Active HIGH Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| CLR | Master Reset (Active LOW) Input | 1.0 U.L. | 0.25 U.L. |
| Q _A -Q _D | Parallel Outputs (Note b) | 10 U.L. | 5(2.5) U.L. |
| RC | Terminal Count (Ripple Carry) Output (Note b) | 10 U.L. | 5(2.5) U.L. |

NOTES:

- a. One TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

STATE DIAGRAM**LOGIC EQUATIONS**

$$\begin{aligned} \text{Count Enable} &= E_{nP} \cdot E_{nT} \cdot Ld \\ \text{RC for } ^\circ\text{LS163A} &= E_{nT} \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D \\ \text{Preset} &= Ld \cdot \text{CLK} + (\text{rising clock edge}) \\ \text{Reset} &= \overline{\text{CR}} \cdot \text{CLK} + (\text{rising clock edge}) \end{aligned}$$

5

FUNCTIONAL DESCRIPTION

The $^{\circ}$ LS163A is a 4-bit synchronous counter with a synchronous Parallel Enable (Load) feature. The counter consists of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CLK). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs, Parallel Enable (Ld), Count Enable Parallel (E_{nP}) and Count Enable Trickle (E_{nT}), select the mode of operation as shown in the table below. The Count Mode is enabled when the E_{nP} , E_{nT} , and Ld inputs are HIGH. When the Ld is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the E_{nP} or E_{nT} can be used to inhibit the count sequence. With the Ld held HIGH, a LOW on either the E_{nP} or E_{nT} inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output

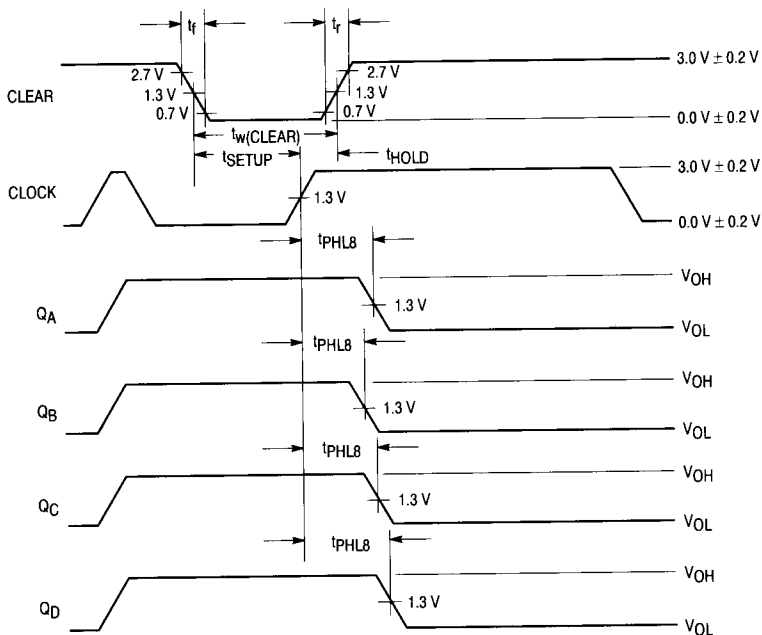
states to be retained. The AND feature of the two Count Enable inputs ($E_{nP} \cdot E_{nT}$) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (RC) output is HIGH when the Counter Enable Trickle (E_{nT}) input is HIGH while the counter is in its maximum count state (HLLH for BCD counters, HHHH for Binary counters). Note that RC is fully decoded and will, therefore, be HIGH only for one count state.

The $^{\circ}$ LS163A counts modulo 16 following a binary sequence. It generates an RC when the E_{nT} input is HIGH while the counter is in the state 15 (HHHH). From this state they increment to state 0 (LLLL).

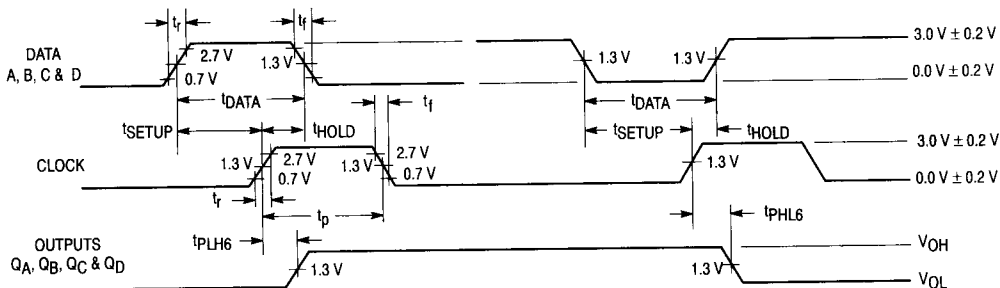
The active LOW Synchronous Reset ($\overline{\text{CR}}$) input of the $^{\circ}$ LS163A acts as an edge-triggered control input, overriding E_{nT} , E_{nP} and Ld , and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

VOLTAGE WAVEFORM 1



NOTE:
 The Clear pulse generator has the following characteristics:
 $V_{\text{gen}} = 3.0 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_w(\text{Clear}) = 25 \text{ ns}$,
 $t_{\text{SETUP}} = 25 \text{ ns}$, $t_{\text{HOLD}} = 0 \text{ ns}$.

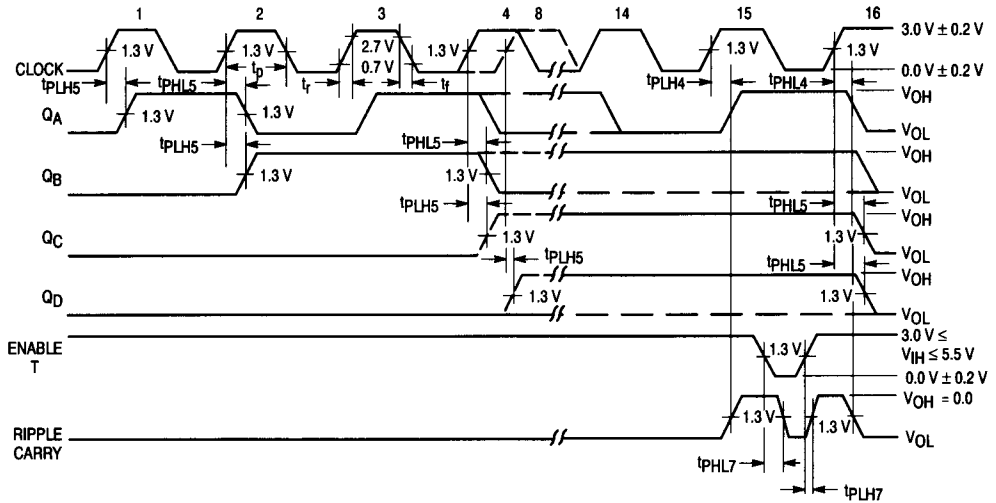
VOLTAGE WAVEFORM 2



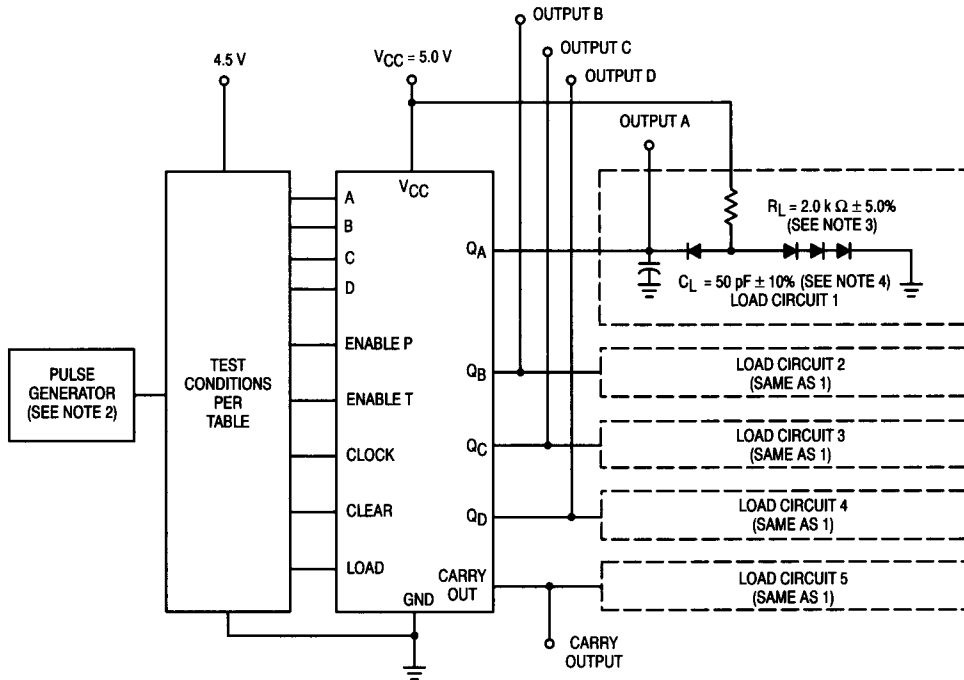
NOTE:
 The data pulse generator has the following characteristics:
 $V_{\text{gen}} = 3.0 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_{\text{DATA}} = 30 \text{ ns}$, $t_{\text{SETUP}} = 20 \text{ ns}$,
 $t_{\text{HOLD}} = 10 \text{ ns}$.

54LS163A

VOLTAGE WAVEFORM 3



TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-198

54LS163A

| Symbol | Parameter | Limits | | | | | | Unit | Test Condition (Unless Otherwise Specified) |
|------------------|------------------------------|------------|------|-------------|------|-------------|------|------|--|
| | | + 25°C | | + 125°C | | - 55°C | | | |
| | | Subgroup 1 | | Subgroup 2 | | Subgroup 3 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| V _{OH} | Logical "1" Output Voltage | 2.5 | | 2.5 | | 2.5 | | V | V _{CC} = 4.5 V, I _{OH} = -0.4 mA, V _{IL} = 0.7 V, CR = 4.5 V, E _{NP} = open, CLK = (See Note 7), V _{IH} = 2.0 V, E _{NT} = 2.0 V, L _d = GND. |
| V _{OL} | Logical "0" Output Voltage | | 0.4 | | 0.4 | | 0.4 | V | V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V, L _d = GND, CLK = (See Note 7), V _{IH} = 2.0 V, CR = 4.5 V, E _{NP} = open, E _{NT} = 0.7 V. |
| V _{IC} | Input Clamping Voltage | | -1.5 | | | | | V | V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open. |
| I _{IH} | Logical "1" Input Current | | 20 | | 20 | | 20 | μA | V _{CC} = 5.5 V, V _{IH} = 2.7 V, (other inputs are open). |
| I _{IH} | Logical "1" Input Current | | 40 | | 40 | | 40 | μA | V _{CC} = 5.5 V, V _{IH} = 2.7 V (other inputs are open). |
| I _{IHH} | Logical "1" Input Current | | 100 | | 100 | | 100 | μA | V _{CC} = 5.5 V, V _{IHH} = 5.5 V (other inputs are open), L _d & E _{NT} = GND or open. |
| I _{IHH} | Logical "1" Input Current | | 200 | | 200 | | 200 | μA | V _{CC} = 5.5 V, V _{IHH} = 5.5 V (other inputs are open), L _d & E _{NP/T} = GND or 5.5 V. |
| I _{OS} | Output Short Circuit Current | -15 | -100 | -15 | -100 | -15 | -100 | mA | V _{CC} = 5.5 V, V _{IN} = 4.5 V (other inputs are open), L _d = GND, V _{OUT} = GND, CLK = (See Note 7), CR = 4.5 V, E _{NP/T} = open. |
| I _{IL1} | Logical "0" Input Current | -300 | -760 | -300 | -760 | -300 | -760 | μA | V _{CC} = 5.5 V, V _{IN} = 0.4 V (other inputs are open), L _d & E _{NP/T} = 4.5 V or 0.4 V. |
| I _{IL2} | Logical "0" Input Current | -120 | -360 | -120 | -360 | -120 | -360 | μA | V _{CC} = 5.5 V, V _{IN} = 0.4 V (other inputs are open). |
| I _{IL3} | Logical "0" Input Current | -160 | -400 | -160 | -400 | -160 | -400 | μA | V _{CC} = 5.5 V, V _{IN} = 0.4 V (other inputs are open), L _d = GND. |
| I _{IL4} | Logical "0" Input Current | -150 | -380 | -150 | -380 | -150 | -380 | μA | V _{CC} = 5.5 V, V _{IN} = 0.4 V, L _d & E _{NT} = 4.5 V, other inputs are open. |
| I _{IL5} | Logical "0" Input Current | -150 | -450 | -150 | -450 | -150 | -450 | μA | V _{CC} = 5.5 V, V _{IN} = 0.4 V. |
| I _{CCH} | Power Supply Current Off | | 31 | | 31 | | 31 | mA | V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), L _d = 5.5 V or GND. |
| I _{CCL} | Power Supply Current Off | | 32 | | 32 | | 32 | mA | V _{CC} = 5.5 V, V _{IN} = GND (all inputs), CLK = GND or 5.5 V. |
| V _{IH} | Logical "1" Input Voltage | 2.0 | | 2.0 | | 2.0 | | V | V _{CC} = 4.5 V. |
| V _{IL} | Logical "0" Input Voltage | | 0.7 | | 0.7 | | 0.7 | V | V _{CC} = 4.5 V. |
| | Functional Tests | Subgroup 7 | | Subgroup 8A | | Subgroup 8B | | | per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V. |
| | | | | | | | | | |

54LS163A

| Symbol | Parameter | Limits | | | | | | Unit | Test Condition (Unless Otherwise Specified) |
|--|---|------------|----------|-------------|----------|-------------|----------|------|---|
| | | + 25°C | | + 125°C | | - 55°C | | | |
| | | Subgroup 9 | | Subgroup 10 | | Subgroup 11 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PHL4} t _{PHL4} | Propagation Delay /Data-Output High-Low | 3.0 — | 40 35 | 3.0 — | 56 44 | 3.0 — | 56 44 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| t _{PLH4} t _{PLH4} | Propagation Delay /Data-Output Low-High | 3.0 — | 40 35 | 3.0 — | 56 44 | 3.0 — | 56 44 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| t _{PHL5} t _{PHL5} | Propagation Delay /Data-Output High-Low | 3.0 — | 32 27 | 3.0 — | 42 34 | 3.0 — | 42 34 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| t _{PLH5} t _{PLH5} | Propagation Delay /Data-Output Low-High | 3.0 — | 29 24 | 3.0 — | 38 31 | 3.0 — | 38 31 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| t _{PHL6} t _{PHL6} | Propagation Delay /Data-Output High-Low | 3.0 — | 32 14 | 3.0 — | 48 18 | 3.0 — | 48 18 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| t _{PLH6} t _{PLH6} | Propagation Delay /Data-Output Low-High | 3.0 — | 29 14 | 3.0 — | 42 18 | 3.0 — | 42 18 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| t _{PHL7} | Propagation Delay /Data-Output High-Low | 3.0 | 19 | 3.0 | 28 | 3.0 | 28 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ |
| t _{PLH7} | Propagation Delay /Data-Output Low-High | 3.0 | 19 | 3.0 | 28 | 3.0 | 28 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ |
| t _{PHL8} t _{PHL8} | Propagation Delay /Data-Output High-Low | 3.0 — | 33 28 | 3.0 — | 46 35 | 3.0 — | 46 35 | ns | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |
| f _{MAX} f _{MAX} | Maximum Clock Frequency | 22 25 | | 22 | | 22 | | MHz | V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF. |

NOTES:

1. Voltage measurements are made with respect to ground terminal.
2. The pulse generator has the following characteristics:
V_{GEN} = 3.0 V, t_r = 6.0 ns, t_f = 6.0 ns, t_p = 0.5 μs, PRR ≤ 1.0 MHz, Z_{OUT} = 50 Ω.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ± 10%, including scope probe and jig capacitance.
5. f_{MAX}: t_r = t_f ≤ 6.0 ns.
6. The limits specified for C_L = 15 pF are guaranteed but not tested.
7. Apply one pulse prior to measurement as follows:

