9340

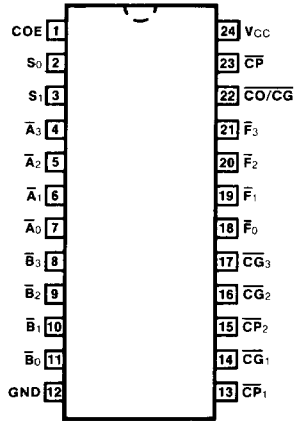
4-BIT ARITHMETIC LOGIC UNIT

(With Carry Lookahead)

DESCRIPTION — The '40 is a high speed arithmetic logic unit with full on-chip carry lookahead circuitry. It can perform the arithmetic operations add or subtract in parallel, or any of six logic functions on two 4-bit binary words. The internal carry lookahead provides either a ripple carry output or carry lookahead outputs. An internal carry input network accepts carry lookahead outputs from up to three other packages producing a 16-bit full carry lookahead ALU without additional gates. Ripple carries can be used between additional blocks of 12 bits to further expand the word length.

- **MULTIFUNCTION CAPABILITY**
  TWO ARITHMETIC OPERATIONS — ADD, SUBTRACT
  SIX LOGIC FUNCTIONS — A EX OR B, A AND B, PLUS FOUR OTHERS
- **ADD TWO 4-BIT WORDS IN 23 ns TYPICAL**
- **SUBTRACT TWO 4-BIT WORDS IN 28 ns**
- **LOOKAHEAD CARRY INPUT AND OUTPUT NETWORKS ON-CHIP**
- **EASILY EXPANDABLE TO LONGER WORD LENGTHS**
- **TYPICAL POWER DISSIPATION OF 425 mW**

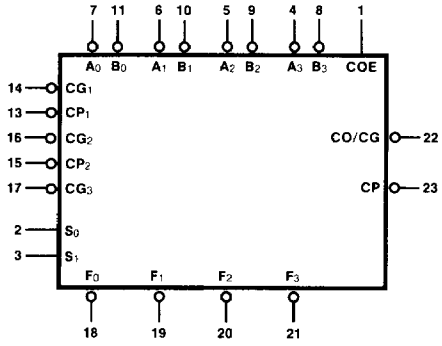
CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9340PC		9N
Ceramic DIP (D)	A	9340DC	9340DM	6N
Flatpak (F)	A	9340FC	9340FM	4M

LOGIC SYMBOL

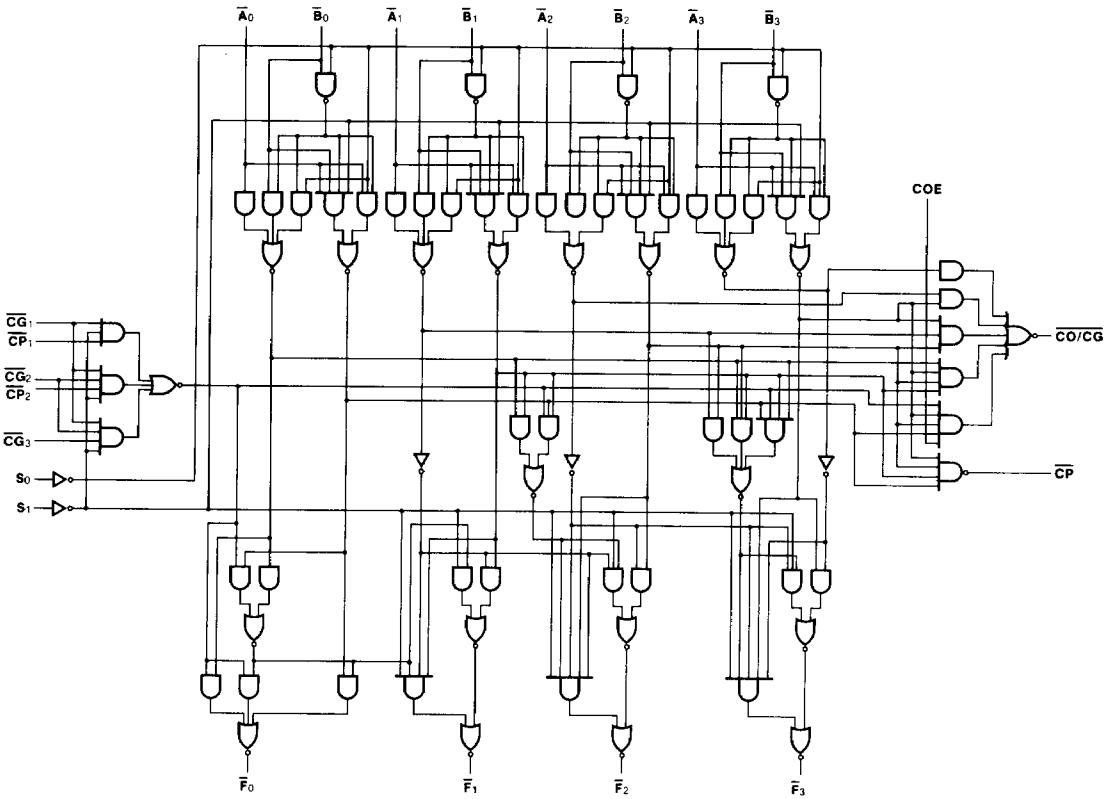


V_{CC} = Pin 24
GND = Pin 12

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand Inputs (Active LOW)	3.0/3.0
S_0, S_1	Mode Select Inputs	1.0/1.0
$\overline{CG}_1$	Carry Generate Input from immediately preceeding stage (Active LOW)	3.0/3.0
$\overline{CP}_1$	Carry Propagate Input from immediately preceeding stage (Active LOW)	1.0/1.0
$\overline{CG}_2$	Carry Generate Input from second preceeding stage (Active LOW)	2.0/2.0
$\overline{CP}_2$	Carry Propagate Input from second preceeding stage (Active LOW)	1.0/1.0
$\overline{CG}_3$	Carry Generate Input from third preceeding stage (Active LOW)	1.0/1.0
COE	Carry Out Enable Input	1.5/1.5
$\overline{F}_0 - \overline{F}_3$	Function Outputs (Active LOW)	20/10
$\overline{CO}/\overline{CG}$	Carry Out/Carry Generate Output (Active LOW)	20/10
$\overline{CP}$	Carry Propagate Output (Active LOW)	20/10

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '40 accepts two 4-bit words, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ and $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$, and produces a 4-bit output, $\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$. The output function is determined by the states on the control lines S_0 and S_1. The inputs and outputs of the '40 may be considered to be active LOW or active HIGH. Logic equivalents for four representations of the '40 are shown in Figure a, b, c, and d.

The add and subtract operations are performed on the entire word, with carries or borrows propagated between bits of different weight. The arithmetic may be performed in 1's complement, 2's complement, or sign-magnitude notation. In the logic modes, carries are inhibited and the device acts like four gates as shown.

To achieve high speed operation, the '40 is designed to be used in a carry lookahead system. Full carry lookahead is used inside the device to propagate carries between bits. Carry lookahead functions over the 4-bit block are available as outputs. These outputs are labeled $\overline{CO/CG}$ (Carry Out/Carry Generate) and $\overline{CP}$ (Carry Propagate) on the logic symbol. The carry in to the device is formed from a set of Carry Generate and Carry Propagate inputs (equation 1) so that three '40's can be interconnected without any additional gates to form a 12-bit full carry lookahead ALU with a carry in. The pin labeled COE (Carry Out Enable) controls the $\overline{CO/CG}$ output according to equation 2. When COE is HIGH, $\overline{CO/CG}$ becomes a Carry Out which can be used to ripple carries between blocks of 12 bits. The $\overline{CG}_1$ input can be used for a ripple carry input, since this signal is sufficient to produce a carry in.

EQUATION:

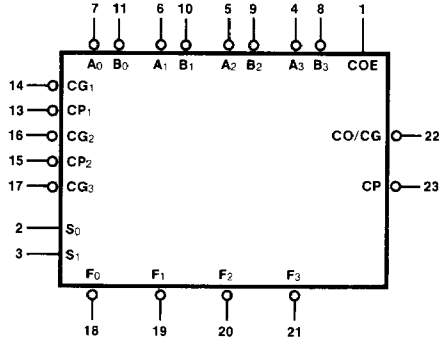
(1) $(\overline{CG}_1) + (\overline{CP}_1)(\overline{CG}_2) + (\overline{CP}_1)(\overline{CP}_2)(\overline{CG}_3) = C_{in}$ (internal)

(2) $\overline{CO/CG} = (\overline{CG}) + (\overline{CP})(C_{in})(COE)$

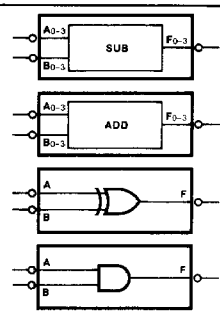
FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE '40

Note that when the input operands are defined as active HIGH, the carry lookahead inputs and outputs are not formally carry generate and carry propagate. Consequently, these pins have been relabled CX and CY in the active HIGH cases. However, the signals are connected in the same manner as $\overline{CG}$ and $\overline{CP}$.

ACTIVE LOW OPERANDS



V_{CC} = Pin 24
GND = Pin 12

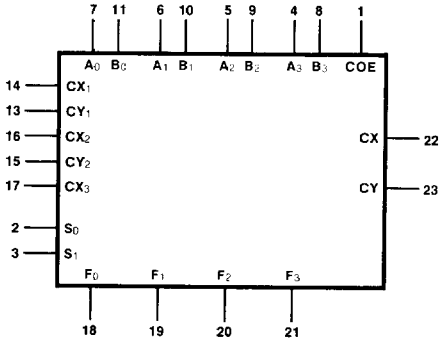
CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EX OR B	
H	H	A AND B	

H = HIGH Voltage Level
L = LOW Voltage Level

Fig. a

FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE '40 (Cont'd)

ACTIVE HIGH OPERANDS

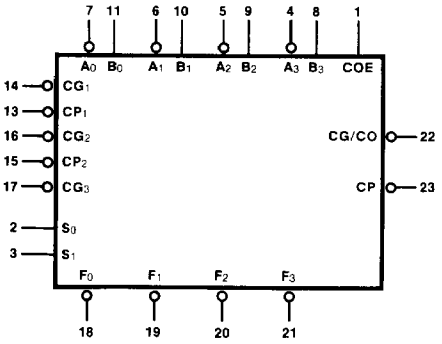


VCC = Pin 24
GND = Pin 12

CONTROL INPUTS S0	S1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EQUIV B	
H	H	A OR B	

Fig. b

ACTIVE LOW OPERANDS WITH INVERTED B

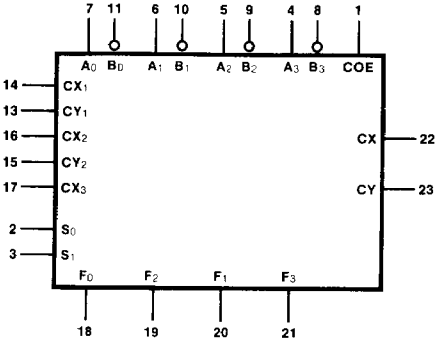


VCC = Pin 24
GND = Pin 12

CONTROL INPUTS S0	S1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EQUIV B	
H	H	A AND $\overline{B}$	

Fig. c

ACTIVE HIGH OPERANDS WITH INVERTED B



VCC = Pin 24
GND = Pin 12

CONTROL INPUTS S0	S1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EX OR B	
H	H	A OR $\overline{B}$	

Fig. d

DC CHARCTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		135	mA	V_{CC} = Max
		XC		146		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF Min	93XX C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Add Mode, $\overline{B}_0$ to $\overline{F}_3$		30 30	ns	S_0, $\overline{CG}_1$, $\overline{CP}$, $\overline{B}_1$, $\overline{B}_2$ = 4.5 V S_1, $\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_3$ = Gnd Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay for Subtract Mode, $\overline{B}_0$ to $\overline{F}_3$		37 32	ns	$\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_3$ = 4.5 V; S_0, S_1, $\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_1$, $\overline{B}_2$ = Gnd Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay for Add Mode, $\overline{B}_0$ to $\overline{CO/CG}$		20 20	ns	S_0, $\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_1$ - $\overline{B}_3$ = 4.5 V; S_1, COE, $\overline{A}_0$ - $\overline{A}_1$ = Gnd Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay for Subtract Mode, $\overline{B}_0$ to $\overline{CO/CG}$		25 22	ns	$\overline{CG}_1$, $\overline{CP}$ = 4.5 V; S_0, S_1, COE, $\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_1$ - $\overline{B}_3$ = Gnd Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay for Either Mode, $\overline{CG}_3$ to $\overline{CO/CG}$		19 19	ns	S_0, $\overline{CG}_1$, $\overline{CG}_2$, COE, $\overline{A}_0$ - $\overline{A}_3$ = 4.5 V; S_1, $\overline{B}_0$ - $\overline{B}_3$ $\overline{CP}_1$, $\overline{CP}_2$ = Gnd Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay for Either Mode, $\overline{CG}_3$ to $\overline{F}_3$		31 29	ns	S_0, $\overline{CG}_1$, $\overline{CG}_2$, $\overline{B}_3$, $\overline{A}_0$ - $\overline{A}_3$ = 4.5 V; S_1, $\overline{B}_0$ - $\overline{B}_2$, $\overline{CP}_1$, $\overline{CP}_2$ = Gnd Figs. 3-1, 3-5