To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT
μPD8875

(5400+5400) PIXELS × 3 COLOR + （5400+5400） PIXELS B&W
CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8875CY-A is a color CCD (Charge Coupled Device) linear image sensor that changes optical images to electrical signal. It has 3 rows of (5400 + 5400) staggered color pixels and (5400 + 5400) staggered pixels of black and white , and each row has dual-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 1200 dpi / A4 color image scanners.

FEATURES

- Valid photocell : (5400 + 5400) staggered pixels of RGB + (5400 + 5400) staggered pixels of B&W
- Photocell's size : 5.25 × 5.75 μm (RGB), 5.25 × 3.2 μm (B&W)
- Line spacing : 63 μm (12 lines) Red line - Green line, Green line - Blue line
  63 μm (12 lines) Blue odd line - B&W even line
- Color filter : High transmittance new color filter
  Primary colors (red, green and blue), pigment filter (with light resistance 107 lx•hour)
- Resolution : 48 dot/mm A4 (210 × 297 mm) size (shorter side) for color and B&W
  1200 dpi US letter (8.5" × 11") size (shorter side) for color and B&W
- Drive clock level : CMOS output under 5 V operation
- Data rate : 20 MHz Max (RGB), 40 MHz Max (B&W at 600 dpi mode)
- Power supply : + 12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8875CY-A	CCD linear image sensor 22 pin plastic DIP (10.16 mm (400))

Remark The μPD8875CY-A is a lead-free product.

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Date Published September 2007 NS
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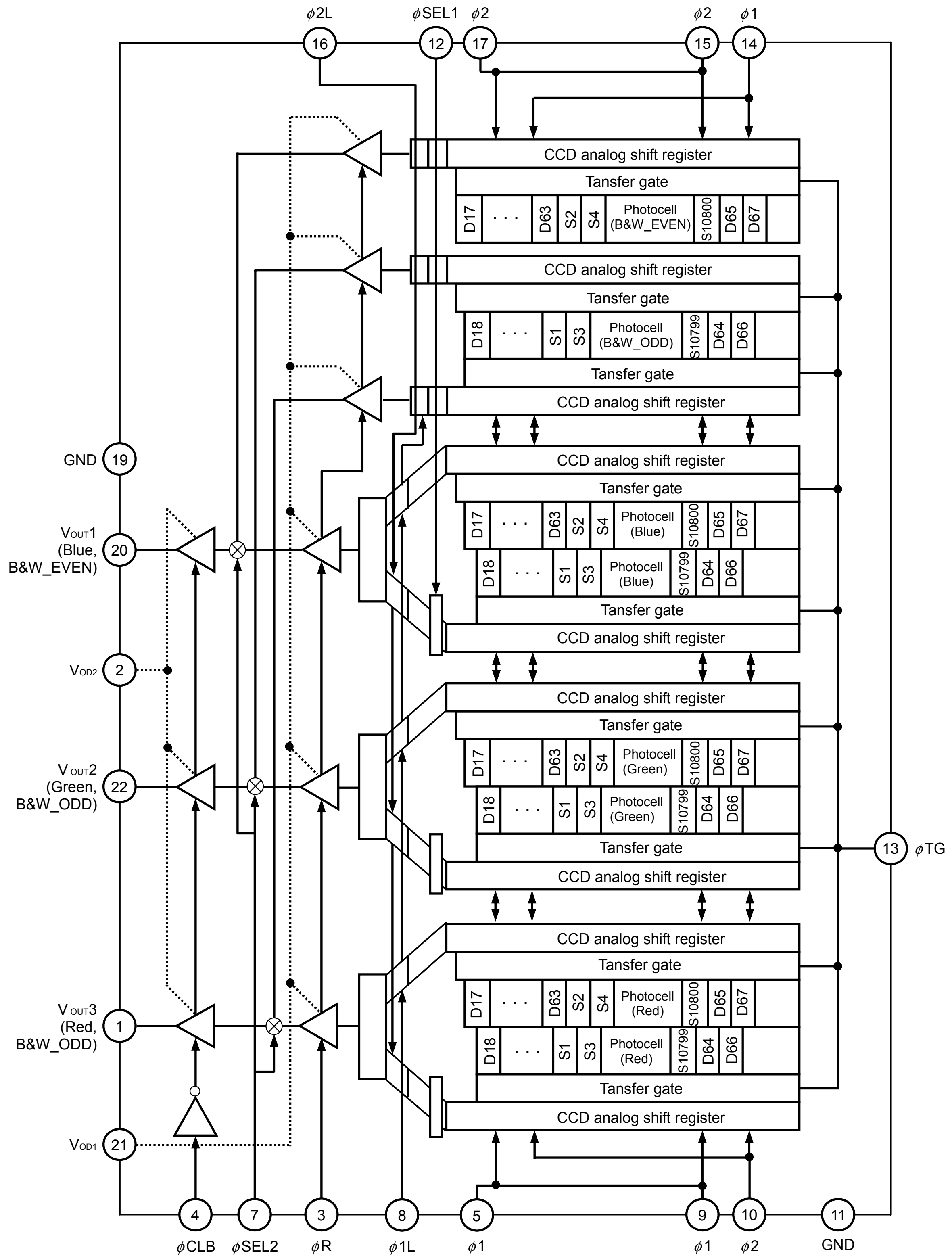
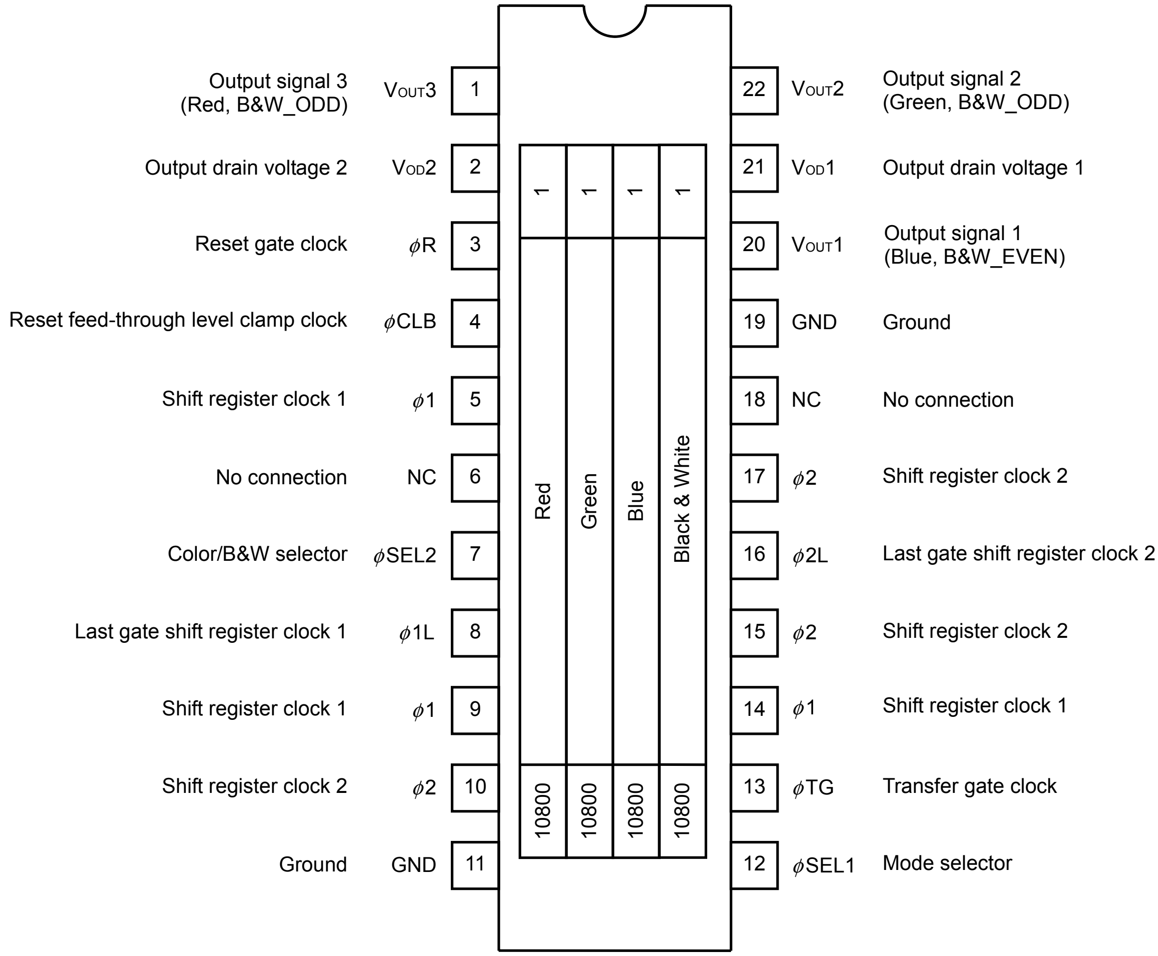
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

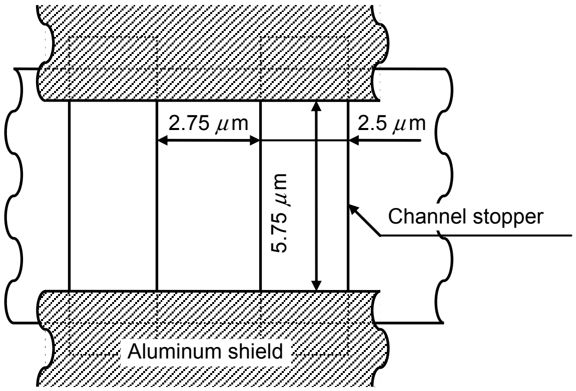
CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

μPD8875CY-A

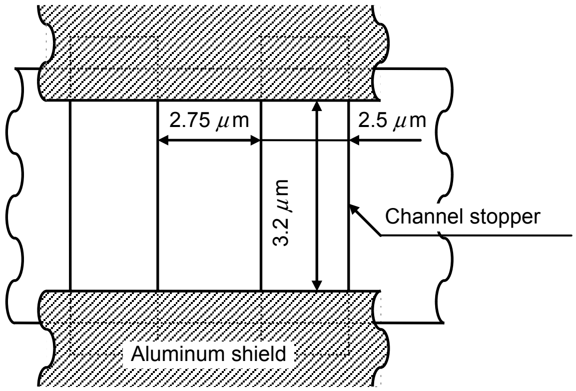


Caution Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM

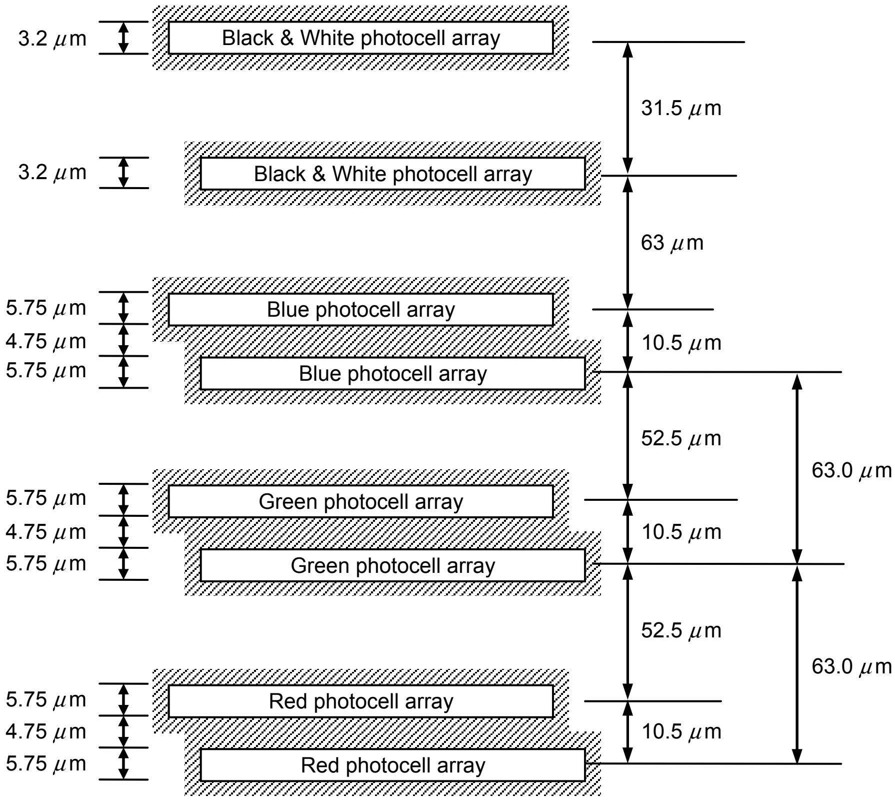


Red, Green, Blue



Black & White

PHOTOCELL ARRAY STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD1}, V_{OD2}	– 0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	– 0.3 to +8	V
Last gate shift register clock voltage	$V_{\phi 1L}$, $V_{\phi 2L}$	– 0.3 to +8	V
Reset gate clock voltage	$V_{\phi R}$	– 0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	– 0.3 to +8	V
Mode select signal voltage	$V_{\phi SEL1}$, $V_{\phi SEL2}$	– 0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG}$	– 0.3 to +8	V
Operating ambient temperature Note	T_A	0 to +55	˚C
Storage temperature	T_{stg}	– 40 to +70	˚C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD1}, V_{OD2}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 1LH}$, $V_{\phi 2LH}$	4.75	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 1LL}$, $V_{\phi 2LL}$	0	0	+0.15	V
Reset gate clock high level	$V_{\phi RH}$	4.75	5.0	5.5	V
Reset gate clock low level	$V_{\phi RL}$	0	0	+0.15	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.75	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	0	0	+0.15	V
Mode select signal high level	$V_{\phi SEL1H}$, $V_{\phi SEL2H}$	4.75	5.0	5.5	V
Mode select signal low level	$V_{\phi SEL1L}$, $V_{\phi SEL2L}$	0	0	+0.15	V
Transfer gate clock high level	$V_{\phi TGH}$	4.75	$V_{\phi 1H}$ Note	$V_{\phi 1H}$ Note	V
Transfer gate clock low level	$V_{\phi TGL}$	0	0	+0.15	V
Data rate	$f_{\phi R}$	–	2	20	MHz
Clock pulse frequency	$f_{\phi 1}$, $f_{\phi 2}$	–	1	20	MHz

Note When Transfer gate clock high level ($V_{\phi TGH}$) is higher than shift register clock high level ($V_{\phi 1H}$), image lag increases.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = +12 V, data rate ($f_{\phi R}$) = 2 MHz, storage time = 5.5 ms, input clock = 5 V_{p-p}
light source: 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm)+ HA-50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V_{sat}		2.5	3.0	–	V
Saturation exposure	Red	SE_R		–	0.3	–	lx•s
	Green	SE_G		–	0.33	–	lx•s
	Blue	SE_B		–	0.6	–	lx•s
	B&W	SE_B&W		–	0.24	–	lx•s
Photo response non-uniformity		PRNU_RGB	V_{OUT} = 1.0 V	–	6.0	20.0	%
		PRNU_B&W		–	10.0	25.0	%
Average dark signal		ADS	Light shielding	–	0.2	2.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	1.5	10.0	mV
Power consumption		P_W	Light shielding	–	360	540	mW
Output impedance		Z_O		–	0.2	0.4	kΩ
Response	Red	R_R		7.0	10.0	13.0	V/lx•s
	Green	R_G		6.3	9.0	11.7	V/lx•s
	Blue	R_B		3.5	5.0	6.5	V/lx•s
	B&W	$R_{B\&W}$		8.7	12.3	16.1	V/lx•s
Image lag		IL	V_{OUT} = 1.0 V	–	3.0	7.0	%
Offset level		V_{OS}		6.5	7.5	8.5	V
Output fall delay time Note		t_d	V_{OUT} = 1.0 V	–	15	–	ns
Total transfer efficiency Note		TTE	V_{OUT} = 1.0 V, data rate = 20 MHz	92	98	–	%
Register imbalance		RI	V_{OUT} = 1.0 V	–	1.0	4.0	%
Response peak	Red			–	610	–	nm
	Green			–	535	–	nm
	Blue			–	460	–	nm
	B&W			–	540	–	nm
Dynamic range		DR1	V_{sat}/DSNU	–	2000	–	times
		DR2	V_{sat}/σCDS	–	1363	–	times
Reset feed-through noise		RFTN	Light shielding	–2000	–100	500	mV
		PRFTN	Light shielding	–	500	800	mV
Random noise (CDS)		σCDS	Light shielding	–	2.2	–	mV

Note When the fall time of ϕ1L and ϕ2L (t1, t2) is typical value. (Refer to **TIMING CHART 2-1** to **2-3**)

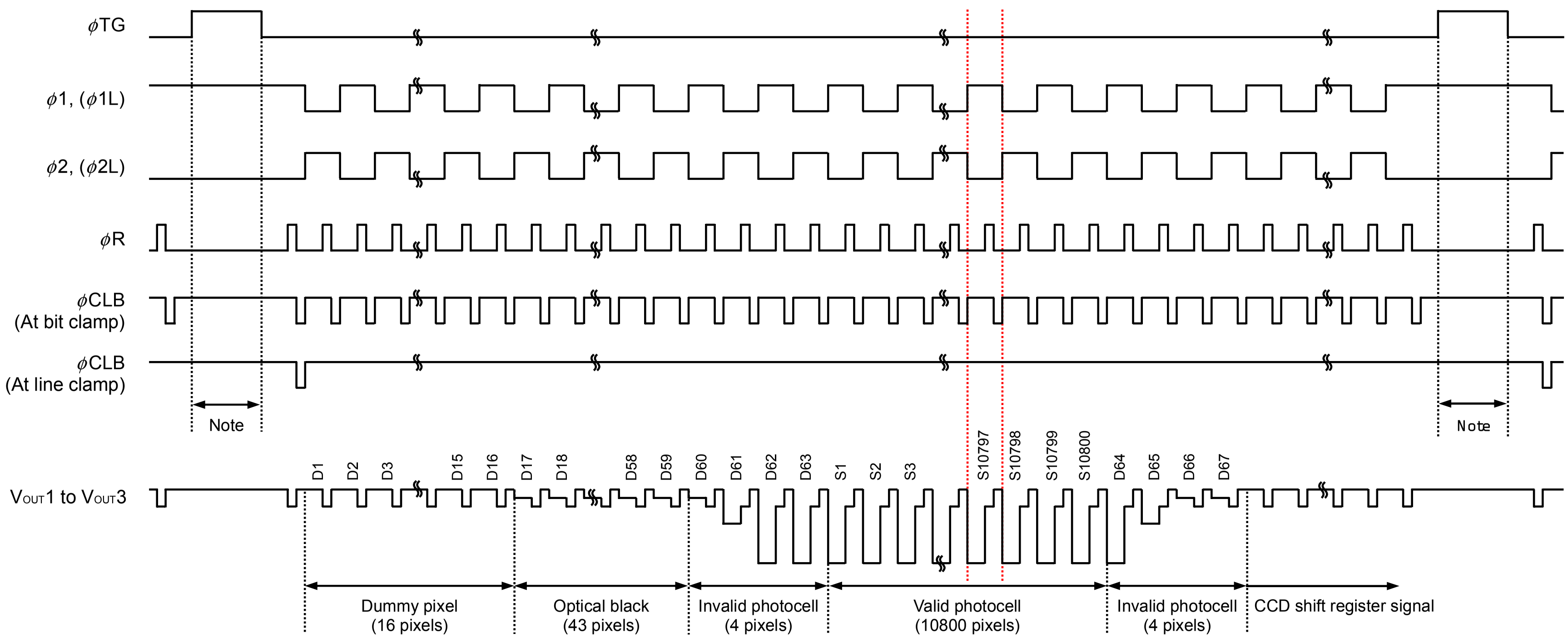
INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = +12 V)

Parameter	Symbol	Pin name	Pin No	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	5	–	600	–	pF
			9	–	600	–	pF
			14	–	600	–	pF
	$C_{\phi 1}$ total capacitance			–	1800	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	10	–	600	–	pF
			15	–	600	–	pF
			17	–	600	–	pF
	$C\phi 2$ total capacitance			–	1800	–	pF
Last gate shift register clock pin capacitance 1	$C_{\phi 1L}$	ϕ1L	8	–	10	–	pF
Last gate shift register clock pin capacitance 2	$C_{\phi 2L}$	ϕ2L	16	–	10	–	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR	3	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	4	–	10	–	pF
Select signal pin capacitance	$C_{\phi SEL1}$	ϕSEL1	12	–	10	–	pF
	$C_{\phi SEL2}$	ϕSEL2	7	–	10	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	13	–	300	–	pF

Remark **1.** Pins 5, 9, 14 (ϕ1) and pins 10, 15, 17 (ϕ2) are each connected inside of the device.

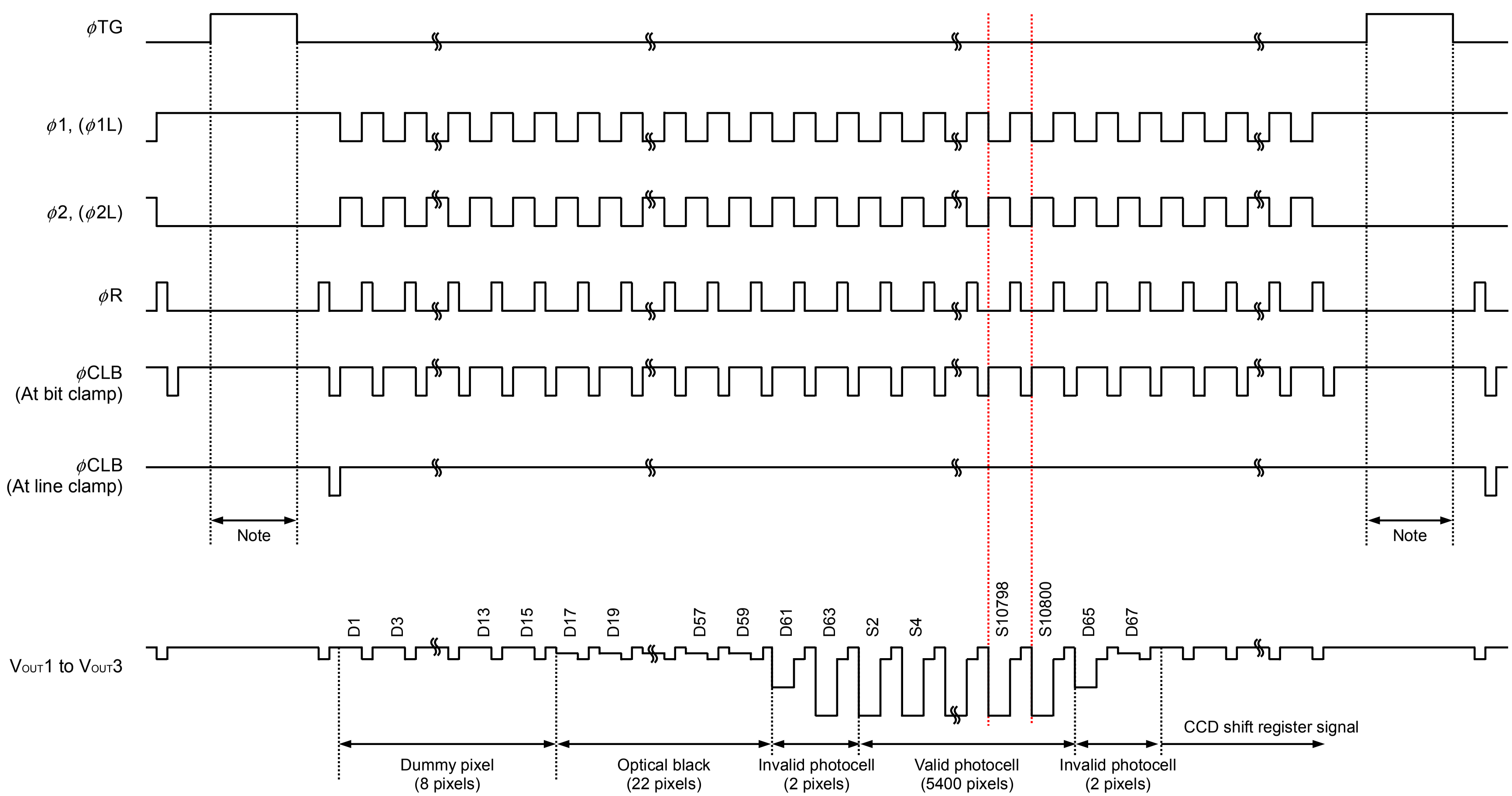
2. $C_{\phi 1}$ and $C_{\phi 2}$ show the equivalent capacity of the real drive including the capacity of between ϕ1 and ϕ2.

TIMING CHART 1-1 (Color 1200 dpi Mode, (φSEL1 = “H”, φSEL2 = “H”))



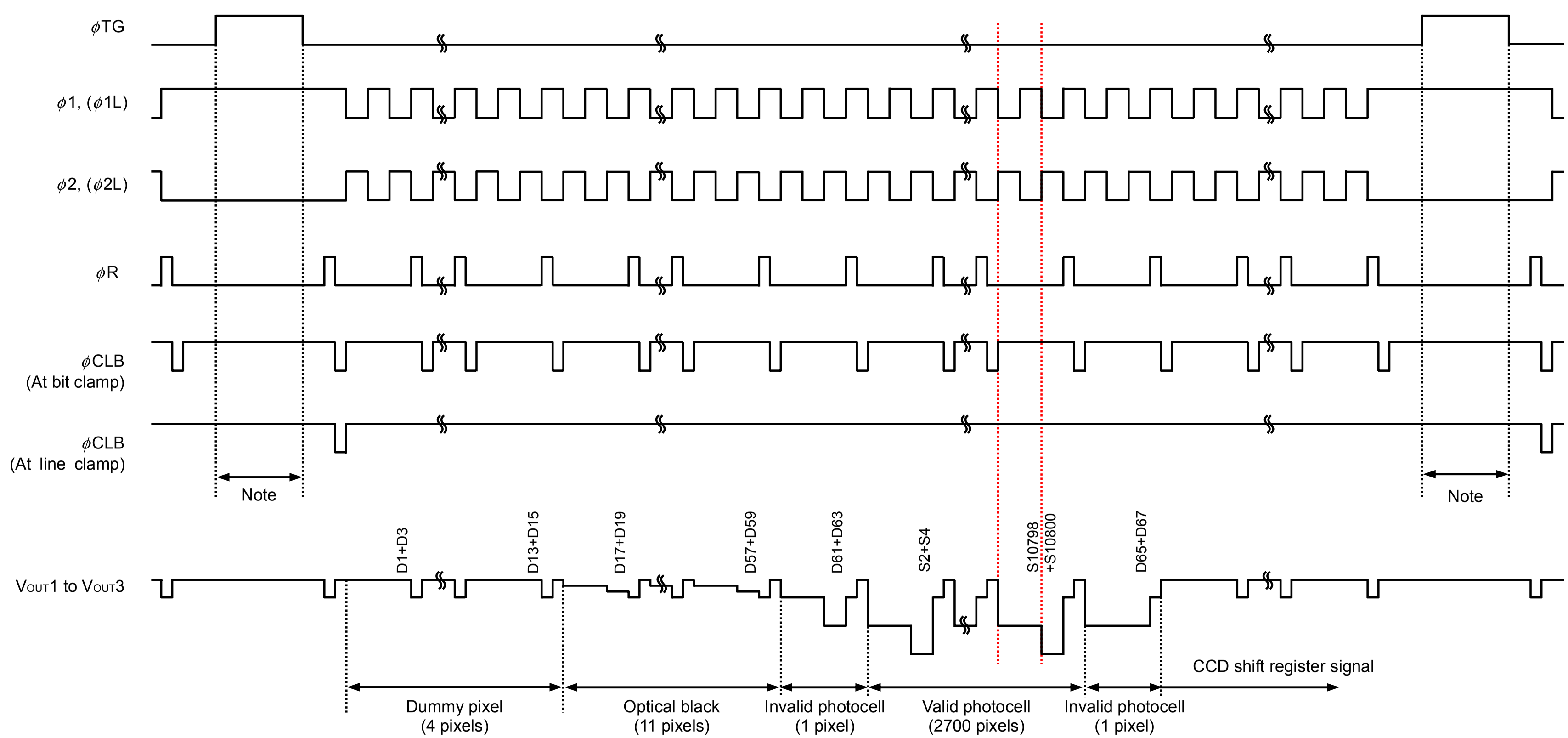
Note Set the φR to low level and the φCLB to high level during this period.

TIMING CHART 1-2 (Color 600 dpi Mode, (φSEL1 = “L”, φSEL2 = “H”))



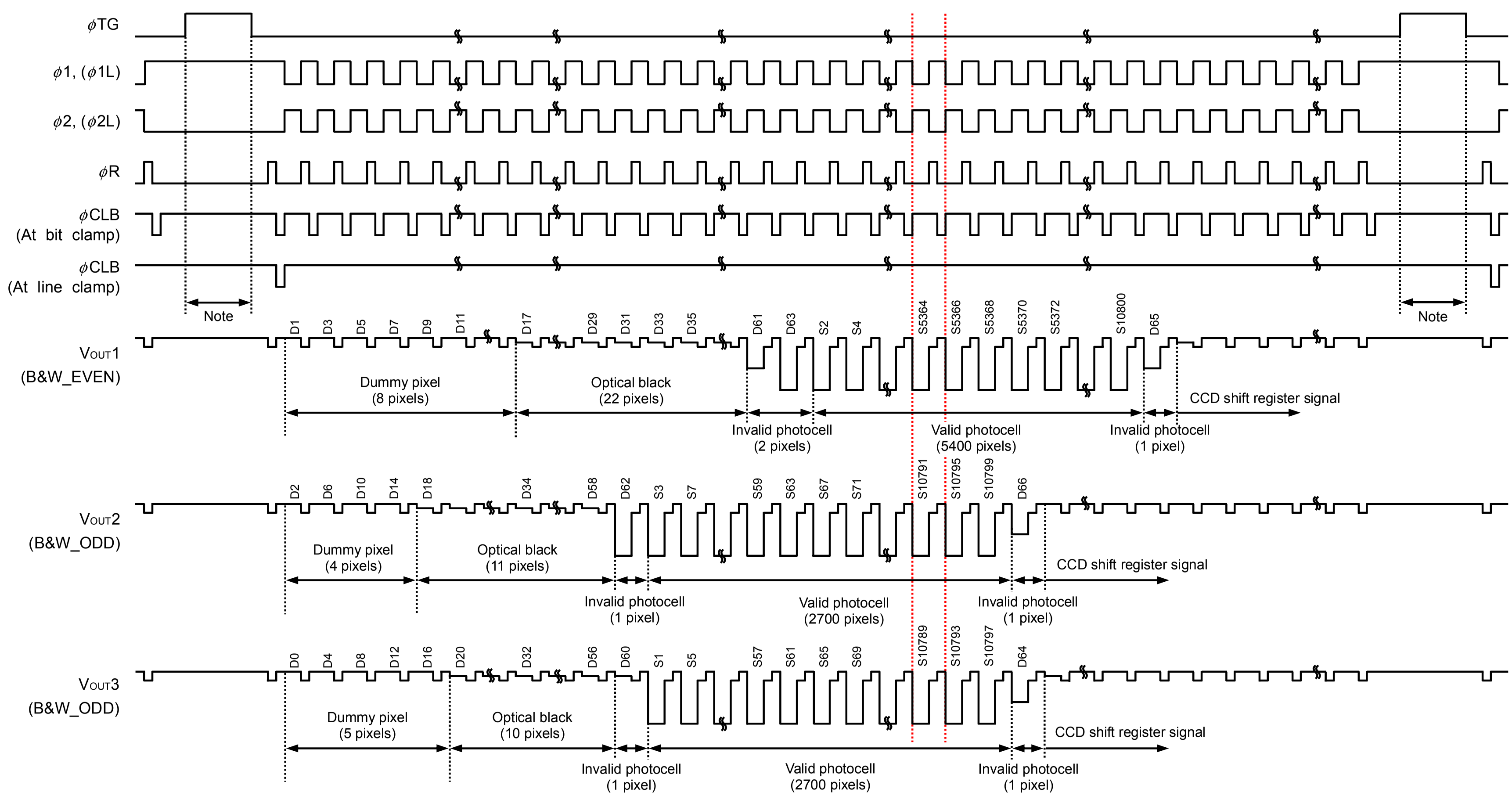
Note Set the φR to low level and the φCLB to high level during this period.

TIMING CHART 1-3 (Color 300 dpi Mode, (φSEL1 = “L”, φSEL2 = “H”))



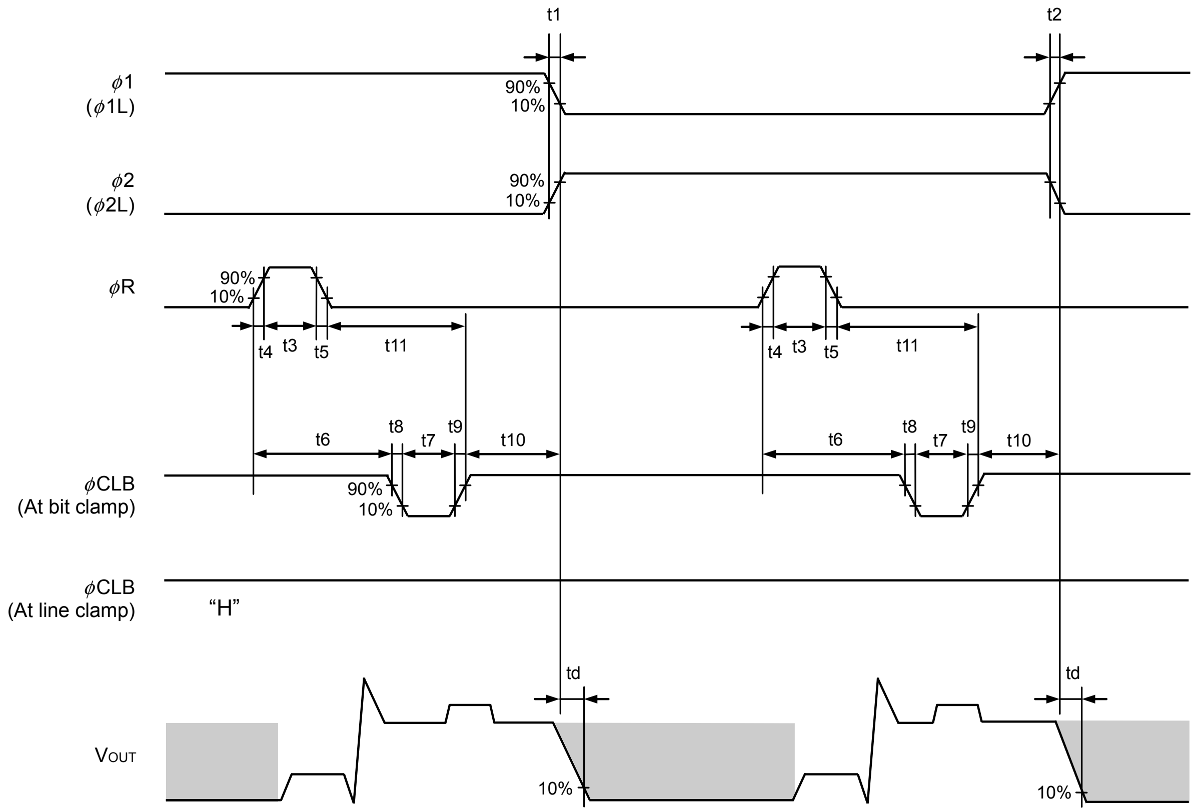
Note Set the φR to low level and the φCLB to high level during this period.

TIMING CHART 1-4 (B&W Mode, (φSEL1 = N/A, φSEL2 = “L”))



Note Set the φR to low level and the φCLB to high level during this period.

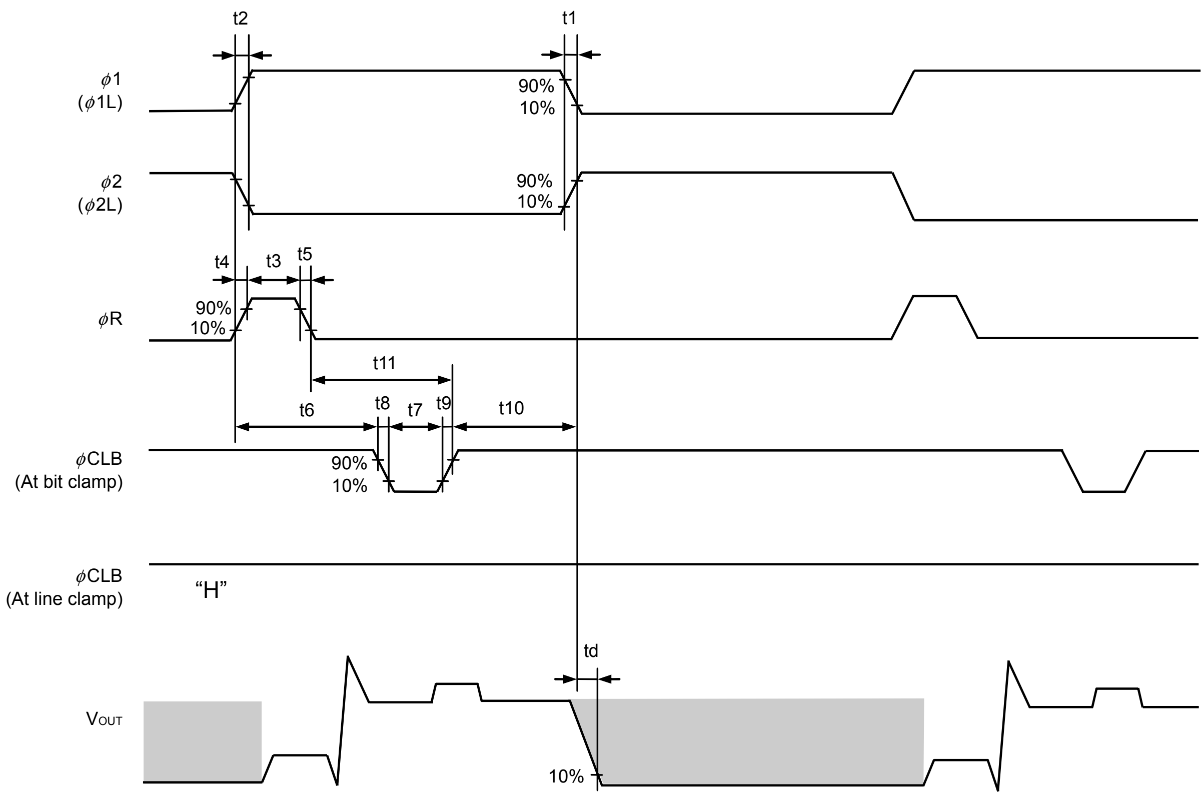
TIMING CHART 2-1 (Color 1200 dpi Mode, (ϕSEL1 = "H", ϕSEL2 = "H"))



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	10	50	–	ns
t4, t5	0	20	–	ns
t6	0	70	–	ns
t7	15	50	–	ns
t8, t9	0	20	–	ns
t10	5	45	–	ns
t11	10	70	–	ns

Note TYP. is the case of ϕR = 2 MHz

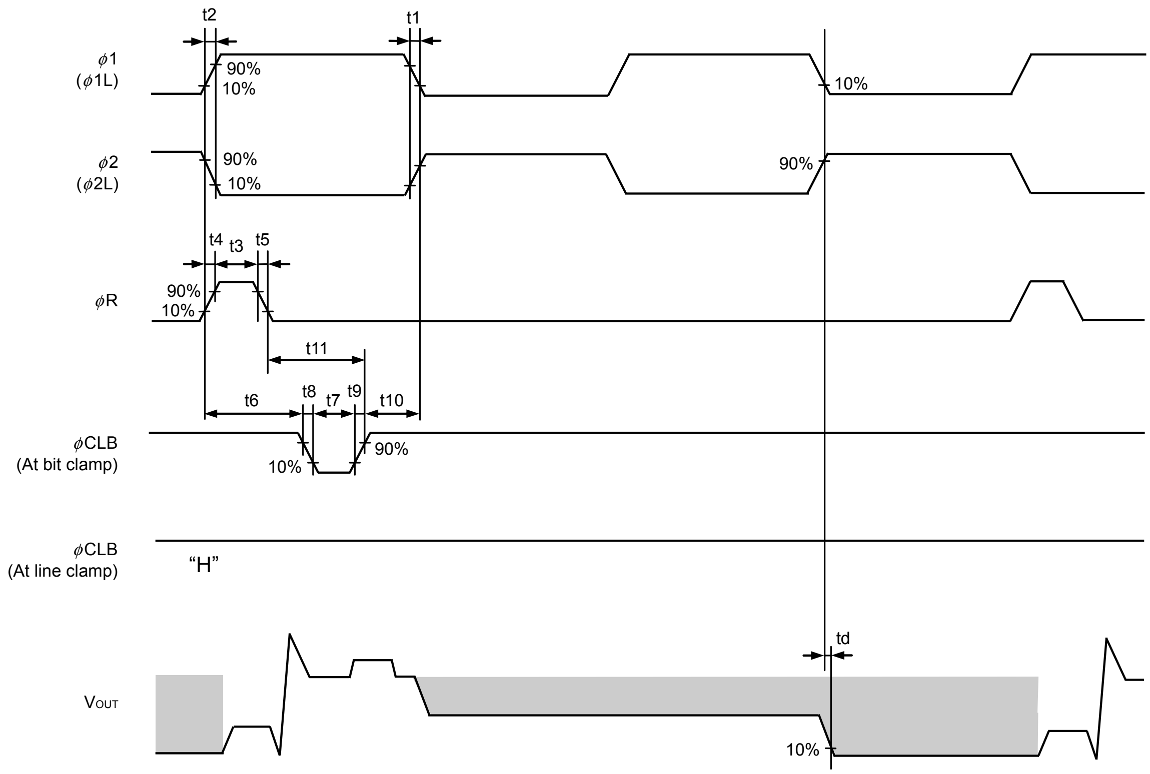
TIMING CHART 2-2 (Color 600 dpi Mode, (φSEL1 = "L", φSEL2 = "H") / B&W Mode, (φSEL1 = N/A, φSEL2 = "L"))



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	10	50	–	ns
t4, t5	0	20	–	ns
t6	0	70	–	ns
t7	15	50	–	ns
t8, t9	0	20	–	ns
t10	5	45	–	ns
t11	10	70	–	ns

Note TYP. is the case of φR = 2 MHz

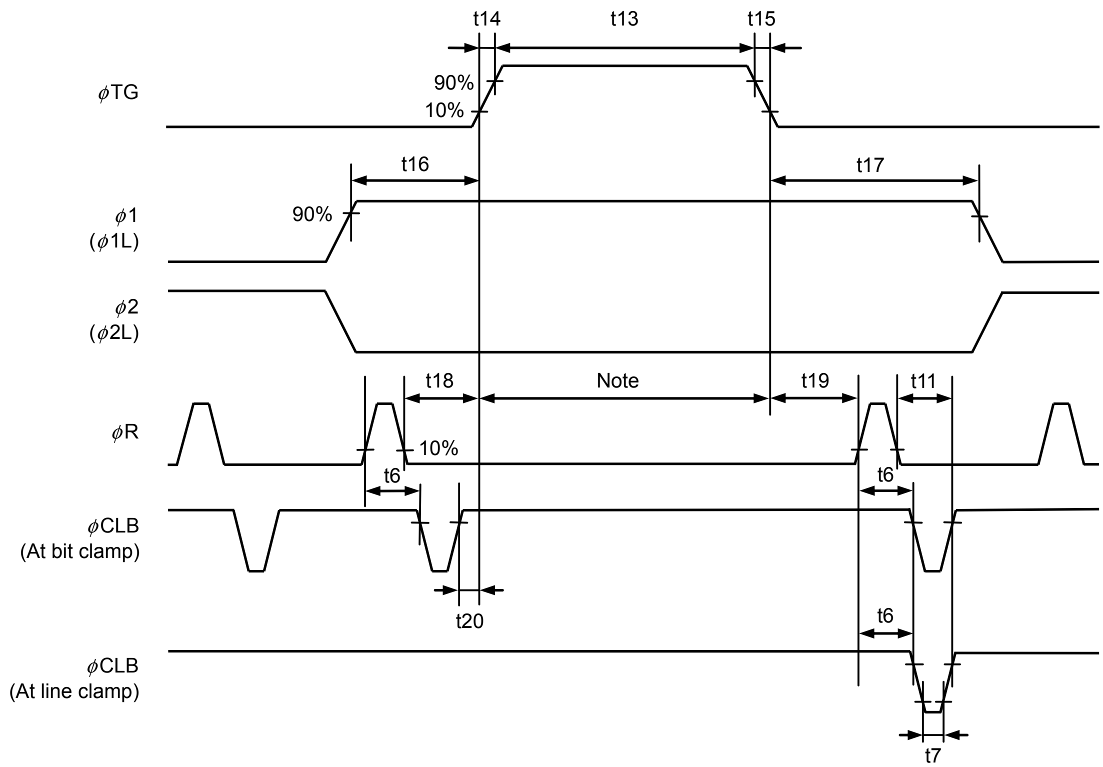
TIMING CHART 2-3 (Color 300 dpi Mode, (φSEL1 = “L”, φSEL2 = “H”))



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25	–	ns
t3	10	50	–	ns
t4, t5	0	20	–	ns
t6	0	70	–	ns
t7	15	50	–	ns
t8, t9	0	20	–	ns
t10	5	45	–	ns
t11	10	70	–	ns

Note TYP. is the case of φR = 1 MHz

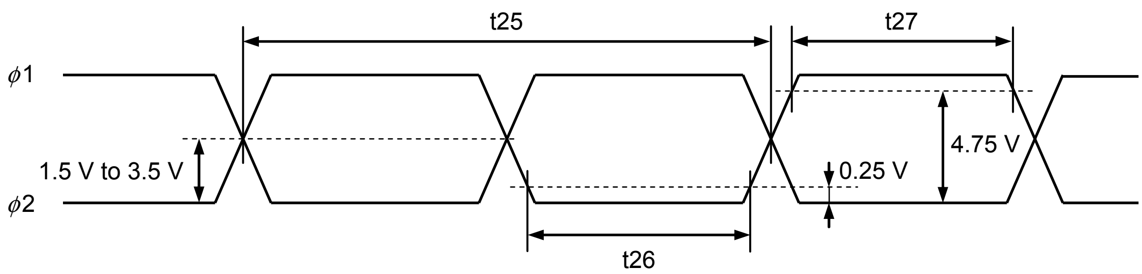
φTG, φ1 (φ1L), φ2 (φ2L) TIMING CHART



Symbol	MIN.	TYP.	MAX.	Unit
t6	0	70	–	ns
t7	15	50	–	ns
t11	10	50	–	ns
t13	5000	10000	50000	ns
t14, t15	0	50	–	ns
t16, t17	900	1000	–	ns
t18, t19	200	400	–	ns
t20	10	350	–	ns

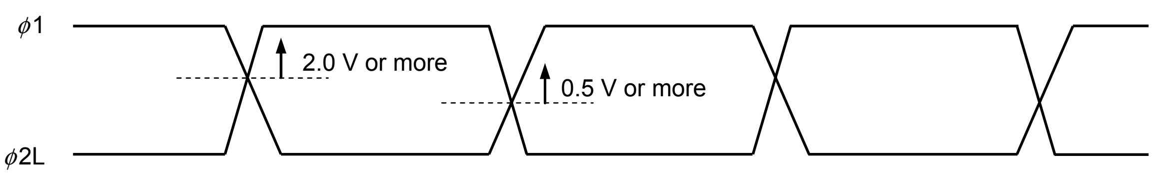
Note Set the φR to low level and the φCLB to high level during this period.

ϕ1, ϕ2 CROSS POINT

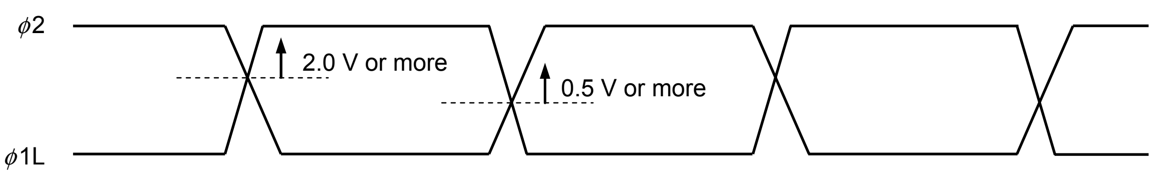


Symbol	MIN.	TYP.	MAX.	Unit
t25	50	–	–	ns
t26, t27	20	–	–	ns

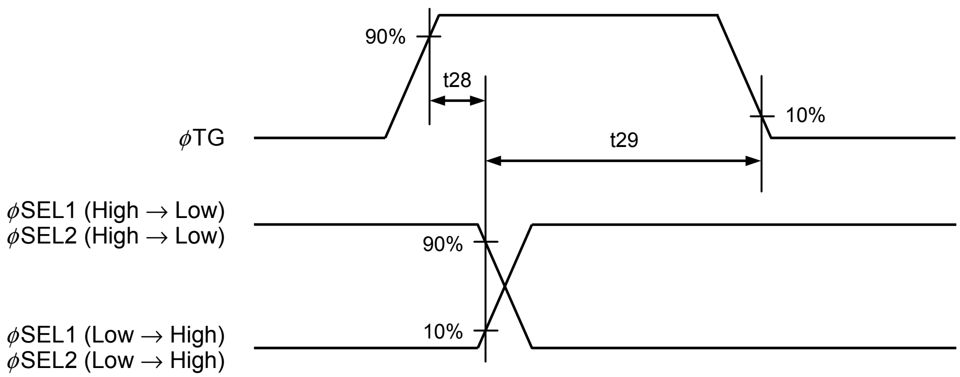
ϕ1, ϕ2L CROSS POINT



ϕ2, ϕ1L CROSS POINT



ϕTG, ϕSEL TIMING CHART



Symbol	MIN.	TYP.	MAX.	Unit
t28	0	0	–	ns
t29	4500	9500	–	ns

SELECTION OF RESOLUTION MODE

The uPD8875CY-A has function of two readout modes, High Resolution Mode and Low Resolution Mode. These two modes can be selected by ϕSEL1 switch.

Mode	Description	ϕSEL1
High Resolution Mode	1200 dpi (Max.)	High level
Low Resolution Mode	600 dpi (Max.) (even line readout mode)	Low level

(1) High Resolution Mode

In this mode, both signals in odd lines and even lines can be read out. This mode enables 1200 dpi (max.) resolution with A4 size (210 × 297 mm, shorter side).

Please refer to **TIMING CHART 1-1** and **TIMING CHART 2-1**.

(2) Low Resolution Mode

In this mode, only signal output in even lines can be read out.

Signal output in even lines: Can be read out
Signal output in odd lines: Can not be read out

This mode enables 600 dpi (max) resolution with A4 size.

To use intermittent reset drive enable signal charges of adjacent pixels in even line to add at the charge to voltage conversion area. Then it can achieve low resolution with A4 size such as 300, 200, 150 dpi.

Please refer to **TIMING CHART 1-2**, **1-3** and **TIMING CHART 2-2**, **2-3**.

DEFINITIONS OF CHARACTERISTIC

1. Saturation voltage : V_{sat}

Output signal voltage at which the response linearity is lost.

2. Saturation exposure : SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : PRNU

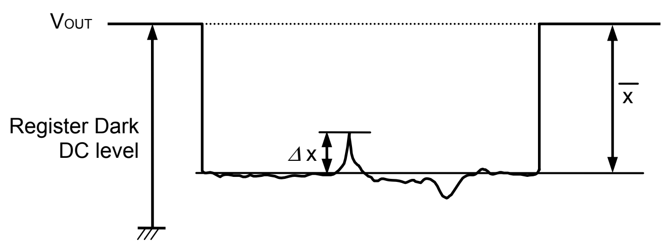
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $| x_j - \overline{x} |$

$$\overline{x} = \frac{\sum_{j=1}^{10800} x_j}{10800}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{ADS (mV)} = \frac{\sum_{j=1}^{10800} d_j}{10800}$$

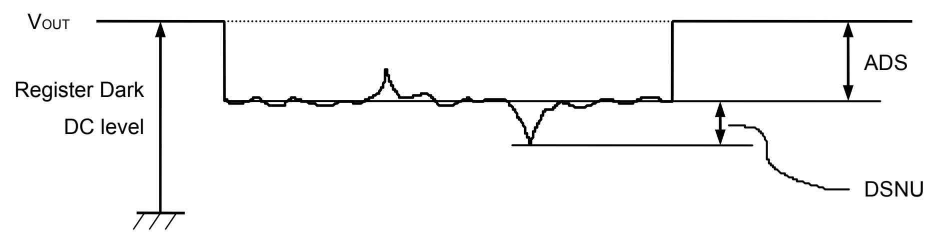
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV) : maximum of | dj – ADS | $_{j = 1 \text{ to } 10800}$

dj : Dark signal of valid pixel number j



6. Output impedance : Zo

Impedance of the output pins viewed from outside.

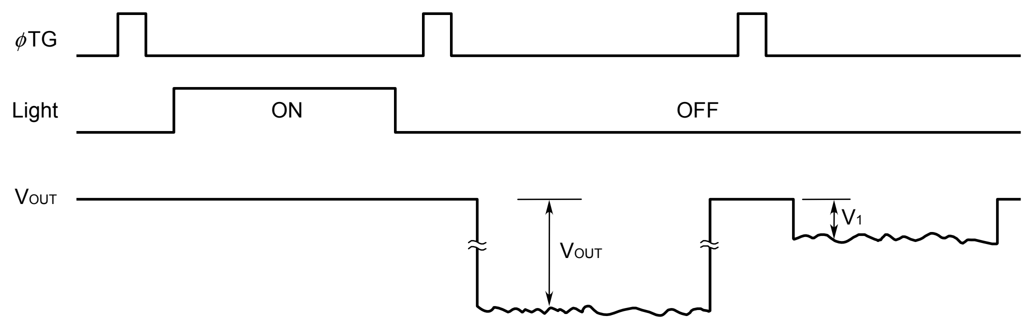
7. Response : R

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : IL

The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance : RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

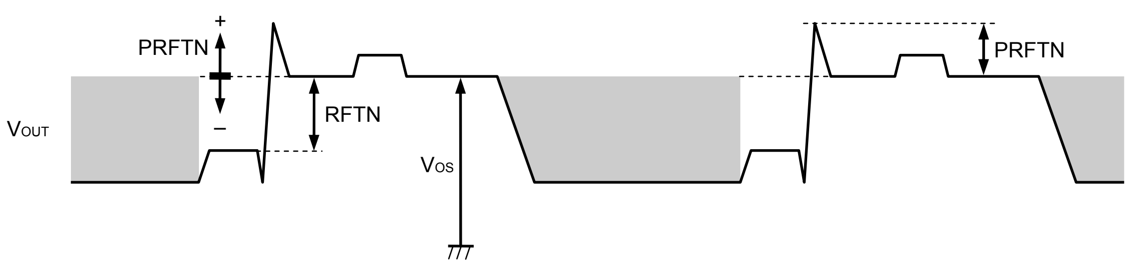
V_j : Output voltage of each pixel

10. Offset level : VOS

DC level of output signal is defined as follows.

11. Reset feed-through noise : RFTN, PRFTN

Reset feed-through noise (RFTN) and peak of RFTN (PRFTN) are defined as follows.



12. Random noise (CDS) : σCDS

Random noise σCDS is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding). σCDS is calculated by the following procedure.

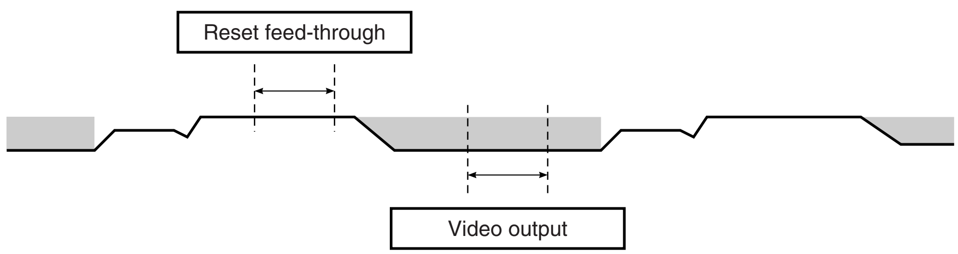
1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get "VD_i".
3. The output level is measured during the video output time averaged over 100 ns to get "VO_i".
4. The correlated double sampling output is defined by the following formula.

$$VCDS_i = VD_i - VO_i$$

5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σCDS using the following formula equation.

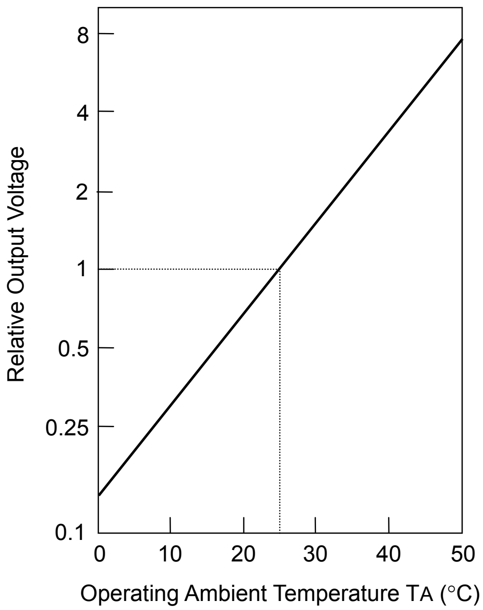
$$\sigma\text{CDS (mV)} = \sqrt{\frac{\sum_{i=1}^{100}(VCDS_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} VCDS_i$$

The following figure shows output waveform (valid photocell under dark condition).

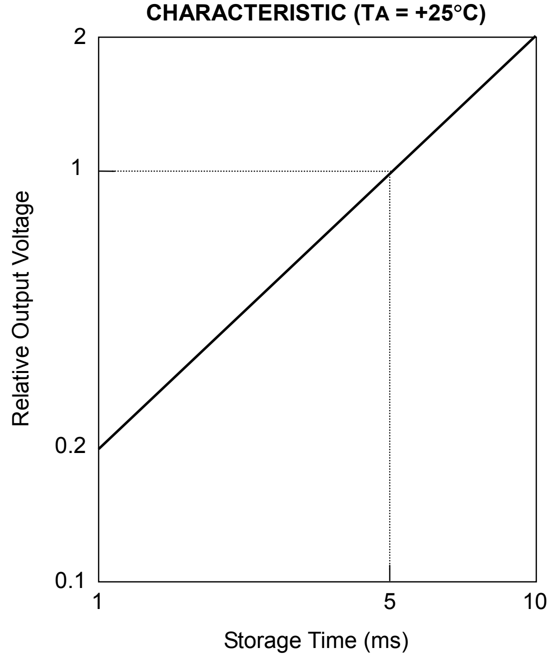


STANDARD CHARACTERISTIC CURVES (1) (Reference Value)

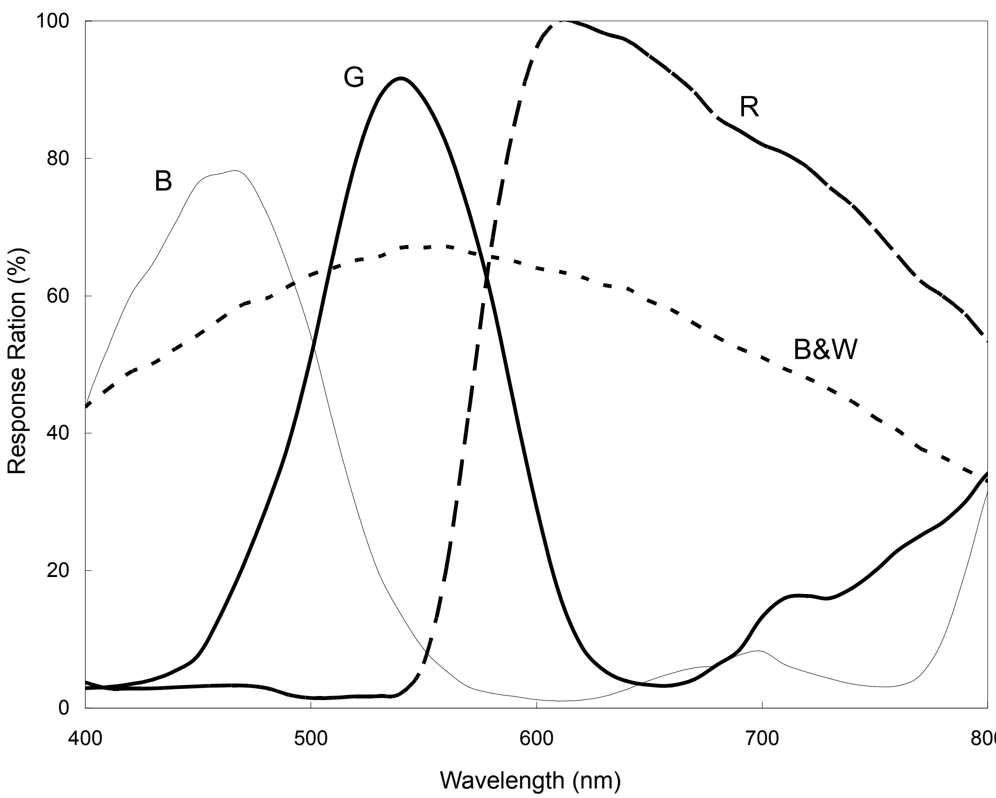
DARK OUTPUT TEMPERATURE CHARACTERISTIC



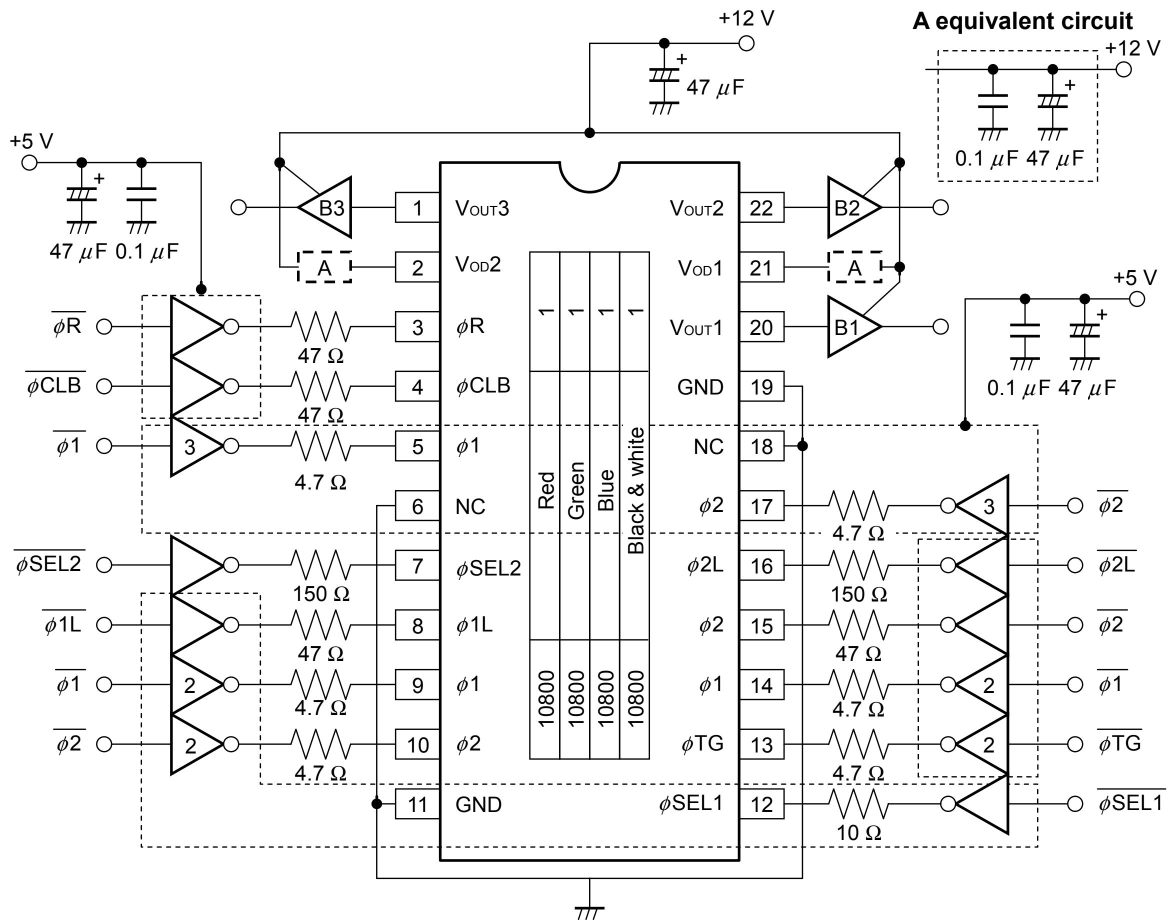
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (TA = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS
(Without infrared cut filter and heat absorbing filter) (T_A = +25 °C)

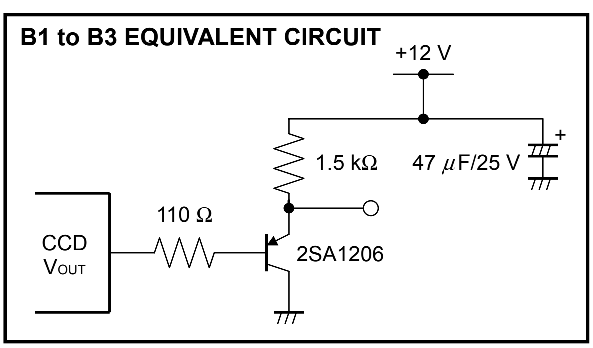


APPLICATION CIRCUIT EXAMPLE



Caution **Connect the no connection pins (NC) to GND.**

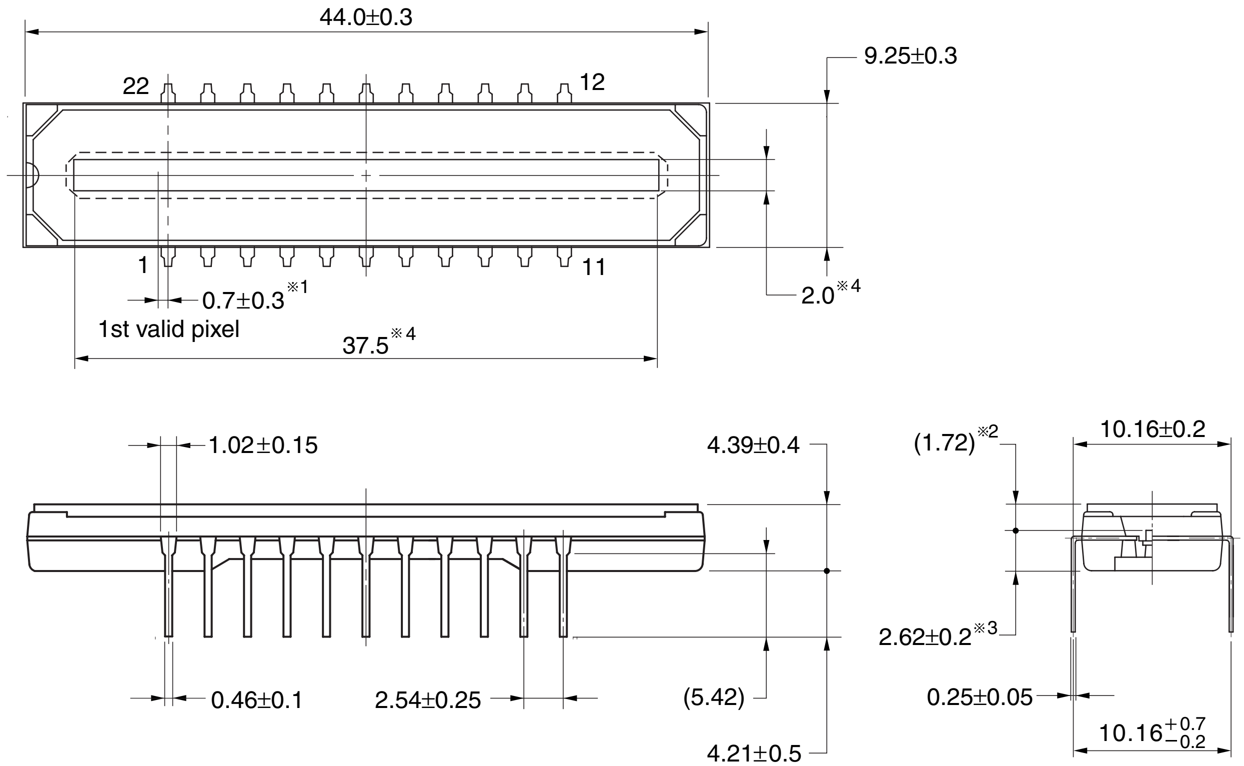
Remark The inverters are the 74AC04, and pins 5, 9, 10, 13, 14 and 17 connect two or three inverters in parallel.



PACKAGE DRAWING

μPD8875CY-A
CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.7×8.35×0.8(0.7 ※5)	1.5

※1 Distance between the 1st valid pixel and the center of the pin1
※2 Distance between the top of the cap and the surface of the CCD chip
※3 Distance between the bottom of the package and the surface of the CCD chip
※4 Transparent window
※5 Thickness of the transparent window

22C-1CCD-PKG20

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8875CY-A: CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature: 380°C or below, Heat time: 3 seconds or less (per pin).

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.

Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.