89C124FX
DATA/FAX MODEM CHIP SET

- 9600 bps Send and Receive FAX
- V.29 and V.27ter Compatible
- Supports Communicating Applications Specification (CAS)
- EIA/TIA-578 Compliant FAX Command Set (Service Class 1)
- Compatible with CCITT Group 3 FAX Machines
- 2400 bps Data Modem
- V.22bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- V.42 Compliant Error Correction (LAPM and *MNP4)
- V.42bis and MNP5 Data Compression
- Easy Upgrade from Intel Modem Chip Sets
- AT Command Set
- Minimum Chip Count for Small Size
- CHMOS for Low Operating Power
- Low Standby Power
- On-Chip Hybrid
- DTMF and Pulse Dialing
- Automatic Speed Matching in Reliable and Normal Modes
- Serial Interface to External NVRAM
- Hardware and Software Flow Control
- Analog/Digital Loopback Diagnostics
- Automatically Detects Remote Modem Type and Data Rate
- Easily Customized Command Set and Features
- Synchronous Modes
- On-Chip Serial Port Handshake Signals for RS-232/V.24 Interface
- Packaging
  - —89127:
    28-Lead PDIP and PLCC, 64-Lead QFP Packages
    Package Type P, N and S
  - —89C126FX:
    68-Lead PLCC and 80-Lead QFP
    Package Type N and SB

(See Packaging Spec Order No. 240800)

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Order Number: 290415-002

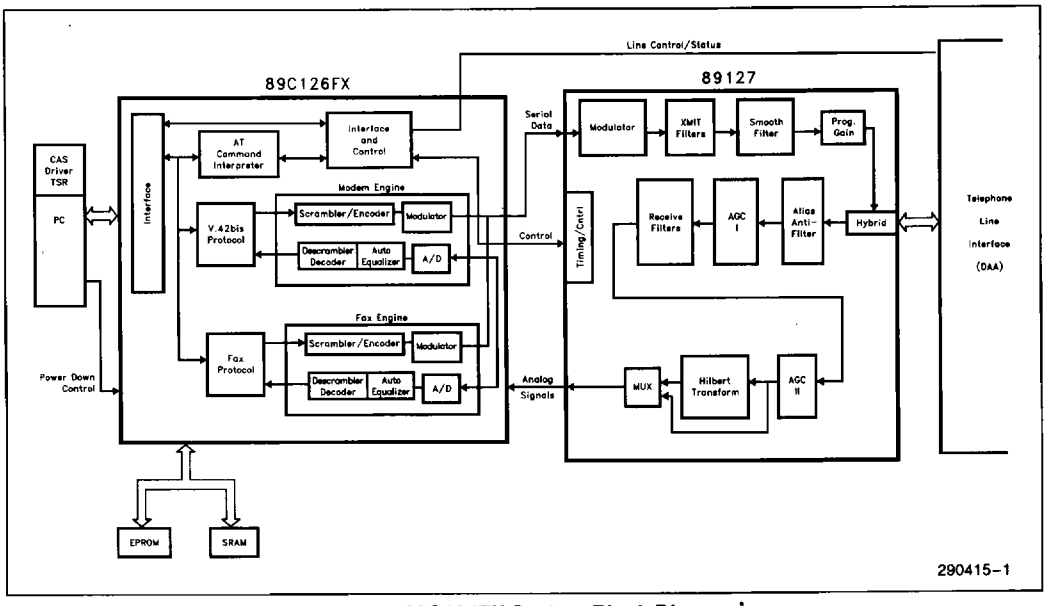


Figure 1. 89C124FX System Block Diagram

GENERAL DESCRIPTION

The Intel 89C124FX is a highly integrated, Send and Receive data-FAX modem chipset. This two chip solution is composed of the 89C126FX microcontroller and the 89127 Analog Front End. The 89C124FX features 9600 bps Send and Receive FAX, V.42/V.42bis error correction and data compression, low power consumption, easy upgrade from other Intel modem chipsets, and ease of use, via the Intel/DCA Communicating Applications Specification (CAS).

The 89C126FX microcontroller executes DSP algorithms for modulation, demodulation, and data formatting. It also performs the AT and EIA/TIA-578 command set interface functions, and error correction and data compression. The 89C126FX comes in a 68-pin PLCC package.

The 89127 AFE provides D/A conversion, filtering, AGC, 2 wire hybrid conversion and telephone line data access arrangement (DAA) interface. The 89127 comes in 28-pin PLCC and 28-pin PDIP packages.

EIA/TIA-578

EIA/TIA-578 is a specification of AT level commands for control of FAX functions. EIA/TIA-578 compliancy assures compatibility with products conforming to this industry standard. EIA/TIA-578 is also known as "Facsimile Service Class 1".

Communicating Applications Specification (CAS)

CAS is a high-level Applications Programmer Interface (API) which: 1) Allows the end user to FAX directly from an application program without using a standalone communications package, and 2) Gives PC-based application software vendors an easy way to include FAX functionality in their products. The 89C124FX supports CAS via a Terminate and Stay Resident (TSR) driver program that resides on the PC. The CAS TSR driver communicates with the 89C124FX via the EIA/TIA-578 interface.

V.42/V.42bis

V.42/42bis compliancy assures adherence to international error correction (V.42: LAPM) and data compression (V.42bis: BTLZ and MNP class 5) standards. V.42bis uses BTLZ (British Telecom Lempel Ziv) data compression algorithm to achieve throughputs of up to 4 times the transmission rate, effectively providing up to 9600 bps throughput with a 2400 bps modem.

V.42/42bis compliancy assures compatibility with the installed base of MNP class 4 modems, and provides an increased throughput of up to 4:1. The chip set also provides MNP class 5 operation. This provides 2:1 compression with the large installed base of MNP class 5 modems. These benefits allow the 89C124FX chip set to provide fast and reliable data transfer with the current and upcoming installed base of modems products.

System Configuration

The 89C124FX chip set, along with a Data Access Arrangement (DAA), a single 128K x 8 EPROM, and a 32K x 8 static RAM, represent the circuitry necessary for implementing a 9600 bps Send/Receive FAX, 2400 bps Data modem with V.42/V.42bis. Refer to Figure 2 for a block diagram of this application. The system is compatible with the following CCITT and Bell transmission standards:

FAX:

- CCITT V.29
  9600 bps async
  7200 bps async
- CCITT V.27ter
  4800 bps async
  2400 bps async

DATA:

- CCITT V.22bis
  2400 bps sync and async
  1200 bps sync and async
- CCITT V.22 A and B
  1200 bps sync and async
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous
- CCITT V.23

Power Down

The 89C124FX chip set supports power-down modes that are selected via the AT command set, providing flexible power-down management control. The power-down modes make the 89C124FX a good fit for laptop and notebook computer applications. Power consumption for the chip set is typically 530 mW during a connection. When powered-down, the chip set consumes 7 mW.

Commands

FAX modem functions are controlled via the EIA/TIA-578 command set. A complete set of industry standard AT commands are provided for configuration and user interface of the data modem functions. Additional commands have been implemented for power down modes, and V.42/42bis/MNP feature control. In applications where user proprietary control commands and features are desired, the user can replace the 89C124FX command module with custom proprietary software.

Optional Features

The 89C124FX supports the addition of a serial EEPROM to store configuration information, LEDs for status indication, and a speaker driver for monitoring the progress of the phone call.

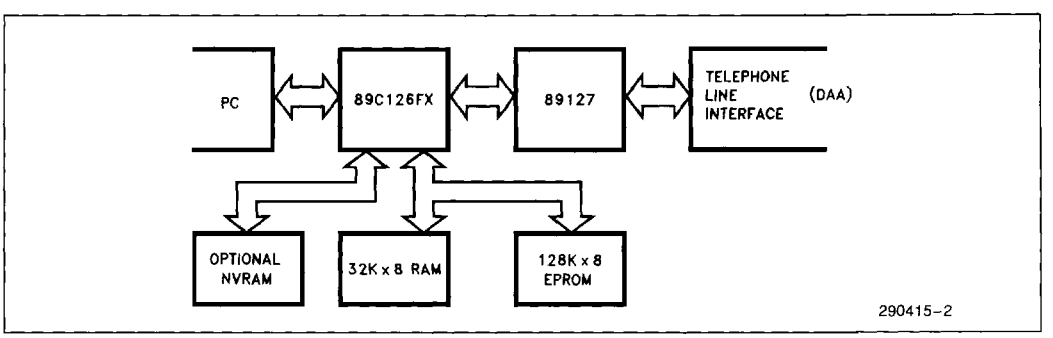


Figure 2. 89C124FX System Block Diagram

PACKAGING

The 89C124FX chipset is available in PLCC and QFP packaging. The 89127 is also available in PDIP packaging. Packages are shown from top view, looking down on component side of PC board. Refer to Intel Packaging handbook, order number 240800 for more details on packaging.

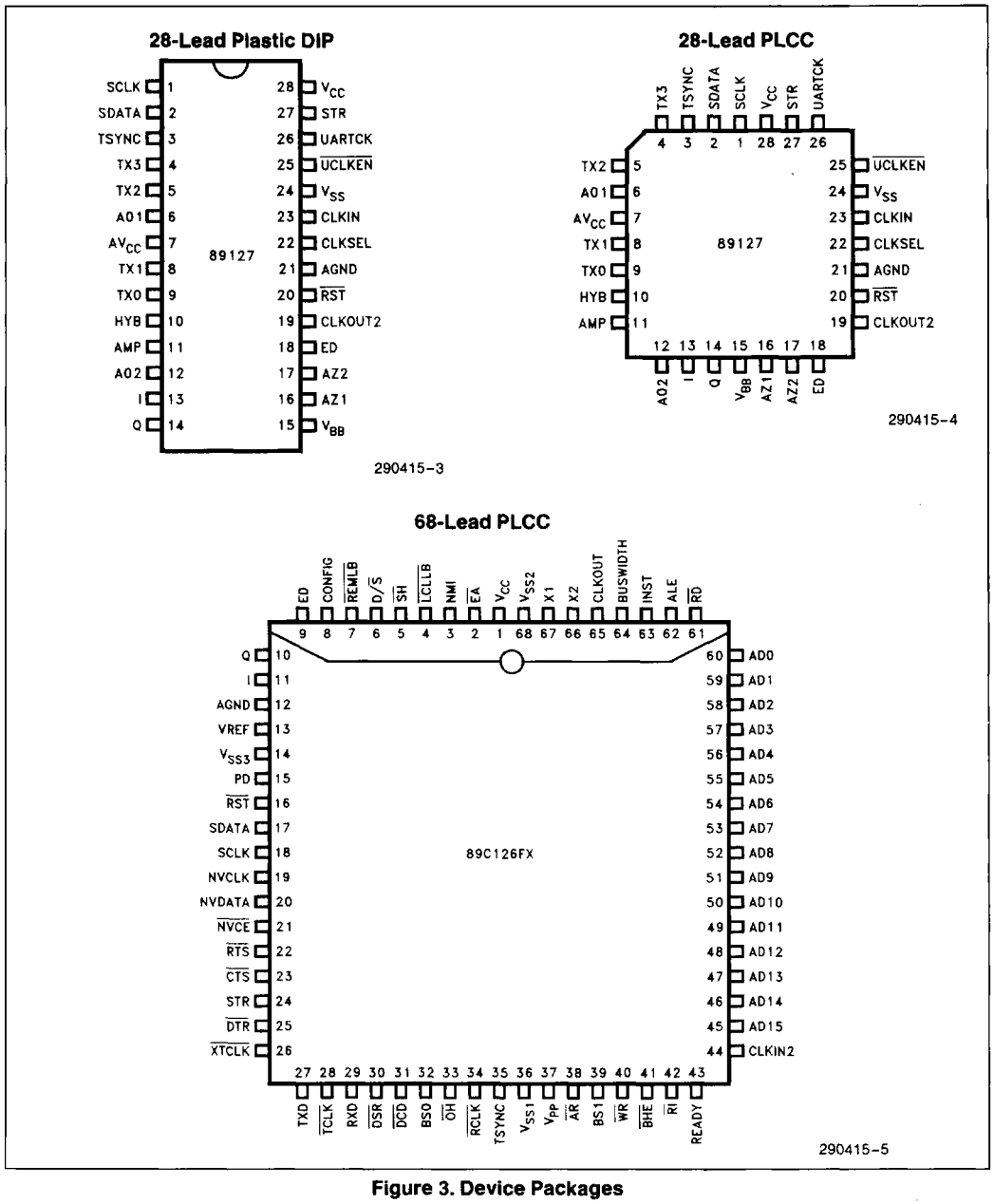
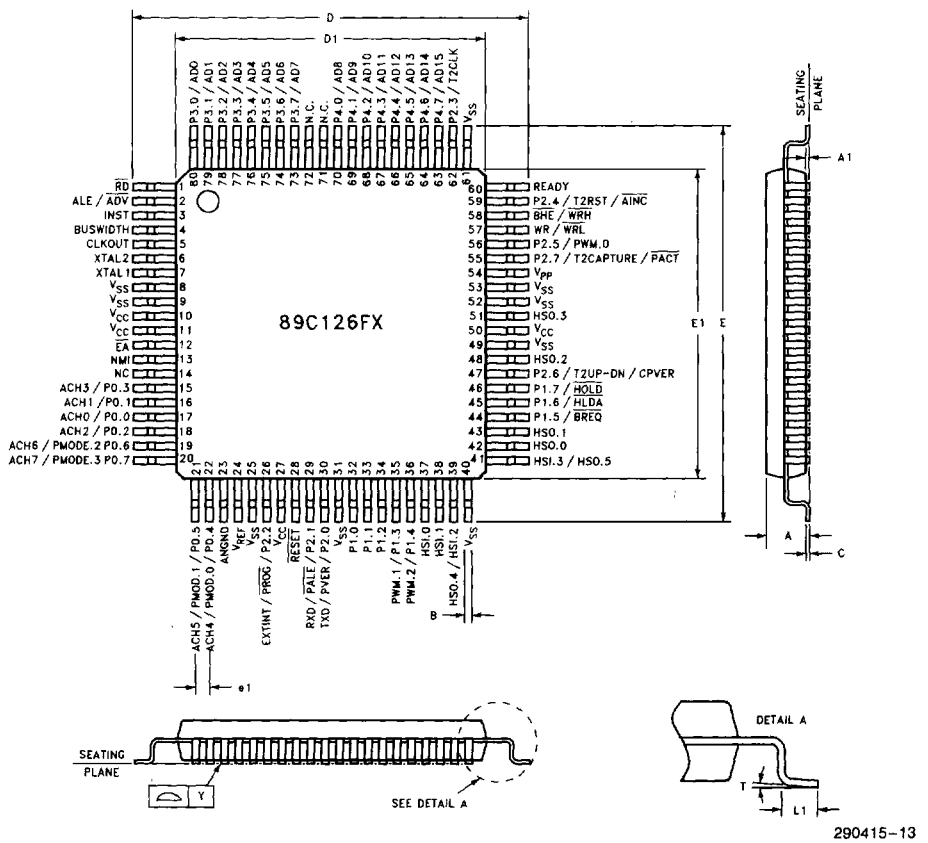


Figure 3. Device Packages

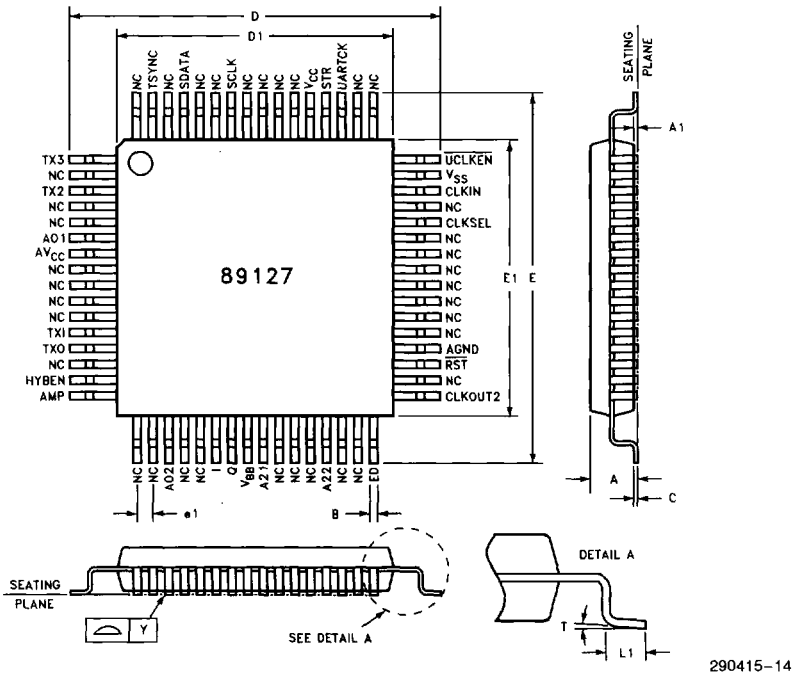
80-LEAD QFP



290415-13

Quad Flatpack Package				
Symbol	Millimeters			
	Minimum	Nominal	Maximum	Notes
A			1.66	
A_1	0.0			
B	0.14	0.20	0.26	
C	0.117	0.127	0.177	
D	13.7	14.0	14.3	
D_1		12.0		
E	13.7	14.0	14.3	
E_1		12.0		
e_1	0.40	0.50	0.60	
L_1	0.30	0.50	0.70	
N		80		Square
T	0.00		10.0	
Y			0.10	
ISSUE	EIAJ			

64-LEAD QFP



Quad Flatpack Package				
Symbol	Millimeters			
	Minimum	Nominal	Maximum	Notes
A			2.55	
A_1	0.0			
B	0.20	0.30	0.40	
C	0.10	0.15	0.20	
D	14.9	15.3	15.7	
D_1		12.0		
E	14.9	15.3	15.7	
E_1		12.0		
e_1	0.53	0.65	0.77	
L_1	0.65	0.85	1.05	
N		64		
T	0.00		10.0	
Y			0.10	
ISSUE	EIAJ			

CALL ESTABLISHMENT, TERMINATION AND RETRAIN (DATA MODEM)

The 89C124FX incorporates all protocols and functions required for automatic or manual call establishment. The modem system also incorporates all protocols and functions required for progress and termination of a data call.

The chip set has a built-in auto-dialer, both DTMF and Pulse type. It can detect dial, busy, and ringback signals from the remote end, and will provide call progress messages to the user. The modem is also capable of re-dialing the last number dialed.

The modem, when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, and then transmit the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be set up by manual dialing. A transition from voice (i.e., for the purpose of manual dialing) to data mode can be done by the use of a mechanical switch (exclusion key) on the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and is compatible with CCITT V.22bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end or by the remote DTE (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests, originated by the remote modem, are of two types (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip set can also be configured to transmit "long-space" just before disconnection.

Because the CCITT and Bell modem connection protocols do not provide recognition of remote modem type (i.e. V.22bis to 212A), the Intel chip set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22bis standard, transparently, to 212A users. Similarly, a user with a 89C124FX based modem system can automatically call data bases with either 212A or V.22bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89C124FX commands and registers that may be used while configuring the data/FAX modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered separately or in string fashion. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the "backspace" key (CNTRL-H) can be used to correct any error. Upper case or lower case characters can be used in the commands.

Table 1. Remote Modem Compatibility

Originating 89C124FX Modem		Answering Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	300	—	300*	300*
	1200	1200*	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	1200*	1200	—	1200	1200
	2400	1200*	1200		1200	2400

Answering 89C124FX Modem		Originating Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	1200	1200
	1200	300	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	300*	1200	—	1200	1200
	2400	300*	1200	—	1200	2400

NOTE:
* These connection data rates are obtained when connecting 89C124FX based modems end to end. The same results may not be obtained when a 89C124FX based modem is connected to other modems.

Data Modem Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn	BELL/CCITT Protocol Compatibility at 300 and 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ;] @)
En	Echo command (En)
Hn	Switch-Hook Control If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn?	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+++	The Default Escape Code
%N	Maximum Line (DCE) Rate
&Cn	DCD Options
&Dn	DTR Options
&Fn	Fetch Factory Configuration Profile
&Gn	Guard Tone
&Jn	Telephone Jack Selection
&Ln	Leased/Dial-up Line Selection
&Mn	Async/Sync Mode Selection
&Pn	Make/Break Pulse Ratio
&Rn	RTS/CTS Options
&Sn	DSR Options
&Tn	Test Commands
&Wn	Write Configuration to Non Volatile Memory
&Xn	Sync Clock Source
&Yn	Default NVRAM Profile Select
&Zn	Store Telephone Number

EIA/TIA-578 FAX Command Set

+FCLASS= <value>	Service Class Selection
+FCLASS?	Read Current Service Class
+FCLASS=?	Read Service Class Capabilities
+FTS=<TIME>	Stop Transmission and Wait
+FRS=<TIME>	Wait for Silence
+FTM=<MOD>	Transmit Data
+FRM=<MOD>	Receive Data
+FTH=<MOD>	Transmit HDLC Data
+FRH=<MOD>	Receive HDLC Data
+FRM/H=?	Read Receive Speed Capabilities
+FTM/H=?	Read Transmit Speed Capabilities

V.42/42bis Feature Control Commands

-Jn	V.42 Detection Phase Control
"Hn	V.42bis Compression Control
"Nn	V.42bis Dictionary Size
"On	V.42bis Dictionary Sizing Length

MNP Feature Control Command Set

\An	Maximum MNP Block Size
%An	Set Auto-Reliable Fallback Character
\Bn	Transmit Break
\Cn	Set Auto-Reliable Buffer
%Cn	Set MNP Compression
\Gn	Set Modem Port Flow Control
\Jn	Bits per Second Rate Adjust
\Kn	Set Break Control
\Nn	Set Operating Mode
\O	Originate Reliable Link
\Qn	Set Serial Port Flow Control
\S	View Active Configuration
\Tn	Set Inactivity Timer
\U	Accept Reliable Link
\Vn	Modify Result Code Form
\Xn	Set XON/XOFF Pass-Through
\Y	Switch to Reliable Mode
\Z	Switch to Normal Mode

Power Down Commands

+En	Disable/Enable Power Down
+Tn	Time to Power Down

CONFIGURATION REGISTERS

The 89C124FX stores all the configuration information in a set of registers. Some registers are dedicated to a special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S0*	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11 *	DTMF Tone Duration
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register
S31 *	Bit Mapped Options Register
S37	Maximum Line (DCE) Rate
S100	Mean Error Monitor Register
S101	FAX Compromise Equalizer Control
S102	Force FAX Transmit and Receive Rates

NOTE:
* These S registers can be stored in the NVRAM.

DIALING

Dial modifiers are available for adding conditions to dialed phone numbers.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
!	Initiate a flash
@	Wait for quiet

Example:

Terminal: AT &Z0 = T 1 (602) 555-1212
Modem: OK

Result: Modem stores the Tone Dial (T) modifier and phone number T16025551212 in the external NVRAM.

The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS0
Modem: T16025551212

Result: Modem dials phone number and attempts to establish a connection.

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

POWER MANAGEMENT

The flexible power management controls allow for a variety of command and hardware driver options. The power-down sequence is initiated by placing a logic "low" on pin 15 ($\overline{PD}$) of the 89C126FX. The laptop or notebook can control the $\overline{PD}$ signal directly. If such a signal is unavailable, $\overline{PD}$ can be controlled by communications software via $\overline{DTR}$. Lack of data activity or an incoming ring signal can also be used to control $\overline{PD}$.

The 89C126FX reduces power consumption by turning off the oscillator. When online and connected to a remote modem, the power consumption for the 89C126FX is typically 530 mW. When the 89127 is not needed (e.g., on-hook, not connected to a remote modem) the 89C126FX places it in idle. In idle, the chip set power consumption is typically 365 mW. In powered down mode, the chip set typically consumes 7 mW. Memory-system power consumption can be minimized by chip selecting memory only when addressed.

APPLICATIONS OVERVIEW

A typical hardware configuration is illustrated in Figure 4 and consists of the following:

- 89C126FX with 21.600 MHz Crystal
- 89127 Analog Front End
- 1 128K x 8 120 ns EPROM (e.g., Intel 27C010-120)
- 1 32K x 8 120 ns SRAM (e.g. 51256-12)
- Bank Switching Logic
- 1K 93C46 Serial EEPROM (Optional)
- Power-Down Logic (Optional)
- Data Access Arrangement (DAA)
- UART (Internal Modem) or Serial Drivers (External Modem)

The DAA section shown in Figure 4 may be implemented using the suggested diagram in Figure 5. Figure 6 shows the use of the power-down feature.

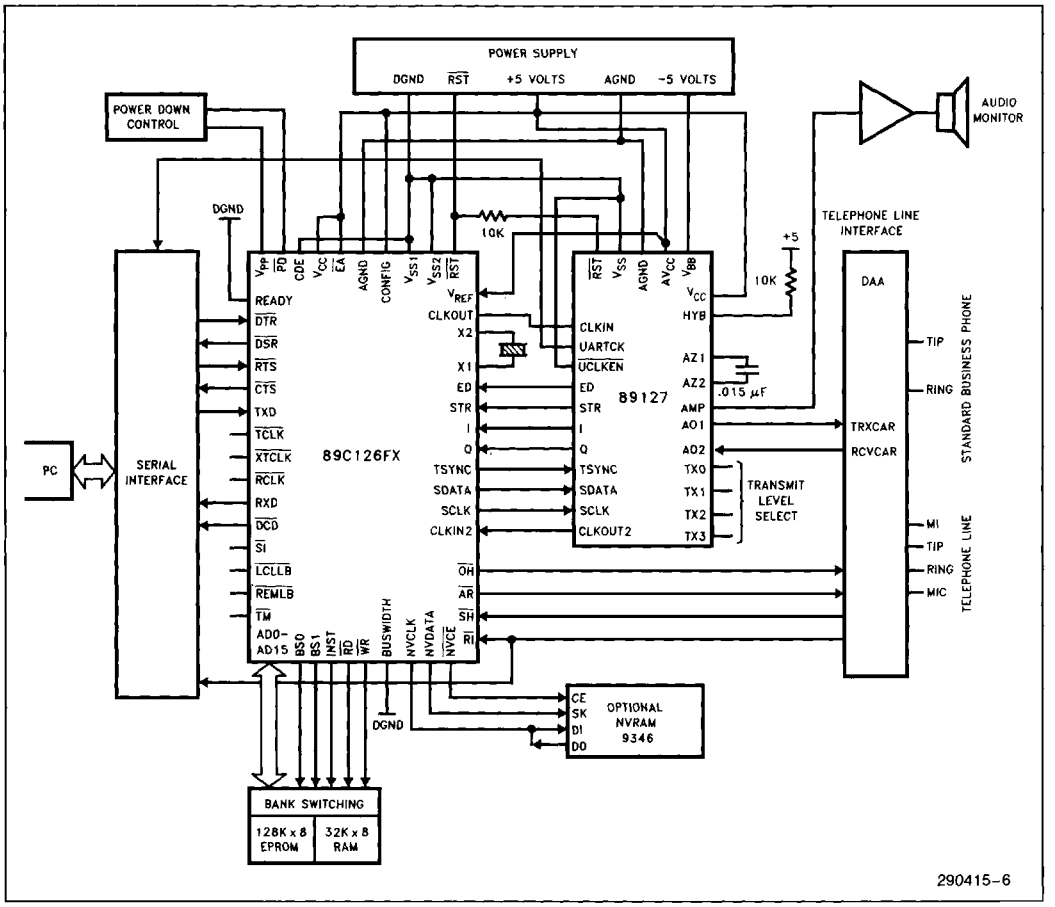


Figure 4. Typical Data FAX Modem

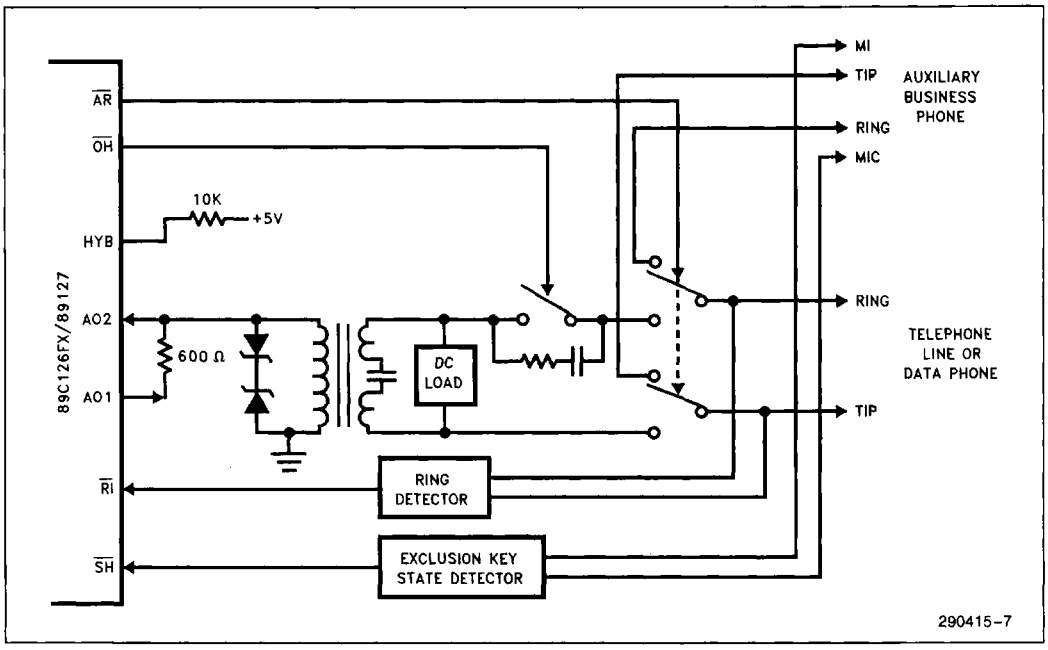


Figure 5. Typical Telephone Line Interface Using Internal Hybrid

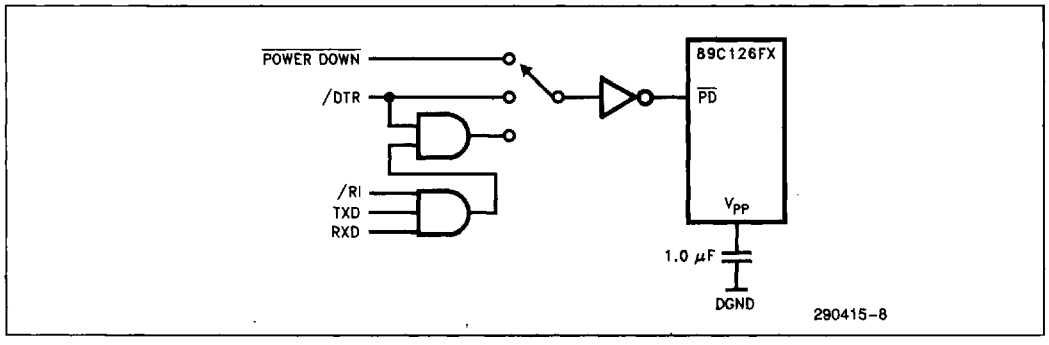


Figure 6. Power-Down Control

SYSTEM COMPATIBILITY SPECIFICATIONS

Specifications at DTE Interface

Parameter	Specification
Direct Mode Synchronous Asynchronous	 2400 bps ±0.01% V.22bis 1200 bps ±0.01% V.22 and BELL 212A 2400, 1200 bps, character async. 0 bps–300 bps anisochronous.
Buffered and Error Correction/Compression Command Modes	9600, 4800, 2400, 1200, 300 bps character asynchronous. (In online command mode, 110 bps and 300 bps only.)
FAX Mode	19,200 bps asynchronous only.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	10 bits, including start, stop, parity. (8, 9, 11 bits optional via software customization.)
Synchronous Timing Source	a) Internal, derived from the local oscillator (default). b) External, provided by DTE through $\overline{\text{XTCLK}}$. c) Slave, derived from the received clock.

Specifications at Telephone Line Interface

Parameter	Specification
Telephone Line Interface	Two-wire full duplex over PSTN, or 4-wire leased lines (modem only). On-chip hybrid and billing delay timer.
Modulation	V.29, QAM at 9600/7200 bps. V.27 ter, PSK at 4800/2400 bps. V.22bis, QAM at 2400 bps. V.22 and Bell 212A, PSK at 1200 bps. V.21 and Bell 103, FSK at 0–300 bps.
Transmit Carrier Frequencies V.29 V.27ter V.22bis, V.22 Bell 212A	 1700 Hz ±1 Hz 1800 Hz ±1 Hz Originate 1200 Hz ±.01% Answer 2400 Hz ±.01%
Transmit Mark and Space Frequencies V.21 Bell 103	 Originate 'space' 1180 Hz ±0.2% Originate 'mark' 980 Hz ±.02% Answer 'space' 1850 Hz ±0.2% Answer 'mark' 1650 Hz ±.02% Originate 'space' 1070 Hz ±.02% Originate 'mark' 1270 Hz ±.02% Answer 'space' 2020 Hz ±.02% Answer 'mark' 2225 Hz ±.02%

Specifications at Telephone Line Interface (Continued)

Parameter	Specification	
Received Carrier Frequency Tolerances		
V.29		1700 Hz ±7 Hz
V.27ter		1800 Hz ±7 Hz
V.22bis, V.22, Bell 212A	Originate	2400 Hz ±7 Hz
	Answer	1200 Hz ±7 Hz
Received Mark and Space Frequency Tolerances		
V.21	Originate 'space'	1850 Hz ±12 Hz
	Originate 'mark'	1650 Hz ±12 Hz
	Answer 'space'	1180 Hz ±12 Hz
	Answer 'mark'	980 Hz ±12 Hz
Bell 103	Originate 'space'	2020 Hz ±12 Hz
	Originate 'mark'	2225 Hz ±12 Hz
	Answer 'space'	1070 Hz ±12 Hz
	Answer 'mark'	1270 Hz ±12 Hz
Typical Energy Detect Sensitivity	> −43 dBm ED is ON. < −48 dBm ED is OFF. Signal measured at AO2.	
Energy Detect Hysteresis	A minimum Hysteresis of 2 dB for QAM scrambled mark.	
Line Equalization	Automatic Adaptive Equalizer for PSK/QAM receive.	

Data Modem Diagnostics

The diagnostics in this section apply only to Data Modem, and not FAX.

Parameter	Specification
Diagnostics Available	Local Analog Loopback. Local Digital Loopback. Remote Digital Loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeroes' and error detector, to be used with most loopbacks. A number indicating the bit errors detected is sent to DTE.

RECEIVER PERFORMANCE SPECIFICATIONS

Test Cases		Typical SNR for 10^{-5} BER Performance	
Data Mode	**Rx Level (dBm)**	**Answer (dB)**	**Originate (dB)**
V.22bis Synchronous	−30	16	16.5
	−40	16.5	18
V.22/Bell 212A Synchronous	−30	6.5	6.5
	−40	6.5	6.5
V.21 Asynchronous	−30	9	7.5
	−40	9	8
Bell 103 Asynchronous	−30	10	11.5
	−40	10	11.5

Test Conditions:

— Receive Signal (Rx) measured at A02 (transmit level set at −9 dBm)

— Unconditioned 3002 Line

— 3 KHz Flat-Band Noise

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		4.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
Default DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10/20		pps	Software Controlled
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	 referenced to High Channel transmit. QAM/PSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec 	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2 	 1.5	 sec 	 Off/On Ratio

89C126FX OVERVIEW

The 89C126FX processor performs data manipulation, signal processing and user interface functions. It requires a single 128K x 8 ROM and 32K x 8 RAM to execute standard, and/or custom code to perform the V.42/42bis, MNP4/5 and FAX protocol functions. A bank switching scheme is used to accommodate the full range of ROM and RAM addresses. Addresses are decoded using the INST, BS0, and BS1 signals. A block diagram of the 89C126FX is provided in Figure 7.

89C126FX contains a TTL compatible serial link to DTE equipment, along with a full complement of V.24/RS-232-C control signals. A UART or USART may be used to transfer data to and from a microcomputer bus. The 89C126FX supports the industry standard AT command set for data modem and EIA/TIA-578 command set for FAX modem functions.

During transmit operation, the 89C126FX synthesizes DTMF tones, 300 BPS FSK signal, and the FAX 9600/7200/4800/2400 bps signals and transmits them to the 89127 as digitized amplitude samples. During 1200 and 2400 BPS operation, DPSK and QAM is used to send 2 to 4 bits of information respectively at 600 baud to the AFE. Because the QAM coding technique is an inherently synchronous transmission mechanism, asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89C126FX transmits digitized phase and amplitude samples to 89127 over the high speed serial link.

In data modem receive operation, the information is received by the 89C126FX from the 89127 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the A/D converter resident on the 89C126FX. DSP algorithms are utilized to implement adaptive equalization, amplitude distortion and gain adjustments, and demodulation. Following demodulation, the data is unscrambled, and if necessary, returned to asynchronous format.

In FAX receive operation, the information is received by the 89C126FX from the 89127 as a filtered and sampled version of the signal on the phone line. The analog signal is digitized by the A/D converter resident on the 89C126FX. DSP algorithms are utilized to implement bandpass filtering, adaptive equalization, and demodulation. Following demodulation, the data is unscrambled.

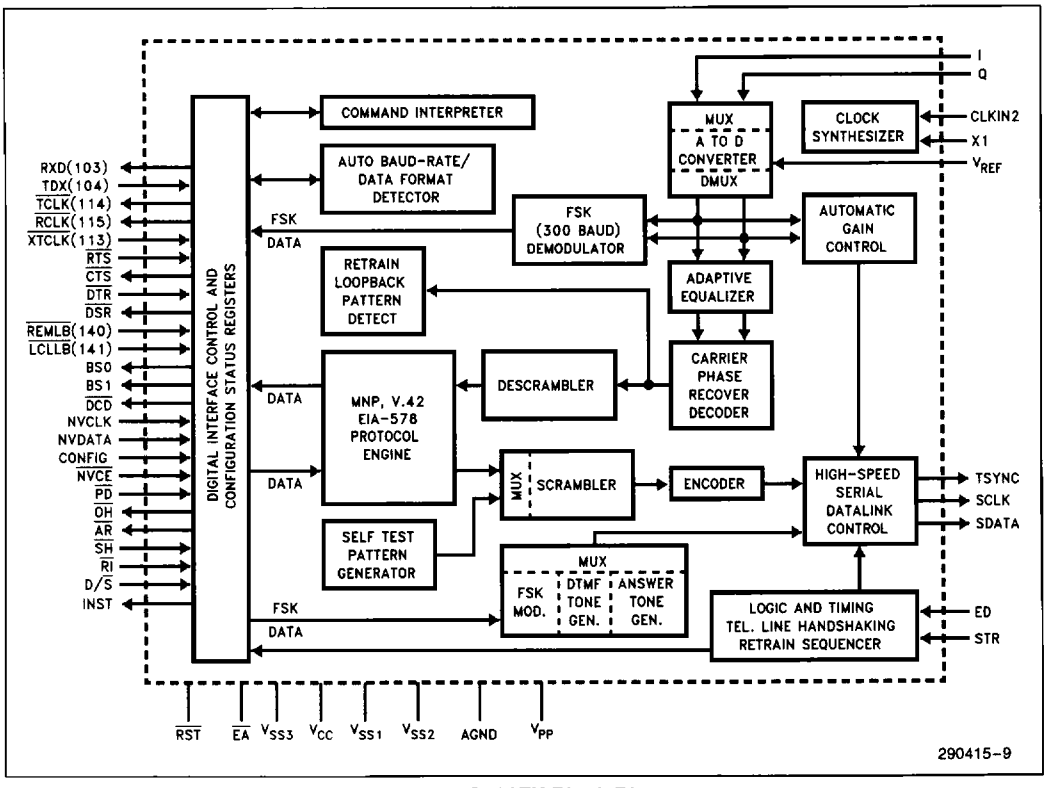


Figure 7. 89C126FX Block Diagram

89C126FX PINOUT

Symbol	Function (89C126FX)	Direction	Pin No.
X1	Crystal Input(2)	In	67
X2	Crystal Output	Out	66
CLKIN2	432 KHz Input from 89127	In	44
CLKOUT	Clock Output to 89127	Out	65
$\overline{RST}$	Chip Reset (Active Low)	In	16
I	In-Phase Received Signal	In	11
Q	Quadrature-Phase Received Signal	In	10
STR	Symbol Timing from 89127	In	24
ED	Energy Detect Input	In	9
TSYNC	Transmitter Sync Pulse to 89127	Out	35
SDATA	Serial Data to 89127	Out	17
SCLK	Serial Clock to 89127	Out	18
$\overline{OH}$	Off-Hook Control to DAA	Out	33
$\overline{SH}$	Switch-Hook from Dataphone	In	5
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay Control to DAA	Out	38
NVDATA	NVRAM Data I/O(1)	I/O	20
NVCLK	NVRAM Clock	Out	19
$\overline{NVCE}$	NVRAM Chip Enable(1)	Out	21
$\overline{PD}$	Power-Down Control	In	15
D/$\overline{S}$	Dumb/$\overline{Smart}$ Mode Select	In	6
CONFIG	Reserved for Future Use (Must be Connected to V_{CC})	In	8
BS0	Bank Select 0(3)	Out	32
BS1	Bank Select 1(3)	Out	39
TXD	Transmitted Data from DTE	In	27
RXD	Received Data to DTE	Out	29
$\overline{RTS}$	Request to Send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received Clock to DTE	Out	34
$\overline{TCLK}$	Transmit Clock to DTE	Out	28
$\overline{XTCLK}$	External Timing Clock from DTE	In	26
$\overline{REMLB}$	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	4
V_{CC}	Positive Power Supply (+5V)	+5V	1
V_{REF}	A/D Converter Reference	+5V	13
V_{SS1}	Digital Ground	GND	36
V_{SS2}	Digital Ground	GND	68
V_{SS3}	Digital Ground(4)	GND	14
AGND	Analog Ground	AGND	12
V_{PP}	Timing Pin for Return from Power-Down	In	37

89C126FX PINOUT

Symbol	Function (89C126FX)	Direction	Pin No.
$\overline{EA}$	External Memory Enable	In	2
AD0–AD15	External Memory Access Address/Data	I/O	60–45
$\overline{AA}$	Auto Answer(5)	Out	60
$\overline{JS}$	Jack Select(5)	Out	59
$\overline{CD}$	Carrier Detect Indicator(5)	Out	58
$\overline{MR}$	Modem Ready Indicator(5)	Out	57
$\overline{REL}$	MNP Reliable Link Active(5)	Out	56
$\overline{COMP}$	Compression Active V.42bis or MNP 5(5)	Out	55
$\overline{ERR}$	Error Detected by LAPM or MNP(5)	Out	54
$\overline{LAPM}$	LAPM Reliable Link Active(5)	Out	53
$\overline{SI}$	Speed Indicator to DTE(5)	Out	60
$\overline{FAX}$	FAX Protocol is Active(5)	Out	59
TM	Test Mode Indicator(5)	Out	58
NMI	Non-Maskable Interrupt	In	3
BUSWIDTH	Bus Width	In	64
INST	External Memory Instruction Fetch	Out	63
ALE	Address Latch Enable	Out	62
$\overline{RD}$	External Memory Read	Out	61
READY	External Memory Ready	In	43
$\overline{BHE}$	External Memory Bus High Enable	Out	41
$\overline{WR}$	External Memory Write	Out	40

NOTES:
1. $\overline{NVCE}$, NVDATA and NVCLK are known as S/A, TCL1, and TCL0, respectively on the 89C024FT. These pins have the same functionality; only the names are different.
2. X1 is known as CLKIN on the 89C024FT, only the naming is different.
3. BS0 and BS1 are known as $\overline{SI}$ and $\overline{TM}$ respectively on the 89C024FT. Their functionality is different. $\overline{SI}$ and $\overline{TM}$ are memory mapped outputs of the 89C124FX.
4. V_{SS3} is known as CDE on the 89C024FT, only the naming is different.
5. These signals are memory mapped, and must be latched externally.

89C126FX PIN DESCRIPTION

$\overline{XTCLK}$

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89C126FX samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$

Clock output from 89C126FX as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. A logic 'high' is mark. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

$\overline{PD}$

Power-down control. A low on this input pin, in conjunction with the +En and +Tn commands, will cause the modem to go into a power-down mode.

V_{PP}

Timing pin for return from power-down. Connect a 1.0 μF capacitor between V_{PP} and V_{SS} if the power-

down option is used. This capacitor causes an internal timing circuit to give the oscillator time to stabilize before turning on internal clocks. This pin may be left floating or connected through a 1.0 μF capacitor to V_{SS} if power-down mode is not required.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation, low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

A low indicates modem is off-hook, is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a low-to-high transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A low-to-high transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

BS0, BS1

Bank Select Pins. These outputs are used by the bank switching logic to generate the MSB address lines for the external ROM.

NVCLK, NVDATA, $\overline{NVCE}$

These pins are used as the serial clock and data for interface to an NVRAM. NVCLK is used to output a clock and serial data is transferred in on NVDATA. $\overline{NVCE}$ is a chip enable for the NVRAM.

$\overline{AR}$

This Auxiliary Relay control is for switching a relay for voice or data calls. High is voice, low is data.

$\overline{RI}$

A low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low sets an off hook condition, high indicates an on hook. When dialing, this signal is used to pulse dial the line.

$\overline{SH}$

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$

A low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins sets the modem to the local digital loopback.

$\overline{REMLB}$

A low on this pin initiates a remote loopback condition.

$\overline{CD}$

A low indicates the presence of carrier signal on the line.

$\overline{MR}$

A low indicates the presence of the DSR signal. Toggling indicates that a test mode is active.

$\overline{REL}$

A low indicates that an MNP reliable link has been established.

$\overline{COMP}$

A low indicates that data compression is in operation (V.42bis or MNP Class 5).

$\overline{LAPM}$

A low indicates that a LAPM reliable link has been established.

$\overline{ERR}$

Goes low for 1 second whenever a reliable connection detects an error.

D/$\overline{S}$

A low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89127 AV_{CC}.

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 Bell) or range of rates. High selects the Low rate or range of rates.

CONFIG

Reserved for future use. This signal should be pulled high.

$\overline{EA}$

When high, memory access from address 2000H to 4000H are directed to on-chip ROM. When low, all Memory access is directed to off-chip memory. This pin must be tied high.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

BUSWIDTH

When high, external memory accesses are 16 bits wide. When low, external memory accesses are 8 bits wide. This pin must be tied low.

READY

When high, no wait states are inserted in external memory accesses. When low, two wait states are inserted in each external memory access.

INST

Output high during an external memory read indicates the read is an instruction fetch. INST is activated only during external memory accesses and output low for data fetch. INST along with AD15 are used to decode the overlapping external ROM and RAM.

$\overline{TM}$

Low indicates maintenance condition in the modem.

$\overline{FAX}$

Low indicates that the modem is off hook in the FAX mode.

89C126FX
Absolute Maximum Ratings*

Ambient Temperature
Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin to V_{SS} . . . . . −0.5V to +7.0V
Power Dissipation 1.5W

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1

Operating Conditions

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25	V
f_{OSC}	Oscillator Frequency	21.5978	21.6022	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

D.C. Characteristics (Over specified operating conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	150		mV	V_{CC} = 5.0V
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA
V_{OH2}	Output High Voltage in RESET on P2.0 (Note 2)	2.0		V	I_{OH} = −0.8 mA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	μA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		±3	μA	0 < V_{IN} < V_{REF}

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.

D.C. Characteristics (Over specified operating conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	V_{IN} = 2.0V
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	V_{IN} = 0.45V
I_{IL1}	AD Bus in Reset			−70	μA	V_{IN} = 0.45V
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 21.6 MHz $V_{CC} = V_{PP} = V_{REF}$ = 5.5V
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	
I_{PD}	Powerdown Mode Current		15	TBD	μA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5V
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	V_{CC} = 5.5V, V_{IN} = 4.0V
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0, and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3, and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

A.C. Characteristics

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} = 21.6 MHz

The system must meet these specifications to work with the 89C124FX:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 68$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 68$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 22$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add $2T_{OSC} * N$, where N = number of wait states.

The 89C124FX will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on $XTAL_1$			MHz	
T_{OSC}	$1/F_{XTAL}$			ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns	
T_{CLCL}	CLKOUT Cycle Time	$2T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	$4T_{OSC}$		ns	(Note 3)
T_{LHLL}	ALE High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC} - 15$			
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC} - 30$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$		ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 23$			(Note 3)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 20$		ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 25$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC} - 10$	$T_{OSC} + 15$	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	$T_{OSC} - 30$		ns	(Note 2)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	$T_{OSC} - 30$		ns	(Note 2)

NOTES:
1. Assuming back-to-back bus cycles.
2. 8-Bit bus only.
3. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

Waveforms

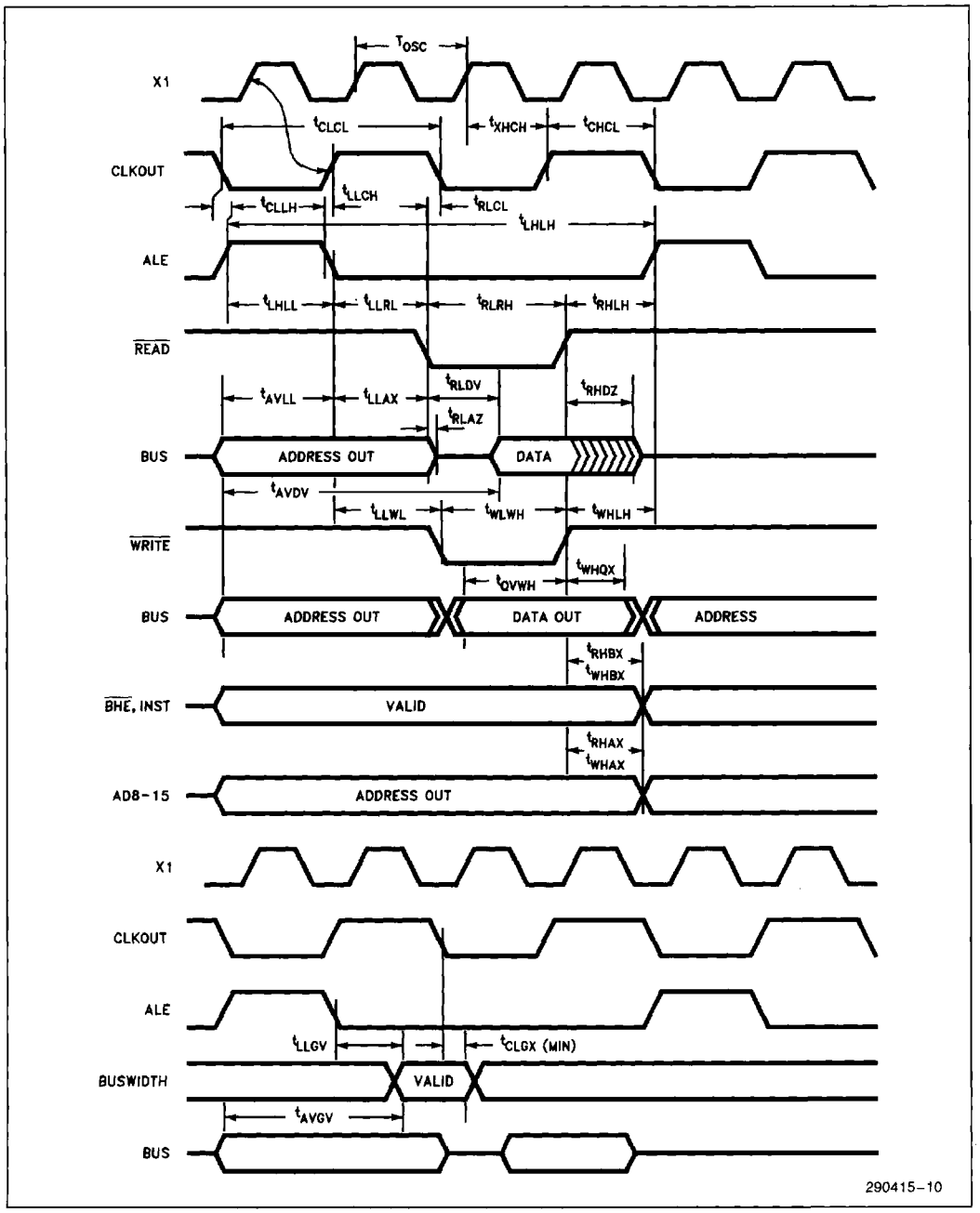


Figure 8. Bus Signal Timings

89127 OVERVIEW

The 89127 is a 28-pin CHMOS analog front end device, which performs most of the complex filtering functions required in data and FAX modem transmitters and receivers. A general block diagram of this chip is provided in Figure 9. Most of the analog signal processing functions in this chip are implemented with CHMOS switched capacitor technology. The 89127 functions are controlled by 89C126FX, through a high speed serial data link.

During FSK and FAX transmit operation, the 89127 receives digitally synthesized information from the 89C126FX. The 89127 converts the signal to its analog equivalents, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89127. This information is modulated onto an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. The 89127 adjusts the signal gain through an on-board programmable gain amplifier before sending it out on the telephone line.

During FAX receive, the signals are passed through anti-alias filters, a bandpass filter, automatic gain control, sample and hold, and the output sent to the 89C126FX processor as an analog signal.

During Data receive operation, the FSK and QAM signals are passed through anti-alias filters, band-split filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89C126FX processor as analog signals.

Other functions provided by the 89127 are: an on-board two-wire to four-wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89127 is available in 28-pin plastic DIP and PLCC packages.

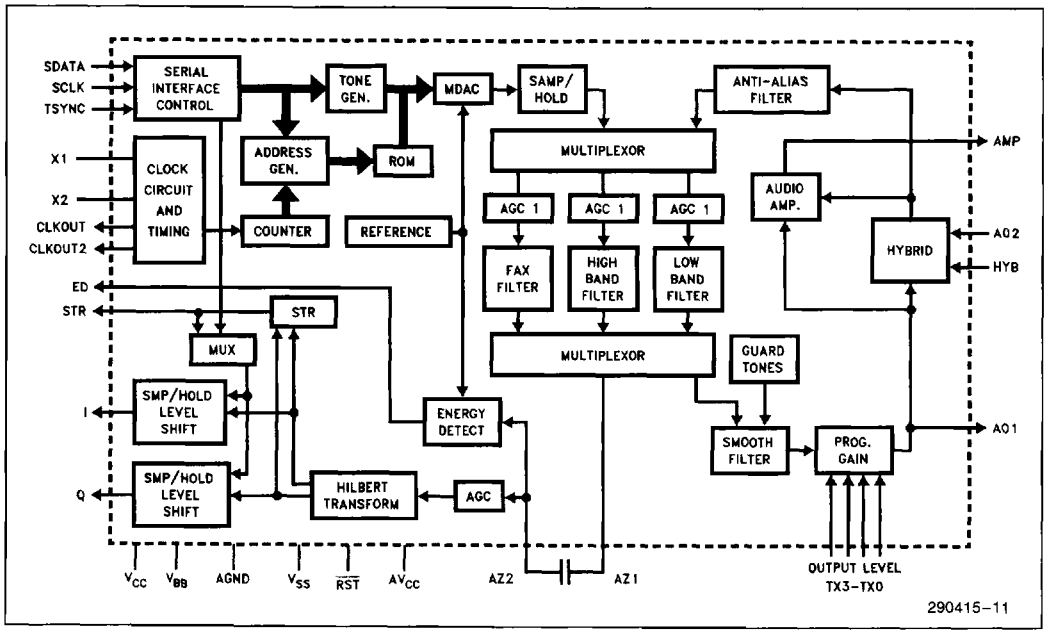


Figure 9. 89127 Block Diagram

89127 PINOUT

Symbol	Function (89127)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
CLKIN	Clock Input(1)	In	23
CLKSEL	Clock Select(2)	In	22
$\overline{UCLKEN}$	UART Clock Enable(3)	In	25
UARTCK	UART Clock(4)	Out	26
CLKOUT2	432 KHz Clock Output to 89C126FX	Out	19
$\overline{RST}$	Chip Reset	In	20
HYB	Enable On-Chip Hybrid	In	10
AZ1	Auto-Zero Capacitor	Out	16
AZ2	Auto-Zero Capacitor	In	17
SDATA	Serial Data from 89C126FX	In	2
SCLK	Serial Clock from 89C126FX	In	1
TSYNC	Transmitter Sync from 89C126FX	In	3
STR	Symbol Timing to 89C126FX	Out	27
ED	Receiver Energy Detect to 89C126FX	Out	18
I	In-Phase Received Signal to 89C126FX	Out	13
Q	Quadrature-Phase Received Signal to 89C126FX	Out	14
AO1	Transmitter Output	Out	6
AO2	Receiver Input	In	12
AMP	Output to Monitor Speaker	Out	11
TX0	Transmitter Level Control (LSB)	In	9
TX1	Transmitter Level Control	In	8
TX2	Transmitter Level Control	In	5
TX3	Transmitter Level Control (MSB)	In	4

NOTES:
1. CLKIN is known as X1 on the 89C024FT, only the naming is different.
2. This pin is a "no connect" on 89C024FT. This is an added function.
3. $\overline{UCLKEN}$ is known as X2 on 89C024FT. Their functionality is different.
4. UARTCK is known as CLOCKOUT on 89C024FT. Their functionality is different.

89127 Pinout Description

CLKIN

Clock Input from 89C126FX.

CLKSEL

Clock Select Pin. GND selects 10.8 MHz clock, V_{BB} selects 6.48 MHz clock.

$\overline{UCLKEN}$

Enables UARTCK when tied low (V_{SS}). If this pin is pulled up, UARTCK is disabled.

UARTCK

Acts as the clock for a UART. Eliminates the need for a crystal on internal Data/FAX modem designs.

CLKOUT2

A 432 KHz clocking signal output that goes to the 89C126FX.

$\overline{RST}$

Active low reset signal. Connect to the controller's $\overline{RST}$ pin.

HYB

Hybrid Enable. A logic high on this pin enables the on-chip hybrid for two-wire telephone line communication. This input, if tied high, must be tied high through a 10K resistor. If HYB is enabled, a line impedance matching network must be connected between AO1 and AO2. If HYB is disabled, and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AZ1, AZ2

Connections for Auto Zeroing Capacitor.

SDATA, SCLK, TSYNC

These pins constitute the serial link used to transmit data from the 89C126FX to the 89127.

AMP

A speaker driver can be connected to this pin, allowing monitoring of call progress tones and operation of the line.

TX0-3

These four pins control the transmitted signal level.

ABSOLUTE MAXIMUM RATINGS(2)

Temperature Under Bias .....0 to +70° C

Storage Temperature .....−40 to +125° C

All Input and Output Voltages with Respect to V_{BB} .....−0.3V to +13.0V

All Input and Output Voltages with Respect to V_{CC} & AV_{CC} .....−13.0V to 0.3V

Power Dissipation 1.35W

Voltage with Respect to V_{SS}(1) .....−0.3V to 6.5V

NOTES:

1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0-TX3 only.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{BB}	Analog Supply Voltage	−4.75	−5.25	V

POWER DISSIPATION Ambient Temp = 0° to 70° C, V_{CC} = AV_{CC} = 5 ±5%, V_{SS} = AGND = 0V.

Symbol	Parameter	Min	Typ	Max	Units
$Aicc_1$	AV_{CC} Operating Current		16.5	25	mA
Icc_1	V_{CC} Operating Current		5.5	7.2	mA
Ibb_1	V_{BB} Operating Current		−16.5	−25.2	mA
$Aicc_s$	AV_{CC} Standby Current		0.2	1.2	mA
Icc_s	V_{CC} Standby Current		5.5	7.2	mA
Ibb_s	V_{BB} Standby Current		−0.7	−2.4	mA
$Aicc_p$	AV_{CC} Power-Down Current		110		μA
Icc_p	V_{CC} Power-Down Current		495		μA
Ibb_p	V_{BB} Power-Down Current		495		μA
Pdo	Operating Power Dissipation		193	300	mW
Pds	Standby Power Dissipation		33	60	mW
Pd_p	Power Down Power Dissipation		7		mW

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89C126FX power supply. Typical Values are for T_A = 25°C and nominal power supply values. V_{CC}, and AV_{CC}. V_{CC}, AV_{CC} and 89C126FX V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: UARTCK

Symbol	Parameter	Min	Max	Units	Test Conditions
Iil	Input Leakage Current	−10	+10	μA	$V_{SS} \leq Vin \leq V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.0	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	Iol ≥ −1.6mA,1 TTL load
Voh	Output High Voltage	2.4		V	Ioh ≤ 50μa, 1 TTL load
Vcol	UARTCK Low Voltage		0.4	V	Load Capacitance = 60 pF
Vcoh	UARTCK High Voltage	0.7 V_{CC}		V	Load Capacitance = 60 pF

1

A.C. CHARACTERISTICS (T_A = 25°C, V_{CC} = AV_{CC} = 5V, V_{SS} = AGND = 0V, V_{BB} = −5V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Receive Signal Level			−9	dBm	Hybrid Enabled
AO2 Input Resistance		10		MOhms	−2.5V<Vin<+2.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±20%
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

CRYSTAL REQUIREMENTS

Parameter	Min	Typ	Max	Units
Frequency Accuracy (0°C–70°C)	−0.0025%	21.600	+0.0025%	MHz
Rx		10	16	Ω
Cx		0.024		pF
Co	5.1	5.6	6.1	pF
Cp		23		pF

NOTES:
1. Crystal Type: Parallel Resonant
2. Crystal manufacturers usually specify the accuracy of a parallel resonant circuit at a given "load capacitance", specified here as Cp, which includes the combination of all capacitances seen at the pins of the crystal. This includes CI, IC pin capacitances, and layout related trace capacitances.
3. Crystal accuracy requirements can be relaxed if layout parasitic capacitances are appropriately considered in the crystal selection.
4. Total capacitance attached to the X1 and X2 pins should not exceed 51 pF each unless Rx Max is decreased.

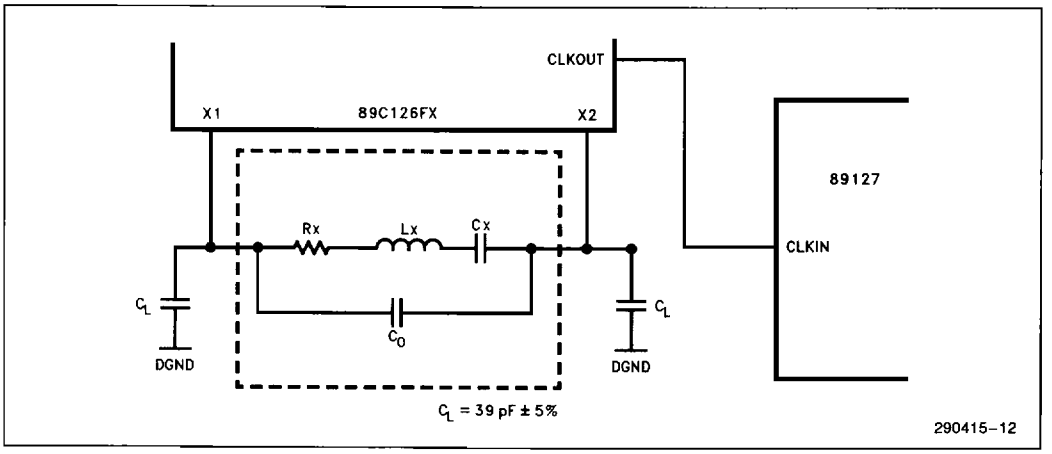


Figure 10. Crystal Equivalent Circuit

ANALOG OUTPUTS: A01, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance AO1 AMP	 600 10			 Ohms kOhms	
Load Capacitance AMP			 100	 pF	
Audio Amp Gain AO1 to Amp		−9 −18 −26 −70		dB dB dB dB	Max Mid (Software Selectable) Min Off
Audio Amp Gain(1) AO2 to Amp		+12 +3 −4 −60		dB dB dB dB	Max Mid (Software Selectable) Min Off

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

SCHEMATICS AND PARTS LIST

The schematics and parts list are for an external data/fax modem design. By adding a UART, the 89C124FX may be used for internal card modem designs. For a schematic of a UART design to interface the 89C124FX to the ISA bus, refer to the Intel Modem Reference Manual, Order Number 296235.

MEMORY ADDRESSING LOGIC

The memory addressing "glue" logic may be implemented using discrete logic gates as in the schematics, or using a PLD (Programmable Logic Device). The equations for using a PLD are as follows:

RAM

$$\overline{CS1} = \overline{AD15} + INST$$

ROM

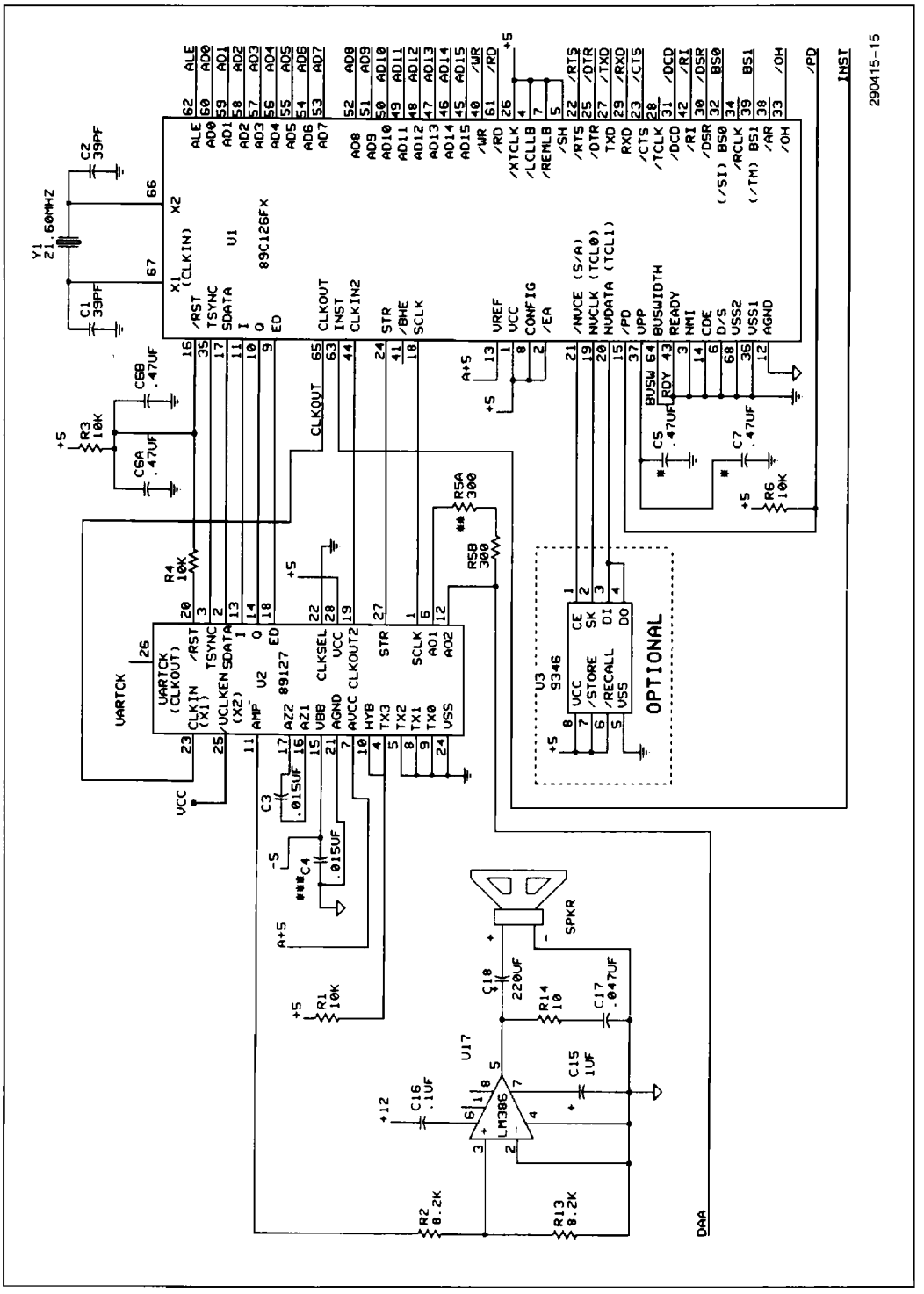
$$\overline{CE} = AD15 \bullet \overline{INST} + AD13 \bullet \overline{AD14} \bullet \overline{AD15}$$

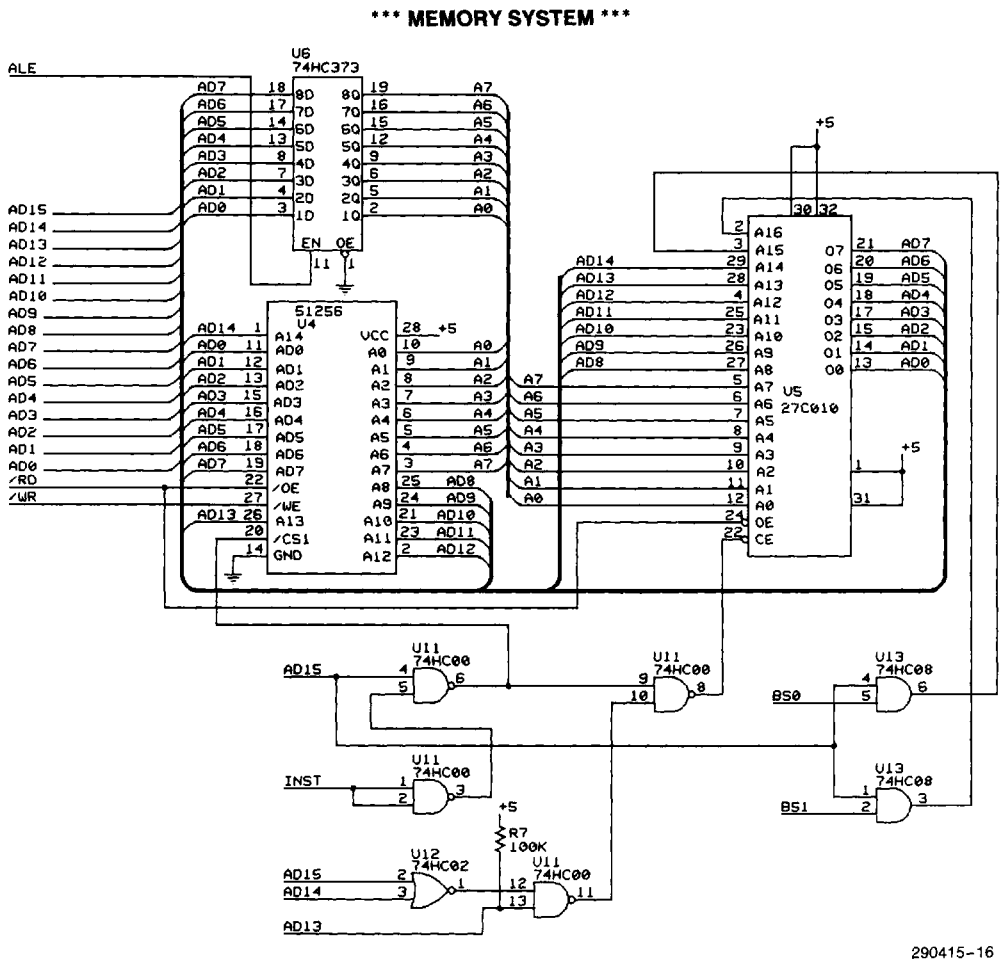
$$A15 = BS0 \bullet AD15$$

$$A16 = BS1 \bullet AD16$$

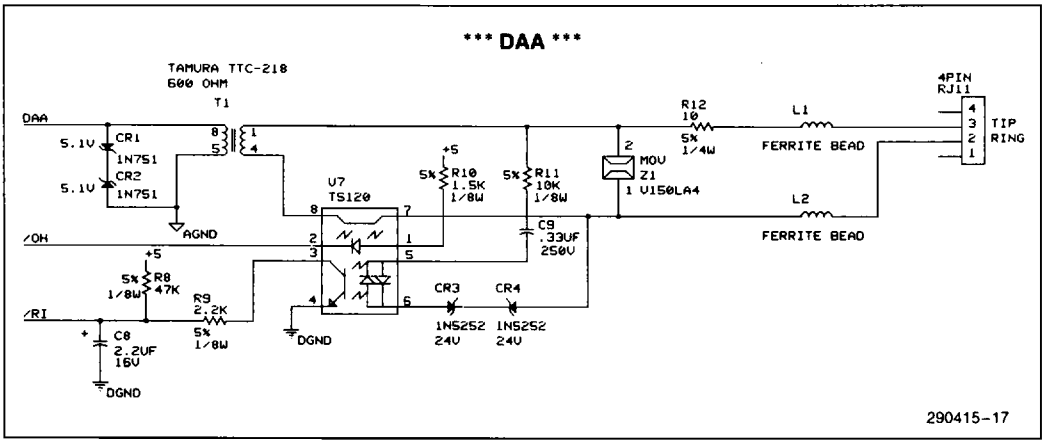
The term $AD13 \bullet \overline{AD14} \bullet \overline{AD15}$ in the $\overline{CE}$ equation disables ROM during internal ROM accesses, and is an optional means for saving power.

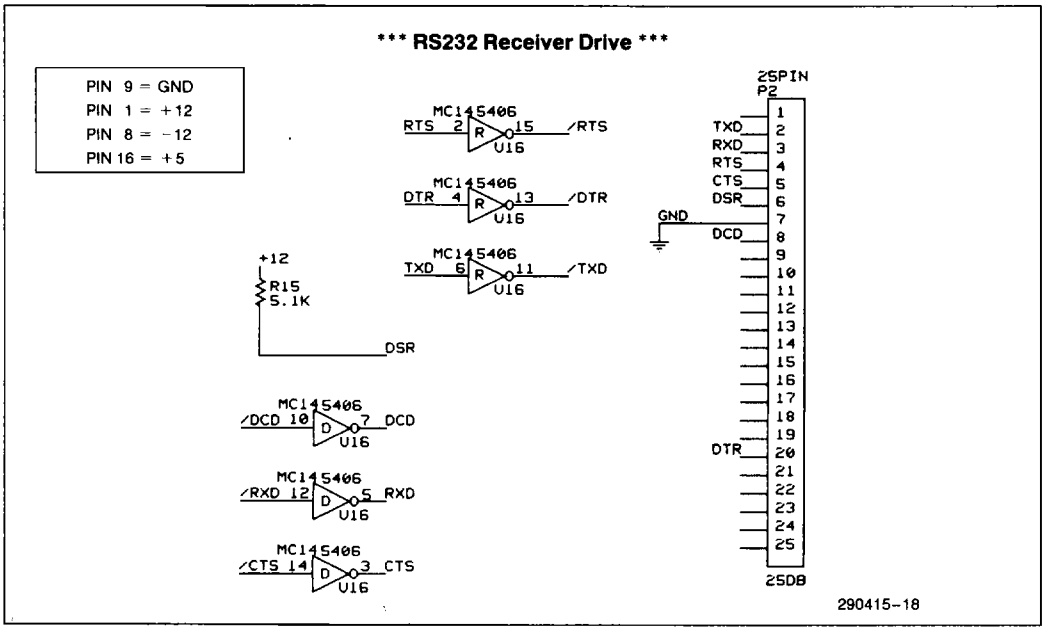
1

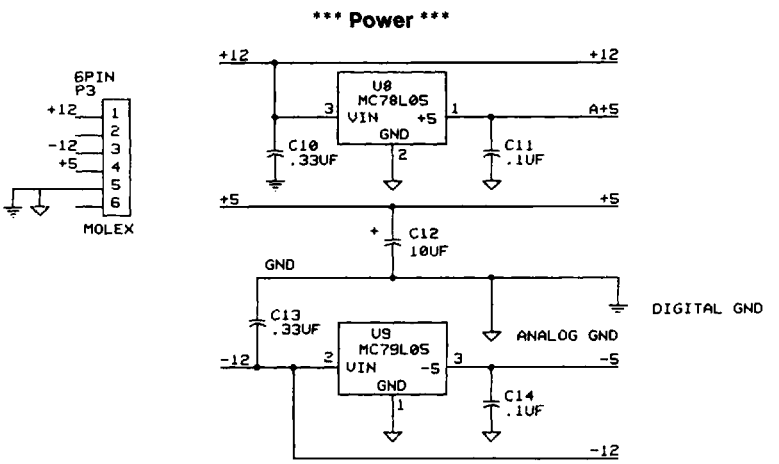

OPTIONAL
SPKR
DAA
INST
290415-15



NOTES:
Tie all spare inputs to GND.
All IC's to be bypassed with 0.1 μF Caps, V_{CC} to GND.

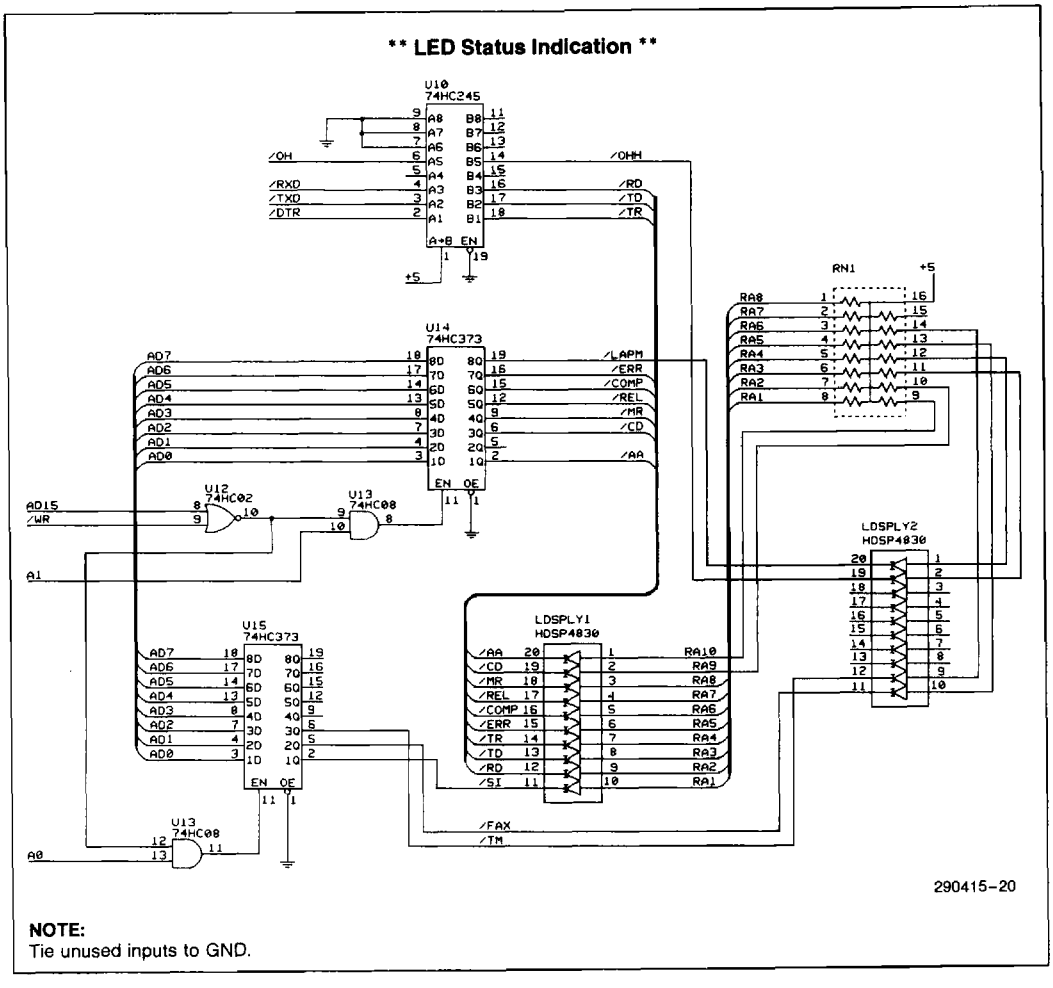

*** DAA ***
TAMURA TTC-218
600 OHM
T1
DAA
5.1V
CR1
1N751
CR2
1N751
AGND
/OH
/RI
+5
R8
47K
R9
2.2K
C8
2.2UF
16V
DGND
U7
TS120
R10
1.5K
1/8W
R11
10K
1/8W
C9
.33UF
250V
CR3
CR4
1N5252
24V
MOV
Z1
1 V150LA4
R12
10
1/4W
L1
L2
FERRITE BEAD
4PIN
RJ11
TIP
RING
290415-17


*** RS232 Receiver Drive ***
PIN 9 = GND
PIN 1 = +12
PIN 8 = -12
PIN 16 = +5
MC145406
RTS
/RTS
DTR
/DTR
TXD
/TXD
U16
+12
R15
5.1K
DSR
/DCD
DCD
/RXD
RXD
/CTS
CTS
25PIN
P2
GND
25DB
290415-18



NOTE:
Mfgr pinouts for regulators vary, this schematic incorporates Motorola parts.

1



NOTE:
Tie unused inputs to GND.

89C124FX External Modem Parts List

Part	Description
U1	Intel 89C126FX Microcontroller
U2	Intel 89127 Analog Front End
U3	93C46 EEPROM 1024-Bit (Optional)
U4	51256 32K x 8 SRAM 120 ns
U5	27C010 128K x 8 ROM 120 ns
U6	74HC373 Octal Transparent Latch
U7	Theta J TS120 Analog Opto Relay
U8	78L05A +5V Regulator
U9	79L05A −5V Regulator
U10	74HC245 Octal Bus Transceiver
U11	74HC00 Quad 2 Input NAND
U12	74HC02 Quad 2 Input NOR
U13	74HC08 Quad 2 Input AND
U14, U15	74HC373 Octal Transparent Latch
U16	MC145406 RS-232 Receiver Driver
C1, C2	39 pF ±5%
C3, C4	0.015 μF
C5, C6A, C6B, C7	0.47 μF
C8	2.2 μF 16V
C9	0.33 μF, 250V. MetalPoly
C10, C13	0.33 μF
C11, C14	0.10 μF
CR1, CR2	1N751A Zener Diode
CR3, CR4	1N5252B Zener Diode
L1, L2	3 Turn Ferrite Bead Inductor
R1, R3, R4, R6, R11	10K 1/8 W
R5A, R5B	300Ω 1/8 Watt 5%
R8	47K, 1/8 W, 5%
R9	2.2K, 1/8 W, 5%
R10	1.5K, 1/8 W, 5%
R12	Fusible Resistor
R15	5.1K, 1/8 W, 5%
RJ11	RJ11 Telephone Jack
P1	Power Connector
P2	DB25 Female 25-Pin Connector
Y1	21.600 MHz XTAL (Crystek Part #013901)
T1	600Ω 1:1 Transformer (TTC-218)
Z1	MOV Surge Protector, V250LA4
SPEAKER CIRCUIT	
U17	LM386
SPKR	Speaker
C15	1 μF
C17	0.047 μF
C18	220 μF
R2, R13	8.2K 1/8 W
C16	0.1 μF
R14	10Ω

89C124FX External Modem Parts List (Continued)

Part	Description
LED CIRCUIT	
U10	74HC245
U14, U15	74HC373
LDSPLY1, LDSPLY2	HDSP4830
RN1	10K RPAK

Transmit Output Level(1)		
TX 3,2,1,0	**Typ**	**Units**
0 0 0 0	+5	dBm
0 0 0 1	+4	dBm
•	•	•
•	•	•
•	•	•
1 1 1 0	−9	dBm
1 1 1 1	−10	dBm

NOTE:
1. For PSK and QAM transmit signal. For FSK transmit signal levels, they are typically 1 dB lower. All signals are measured at A01. The tolerance for the transmit levels is ±1 dBm.

89C024FT CHIP SET USERS

By including a small number of jumpers in the design, one board may be used to implement either an 89C024FT V.42/V.42bis modem, or an 89C124FX Data/FAX modem.

There are 2 pin differences between the 89C126FX and the 89C026FT, as defined below in Table 5.

Table 5. Differences between 89C024FT and 89C126FX

89C026FT Pin	89C126FX Pin	Pin Number
$\overline{SI}$	BS0	32
$\overline{TM}$	BS1	39

On the 89C126FX, $\overline{SI}$ and $\overline{TM}$ are memory mapped.

In addition to the pin redefinitions above, there are name differences between the 89C126FX and the 89C026FT, as specified in Table 6. Note that these are changes in name only, not changes in how these pins are used.

Table 6

89C024FT Name	89C124FX Name	Pin Function	Pin Number
CLKIN	X1	Crystal Input	67
TCL0	NVCLK	NVRAM Clock	19
TCL1	NVDATA	NVRAM Data	20
S/A	$\overline{NVCE}$	NVRAM Chip Enable	21
CDE	V_{SS3}	Digital Ground	14

With the 89C124FX chip set, the system crystal must be connected to the 89C126FX microcontroller. The crystal cannot be connected to the 89127 as it can be with the 89027 AFE. For this reason, the X1 crystal input, pin 23 on the 89027 is renamed CLKIN on the 89127 AFE. The X2 and CLKOUT pins of the 89027 are not needed on the 89127, and are redefined as described in Table 7 below.

Table 7. Differences between 89027 and 89127

89027 Pin	89127 Pin	Pin Number
X2	$\overline{UCLKEN}$	25
CLKOUT	UARTCK	26
N/C	CLKSEL	22

The 89127 Analog Front End produces a clock signal, UARTCK, which replaces the UART crystal required for internal modem designs. UARTCK is enabled via the $\overline{UCLKEN}$ pin.

UARTCK Specifications
Average Frequency is 1.851 MHz ±0.01% (%deviation from 1.8432 MHz is an average of 0.466%)

NOTE:
$\overline{UCLKEN}$ must be tied to V_{SS} to enable UARTCK. If $\overline{UCLKEN}$ is pulled up, UARTCK is disabled.

Reference Documents

The following materials are available to help you with your 89C124FX based design. To obtain these materials, please contact your local Intel Sales Office.

- Modem Hardware Reference Manual (Order Number: 296235)
- Modem Software Reference Manual (Order Number: 296503)
- 89C124FX Design Guide (Order Number: 297161)

The DCA/Intel CAS specification is available through Intel by calling 1-800-538-3373.

The EIA/TIA-578 Asynchronous Facsimile DCE Control Standard specification is available through EIA Standards Sales Department at (202) 457-4966.

89C124FX Revision History

The following differences exist between revision -001 and this version of the datasheet:

1. Schematics and Parts List section and Memory Address Logic Section added.
2. Crystal Specification changed.
3. QFP packaging information added.
4. The address of R. Scott Associates on page 1 has changed.
5. S101 and S102 descriptions have been added to the Configuration Registers Section.
6. Reference Documents section updated.