FAIRCHILD SEMICONDUCTOR™

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# DM74LS193
# Synchronous 4-Bit Binary Counters with Dual Clock

## General Description

The DM74LS193 circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a LOW-to-HIGH level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held HIGH.

The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is LOW. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows.

Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

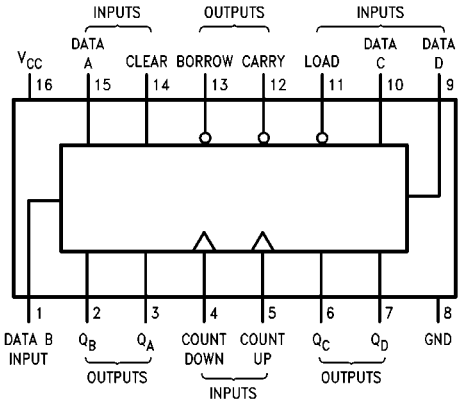
## Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

## Ordering Code:

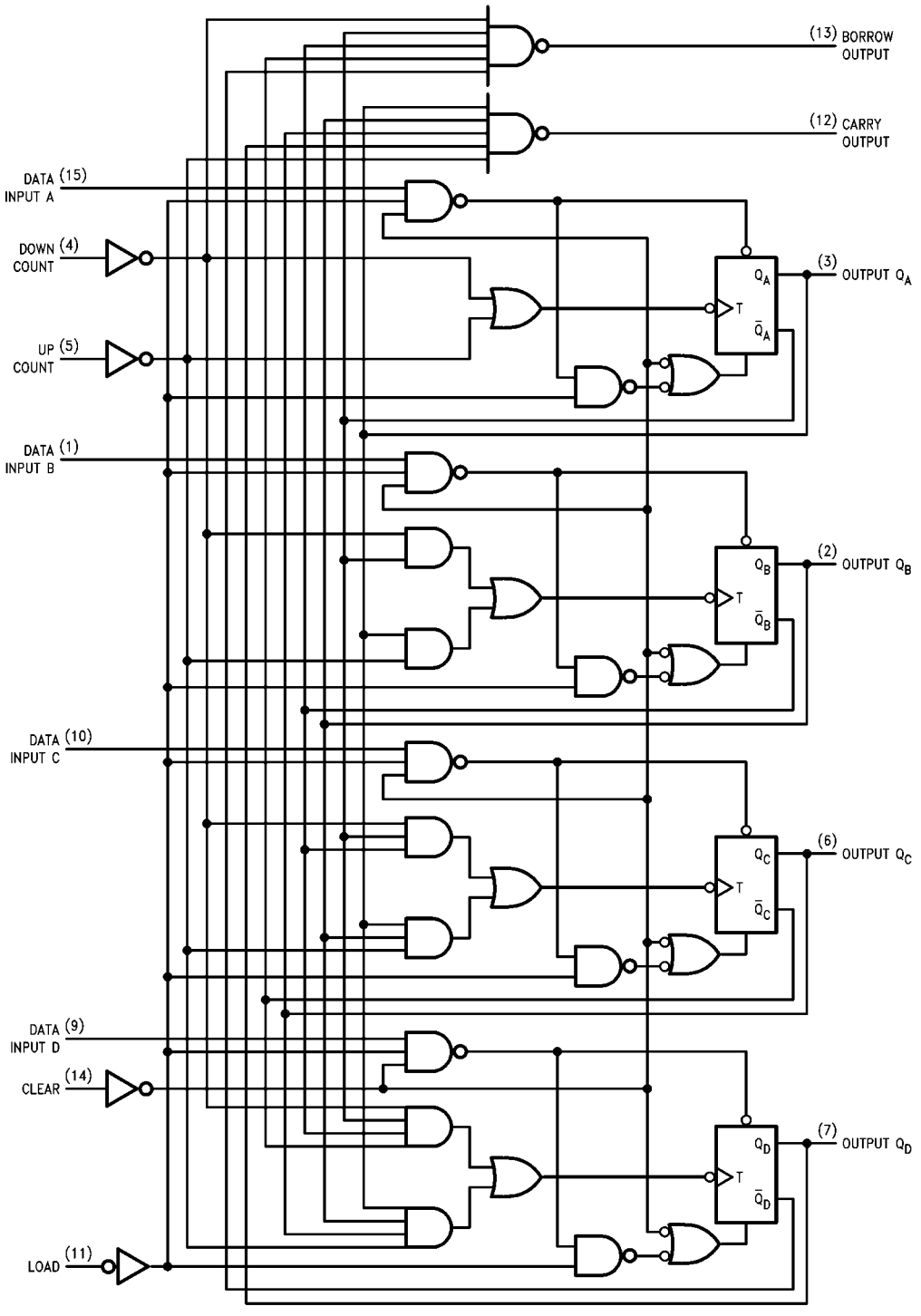
| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS193N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| DM74LS193M | M16A | 16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |

## Connection Diagram

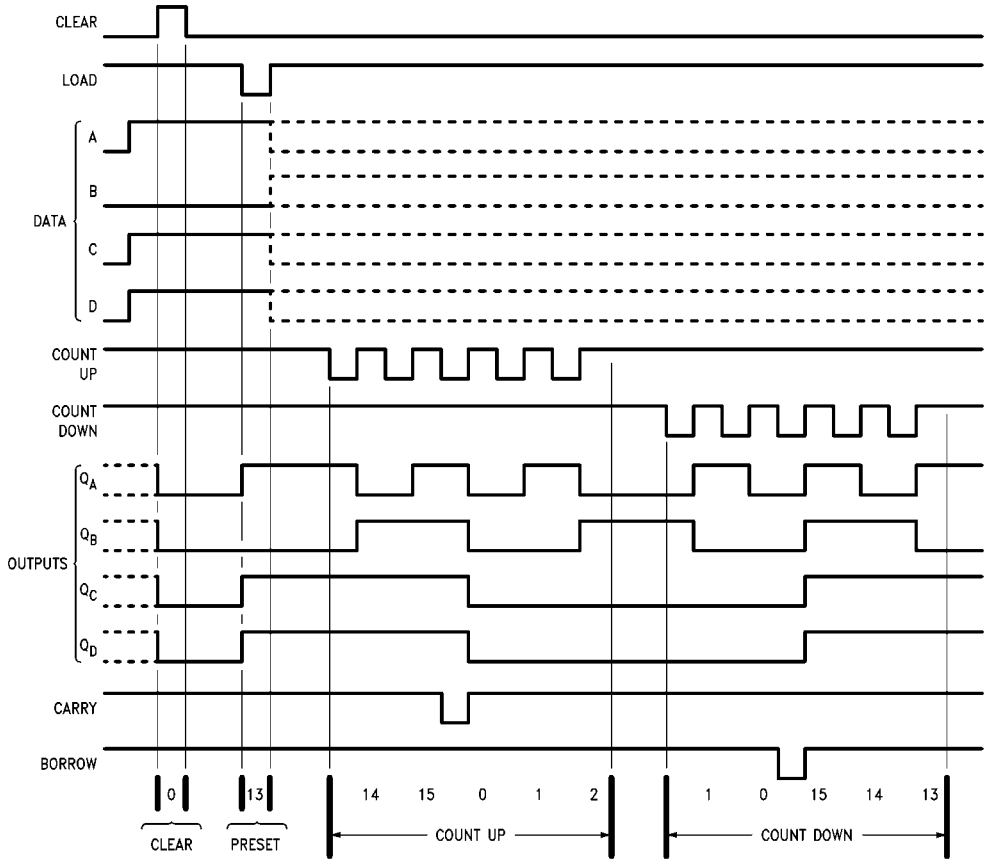


## Logic Diagram



## Timing Diagram




Note A: Clear overrides load, data, and count inputs

Note B: When counting up, count-down input must be HIGH; when counting down, count-up input must be HIGH.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Operating Free Air Temperature Range | –0°C to +70°C |
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Storage Temperature Range | –65°C to +125°C |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the abbsolute maximum ratings. The "Reccommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | –0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | 8 | mA |
| $f_{CLK}$ | Clock Frequency (Note 2) | 0 | | 25 | MHz |
| | Clock Frequency (Note 3) | | | | |
| $t_W$ | Pulse Width of any Input (Note 4) | 20 | | | ns |
| $t_{SU}$ | Data Setup Time (Note 4) | 20 | | | ns |
| $t_H$ | Data Hold Time (Note 4) | 0 | | | ns |
| $t_{EN}$ | Enable Time to Clock (Note 4) | 40 | | | ns |
| $T_A$ | Free Air Operating Temperature | 0 | | 70 | °C |

**Note 2:** $C_L$ = 15 pF, $R_L$ = 2 kΩ, $I_A$ = 25°C and $V_{CC}$ = 5V.

**Note 3:** $C_L$ = 50 pF, $R_L$ = 2 kΩ, $I_A$ = 25°C and $V_{CC}$ = 5V.

**Note 4:** $T_A$ = 25°C and $V_{CC}$ = 5V.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ (Note 5) | Max | Units |
|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = –18 mA | | | –1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max | 2.5 | 3.4 | | V |
| | | $V_{IL}$ = Max, $V_{IH}$ = Min | 2.7 | 3.4 | | |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | | 0.25 | 0.4 | V |
| | | $V_{IL}$ = Max, $V_{IH}$ = Min | | 0.35 | 0.5 | |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = Min | | 0.25 | 0.4 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | | | 20 | µA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | | | –0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max | –20 | | –100 | mA |
| | | (Note 6) | –20 | | –100 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 7) | | 19 | 34 | mA |

**Note 5:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

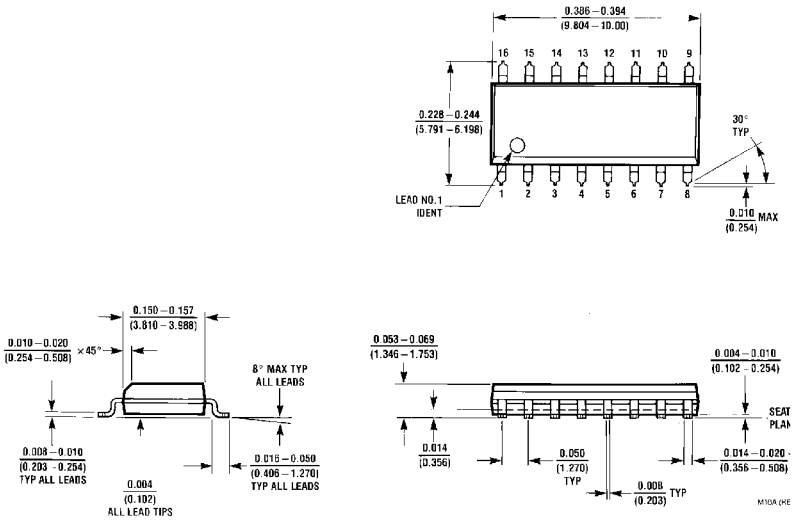
**Note 6:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 7:** $I_{CC}$ is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

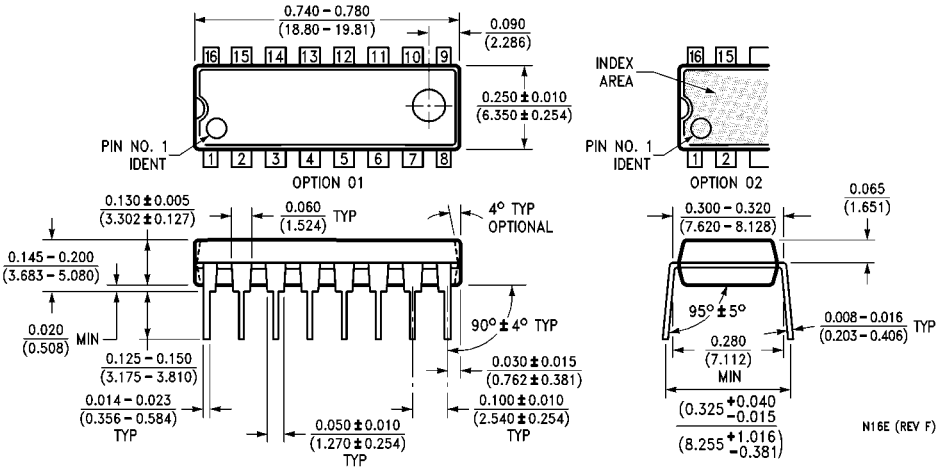
## AC Electrical Characteristics

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2\ k\Omega$ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L = 15$ pF | | $C_L = 50$ pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | 25 | | 20 | | MHz |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Count Up to Carry | | 26 | | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Count Up to Carry | | 24 | | 36 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Count Down to Borrow | | 24 | | 29 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Count Down to Borrow | | 24 | | 32 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Either Count to Any Q | | 38 | | 45 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Either Count to Any Q | | 47 | | 54 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Load to Any Q | | 40 | | 41 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Load to Any Q | | 40 | | 47 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Any Q | | 35 | | 44 | ns |

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Small Outline Integrated Circuit(SOIC), JEDEC MS-012, 0150" Narrow Body**
**Package Number M16A**




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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