

FDS6694

30V N-Channel Fast Switching PowerTrench[®] MOSFET

General Description

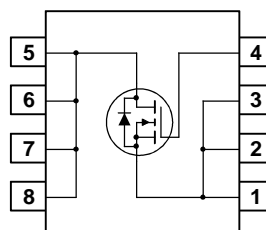
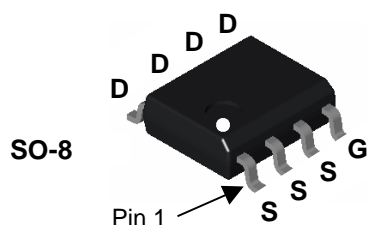
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- DC/DC converter
- Power management
- Load switch

Features

- 12 A, 30 V. $R_{DS(ON)} = 11\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 13.5\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Low gate charge (13 nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability.



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	12	A
	– Pulsed	50	
P_D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.4	
	(Note 1c)	1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Rated	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	125	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6694	FDS6694	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			10	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 12\text{ A}, T_J = 125^\circ\text{C}$		9.1 11.1 12.2	11 13.5 15	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 12\text{ A}$		50		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1293		pF
C_{oss}	Output Capacitance			342		pF
C_{rss}	Reverse Transfer Capacitance			136		pF
R_G	Gate Resistance			0.84		Ω

Switching Characteristics (Note 2)

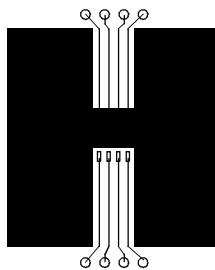
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		9	18	ns
t_r	Turn–On Rise Time			6	12	ns
$t_{d(off)}$	Turn–Off Delay Time			28	45	ns
t_f	Turn–Off Fall Time			10	20	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 5\text{ V}$		13	19	nC
Q_{gs}	Gate–Source Charge			4		nC
Q_{gd}	Gate–Drain Charge			4.7		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			2.1		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.74	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 12\text{ A}, d_F/d_t = 100\text{ A}/\mu\text{s}$		29		nS
Q_{rr}	Diode Reverse Recovery Charge			30		nC

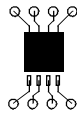
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

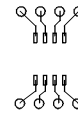


Scale 1 : 1 on letter size paper

a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $105^\circ\text{C}/\text{W}$ when mounted on a $.04\text{ in}^2$ pad of 2 oz copper



c) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

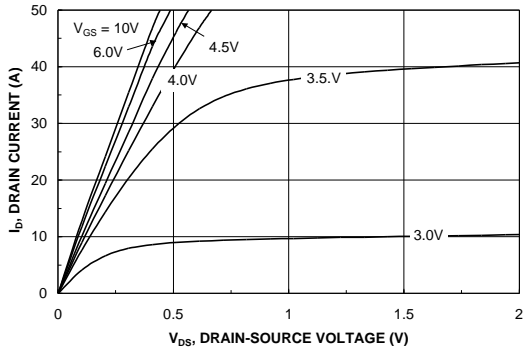


Figure 1. On-Region Characteristics.

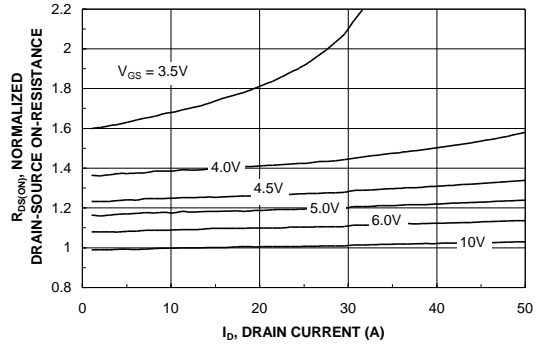


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

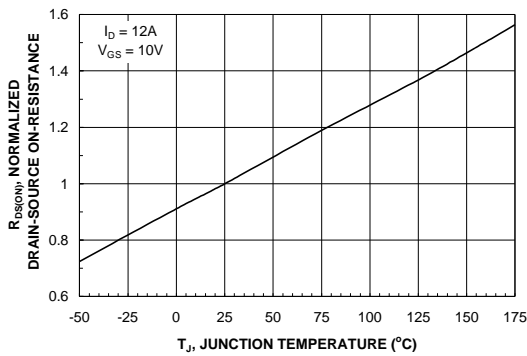


Figure 3. On-Resistance Variation with Temperature.

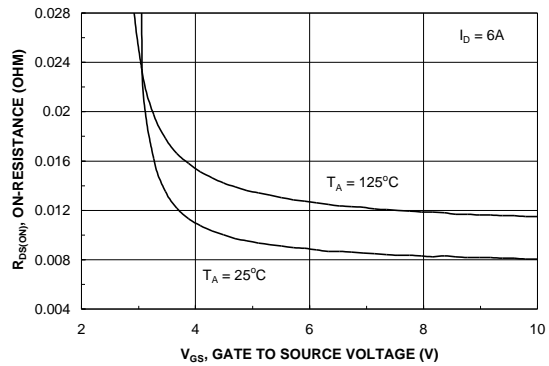


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

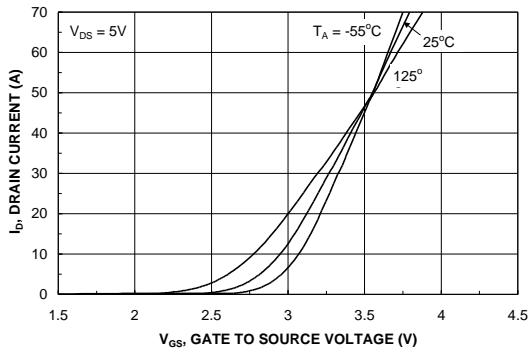


Figure 5. Transfer Characteristics.

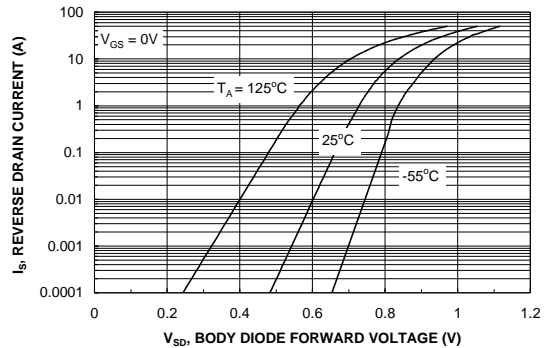


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

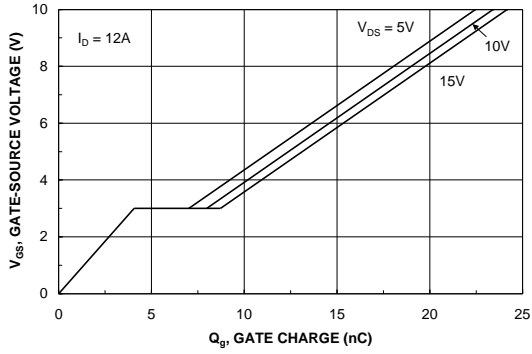


Figure 7. Gate Charge Characteristics.

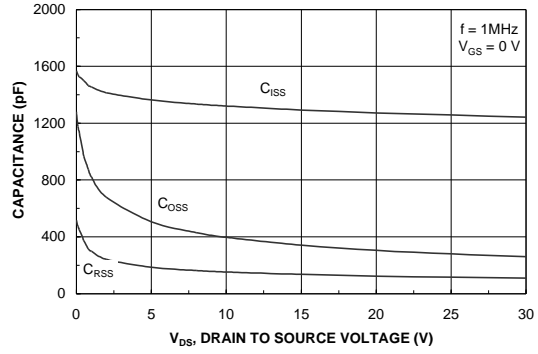


Figure 8. Capacitance Characteristics.

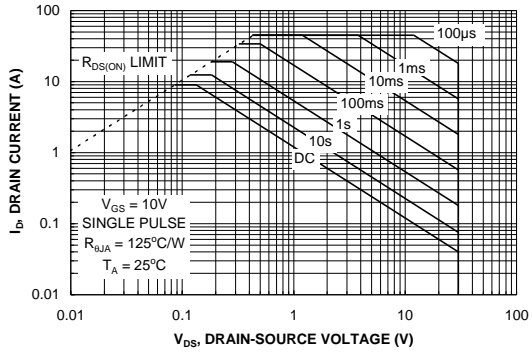


Figure 9. Maximum Safe Operating Area.

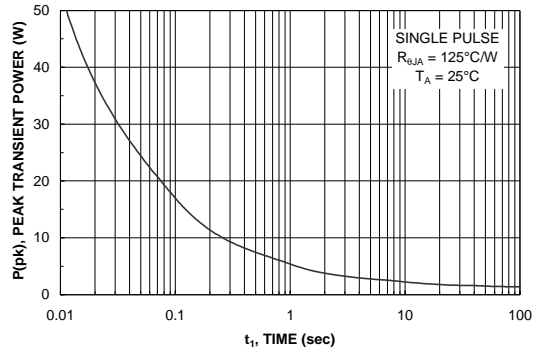


Figure 10. Single Pulse Maximum Power Dissipation.

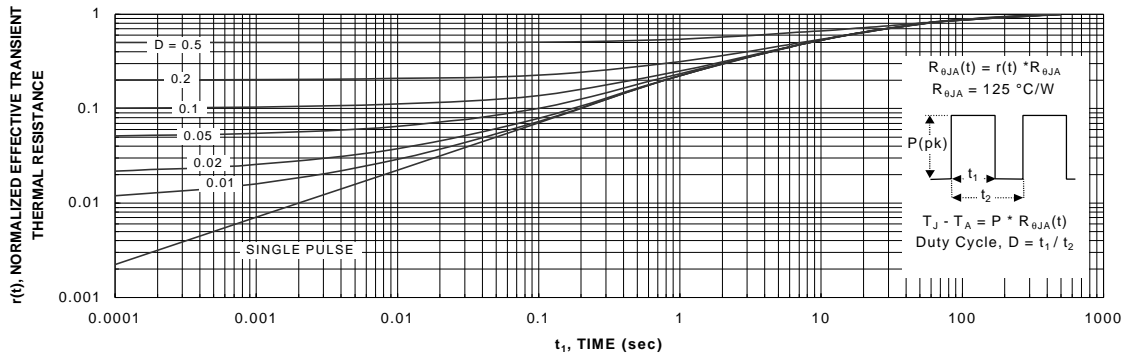


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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CROSSVOLT™	FRFET™	MicroPak™	QS™	SyncFET™
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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General description

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Applications

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Product status/pricing/packaging

BUY

Product	Product status	Pb-free Status	Package type	Leads	Packing method	Package Marking Convention**
FDS6694	Not recommended for new designs		SO-8	8	TAPE REEL	Line 1: \$Y (Fairchild logo) &Z (Asm. Plant Code) &2 (2-Digit Date Code) &T (Die Trace Code) Line 2: FDS Line 3: 6694
FDS6694_NF073	Not recommended for new designs		SO-8	8	TAPE REEL	Line 1: \$Y (Fairchild logo) &Z (Asm. Plant Code) &2 (2-Digit Date Code) &T (Die Trace Code) Line 2: FDS Line 3: 6694



Indicates product with Pb-free second-level interconnect. For more information [click here](#).

Package marking information for product FDS6694 is available. [Click here for more information](#).

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Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
SO-8-8	Electrical	25°C to 125°C	Orcad 9.1	Jul 8, 2003

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Qualification Support

Click on a product for detailed qualification data

Product
FDS6694
FDS6694_NF073

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