THIS SPEC IS OBSOLETE

Spec No: 38-06037

Spec Title: CY7C138 4K X 8/9 DUAL-PORT STATIC RAM WITH SEM , INT, BUSY

Sunset Owner: Adithi Perepu

Replaced by: NONE

CY7C138

4K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

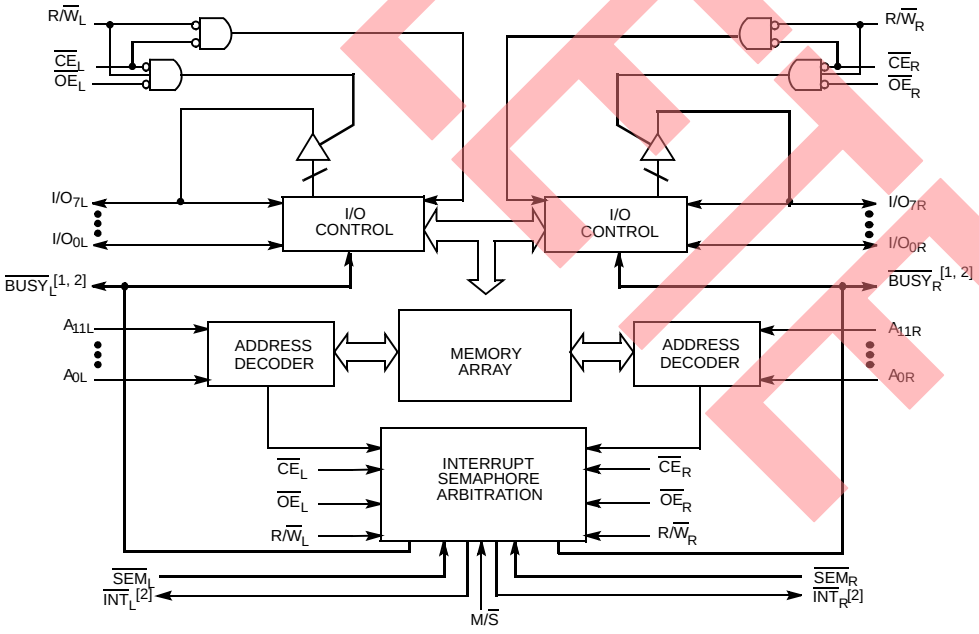
- True dual-ported memory cells that enable simultaneous reads of the same memory location
- 4K x 8 organization (CY7C138)
- 0.65-micron complementary metal oxide semiconductor (CMOS) for optimum speed and power
- High speed access: 25 ns
- Low operating power: I_{CC} = 160 mA (max.)
- Fully asynchronous operation
- Automatic power-down
- Transistor transistor logic (TTL) compatible
- Expandable data bus to 32 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flag for port-to-port communication
- Available in 68-pin plastic leaded chip carrier (PLCC)
- Pb-free packages available

Functional Description

The CY7C138 is a high speed CMOS 4K x 8 dual-port static RAM. Various arbitration schemes are included on the CY7C138 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C138 can be used as a standalone 8-bit dual-port static RAM or multiple devices can be combined to function as a 16-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 16-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

Logic Block Diagram



Notes
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Interrupt: push-pull output and requires no pull-up resistor.

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Pin Configurations

Figure 1. 68-Pin PLCC (Top View)

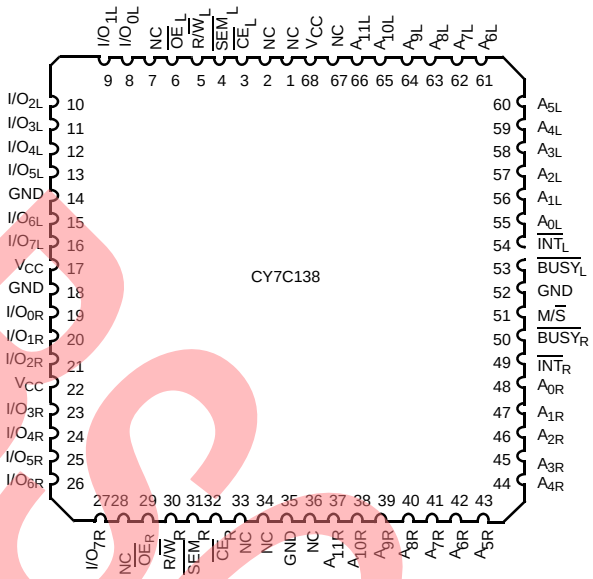


Table 1. Pin Definitions

Left Port	Right Port	Description
$I/O_{0L–7L}$	$I/O_{0R–7R}$	Data bus input/output
$A_{0L–11L}$	$A_{0R–11R}$	Address lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag. $\overline{INT}_L$ is set when right port writes location FFE and is cleared when left port reads location FFE. $\overline{INT}_R$ is set when left port writes location FFF and is cleared when right port reads location FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
M/S		Master or slave select
V_{CC}		Power
GND		Ground

Table 2. Selection Guide

Description		7C138-25	Unit
Maximum access time (ns)		25	ns
Maximum operating current	Commercial	180	mA
Maximum standby current for I_{SB1}	Commercial	40	mA

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[3]

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z state .....–0.5 V to +7.0 V

DC input voltage[4].....–0.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics Over the Operating Range

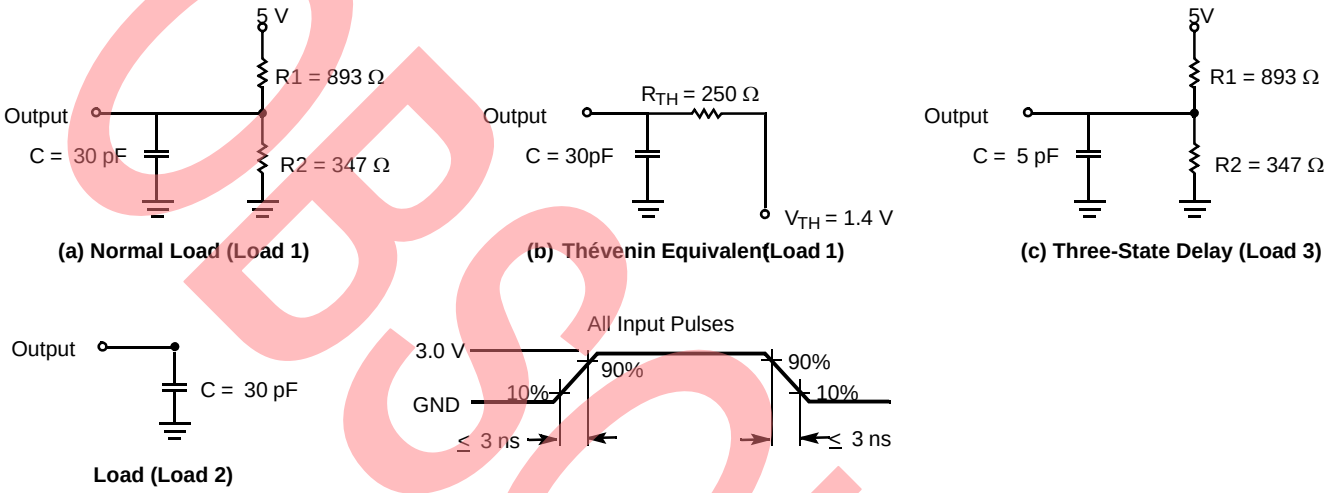
Parameter	Description	Test Conditions		7C138-25 Min	7C138-25 Max	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min., I_{OL} = 4.0 mA		–	0.4	V
V_{IH}				2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–10	+10	µA
I_{OZ}	Output leakage current	Output disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	µA
I_{CC}	Operating current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs disabled	Commercial	–	180	mA
			Industrial	–	190	
I_{SB1}	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Commercial	–	40	mA
			Industrial	–	50	
I_{SB2}	Standby current (One port TTL level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Commercial	–	110	mA
			Industrial	–	120	
I_{SB3}	Standby current (Both ports CMOS levels)	Both ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0[5]	Commercial	–	15	mA
			Industrial	–	30	
I_{SB4}	Standby current (One port CMOS level)	One port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, Active Port outputs, f = f_{MAX}[5]	Commercial	–	100	mA
			Industrial	–	115	

Notes
3. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
4. Pulse width < 20 ns.
5. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}

Capacitance[6]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		15	pF

Figure 2. AC Test Loads and Waveforms



(a) Normal Load (Load 1) (b) Thévenin Equivalent (Load 1) (c) Three-State Delay (Load 3)

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C138-25		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read cycle time	25	–	ns
t_{AA}	Address to data valid	–	25	ns
t_{OHA}	Output hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	25	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	15	ns
t_{LZOE}[8,9,10]	$\overline{OE}$ Low to Low Z	3	–	ns
t_{HZOE}[8,9,10]	$\overline{OE}$ HIGH to High Z	–	15	ns
t_{LZCE}[8,9,10]	$\overline{CE}$ LOW to Low Z	3	–	ns
t_{HZCE}[8,9,10]	$\overline{CE}$ HIGH to High Z	–	15	ns
t_{PU}[10]	$\overline{CE}$ LOW to Power-up	0	–	ns
t_{PD}[10]	$\overline{CE}$ HIGH to Power-down	–	25	ns
WRITE CYCLE				
t_{WC}	Write cycle time	25	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	20	–	ns

Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any temperature and voltage condition for any device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3
10. This parameter is guaranteed but not tested.

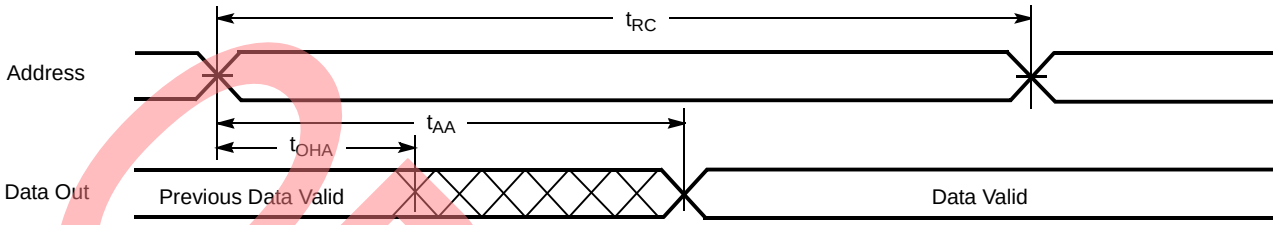
Switching Characteristics Over the Operating Range[7] (continued)

Parameter	Description	7C138-25		Unit
		Min	Max	
t_{AW}	Address setup to write end	20	–	ns
t_{HA}	Address hold from write end	2	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	Write pulse width	20	–	ns
t_{SD}	Data setup to write end	15	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}[11,12]	R/$\overline{W}$ LOW to High Z	–	15	ns
t_{LZWE}[11,12]	R/$\overline{W}$ HIGH to Low Z	3	–	ns
t_{WDD}[13]	Write pulse to data delay	–	50	ns
t_{DDD}[13]	Write data valid to read data valid	–	30	ns
BUSY TIMING[14]				
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch	–	20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	20	ns
t_{PS}	Port setup for priority	5	–	ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20	–	ns
t_{BDD}[15]	$\overline{BUSY}$ HIGH to data valid	–	Note 15	ns
INTERRUPT TIMING[14]				
t_{INS}	$\overline{INT}$ set time	–	25	ns
t_{INR}	$\overline{INT}$ reset time	–	25	ns
SEMAPHORE TIMING				
t_{SOP}	SEM flag update pulse ($\overline{OE}$ or $\overline{SEM}$)	10	–	ns
t_{SWRD}	SEM flag write to read time	5	–	ns
t_{SPS}	SEM flag contention window	5	–	ns

Notes
11. Test conditions used are Load 3.
12. This parameter is guaranteed but not tested.
13. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
14. Test conditions used are Load 2.
15. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Switching Waveforms

Figure 3. Read Cycle No. 1 (Either Port Address Access)[16, 17]



Notes
16. R/$\overline{W}$ is HIGH for read cycle.
17. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads

Switching Waveforms (continued)

Figure 4. Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[18, 19, 20, 21]

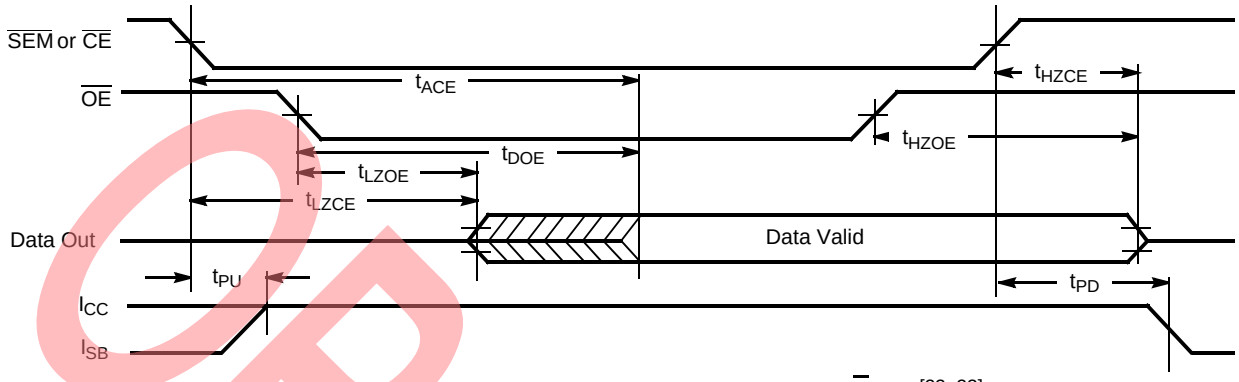
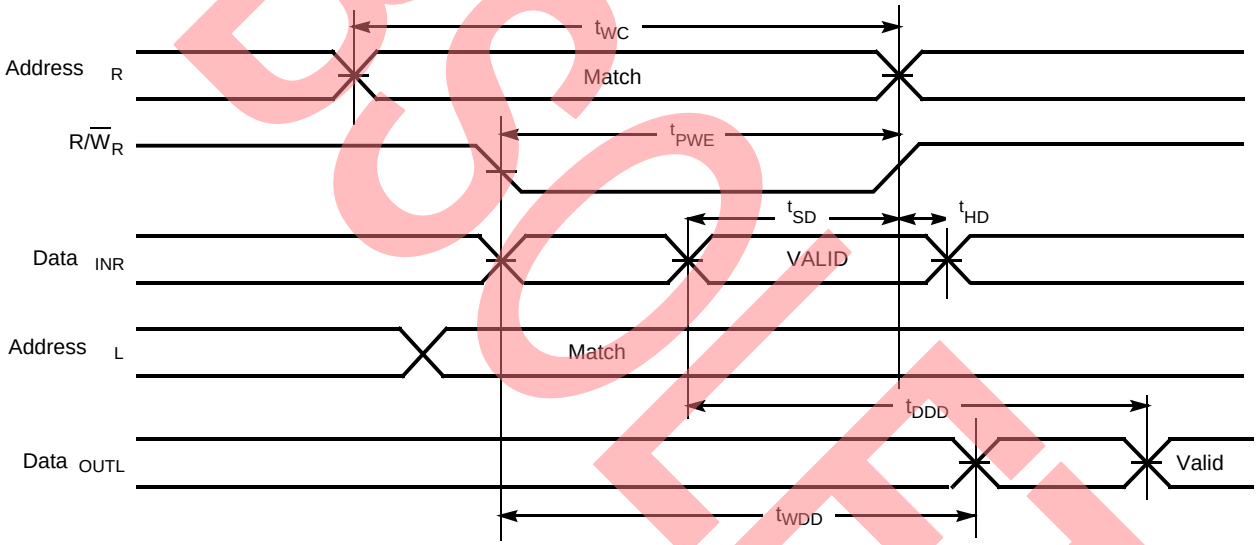


Figure 5. Read Timing with Port-to-Port Delay (M/$\overline{S}$ = L)[22, 23]



Notes
18. R/$\overline{W}$ is HIGH for read cycle.
19. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
21. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
22. $\overline{BUSY}$ = HIGH for the writing port.
23. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[24, 25, 26]

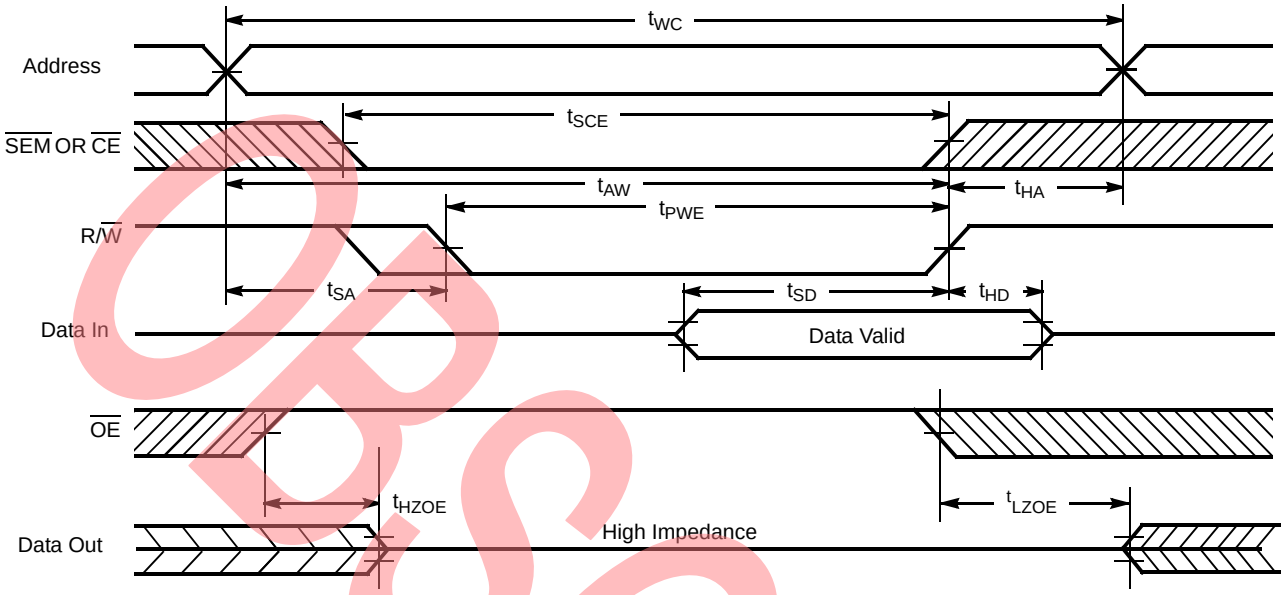
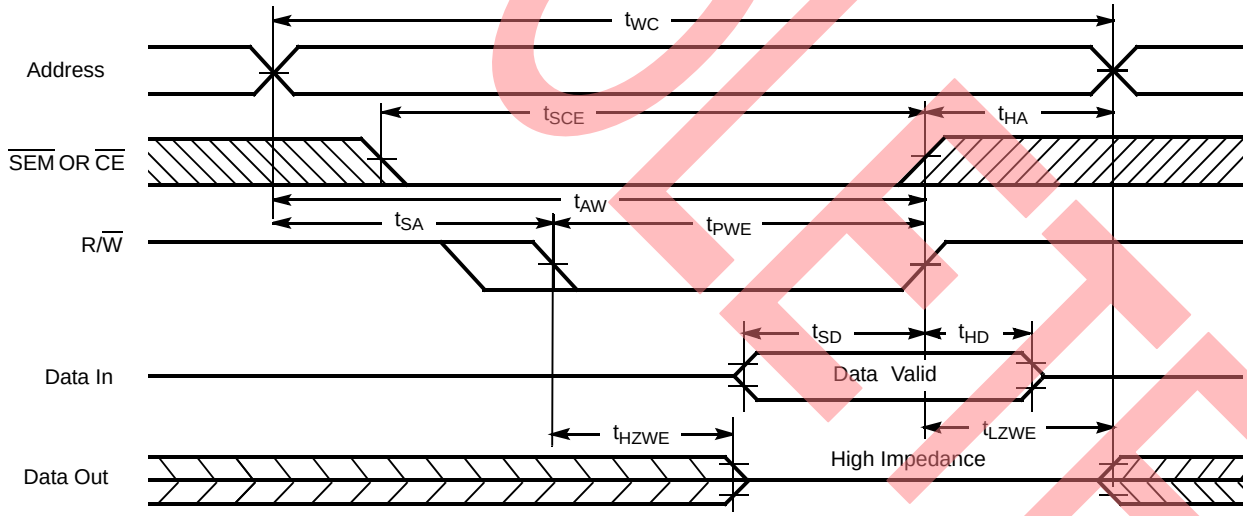


Figure 7. Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[24, 26, 27]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
25. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/W controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
26. R/$\overline{W}$ must be HIGH during all address transitions.
27. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Figure 8. Semaphore Read After Write Timing, Either Side[28]

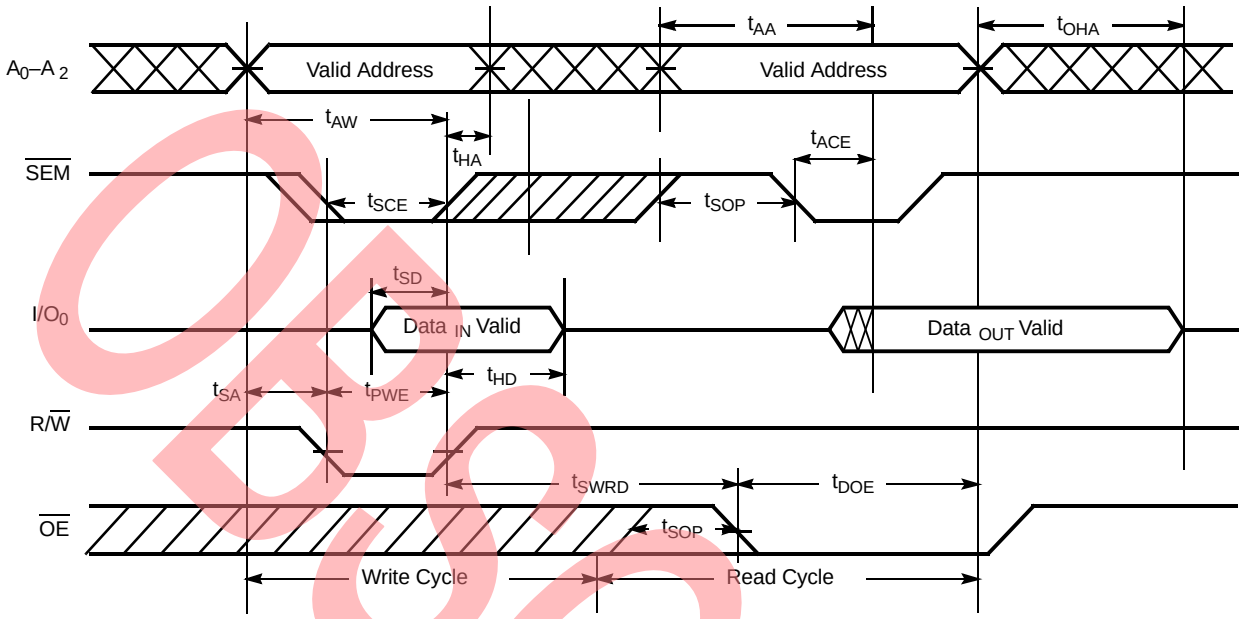
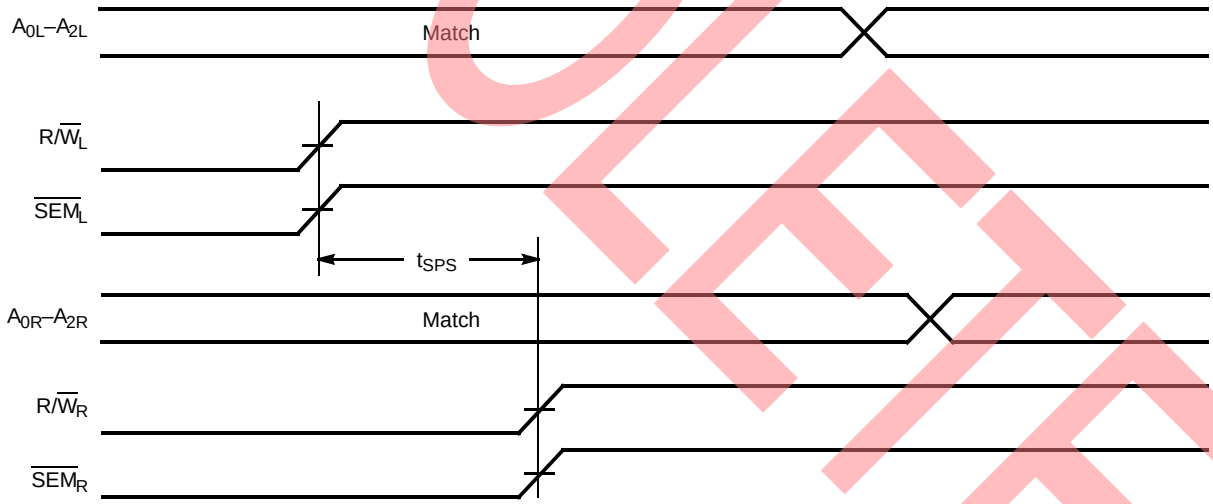


Figure 9. Timing Diagram of Semaphore Contention[29, 30, 31]



Notes
28. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
29. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
30. Semaphores are reset (available to both ports) at cycle start.
31. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Figure 10. Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$ = HIGH)[32]

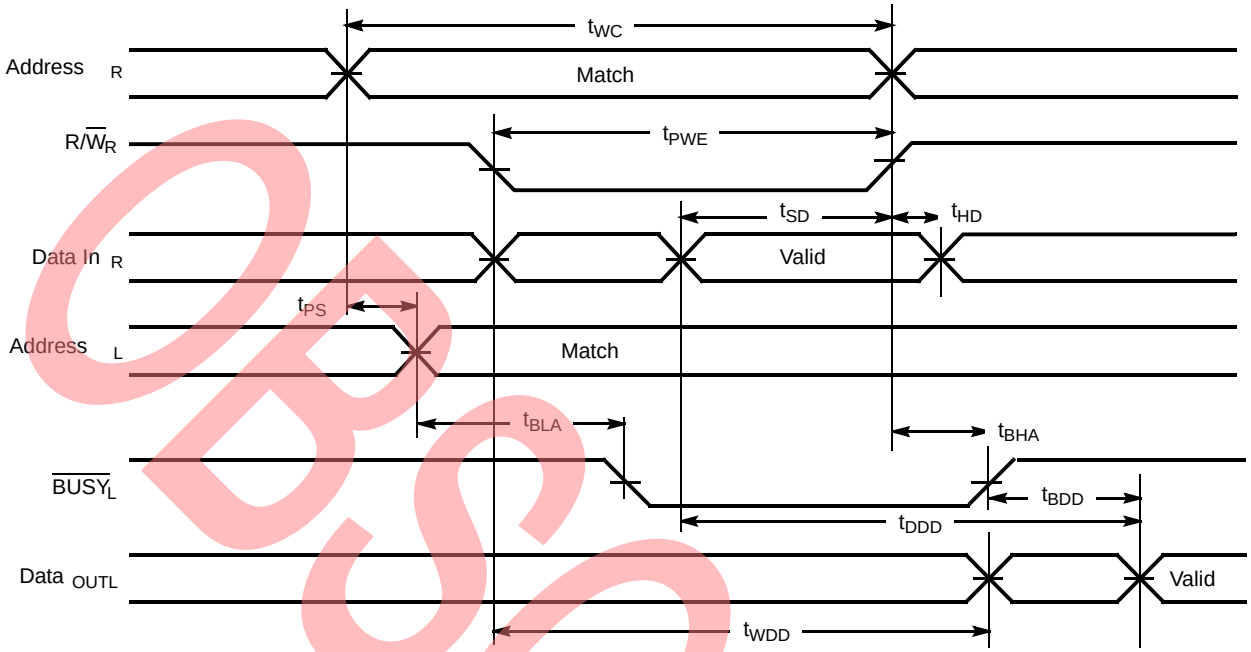
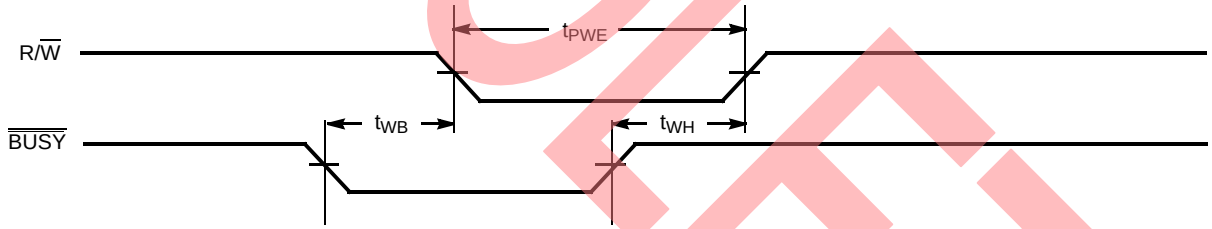


Figure 11. Write Timing with Busy Input (M/$\overline{S}$=LOW)



Note
32. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 12. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[33]

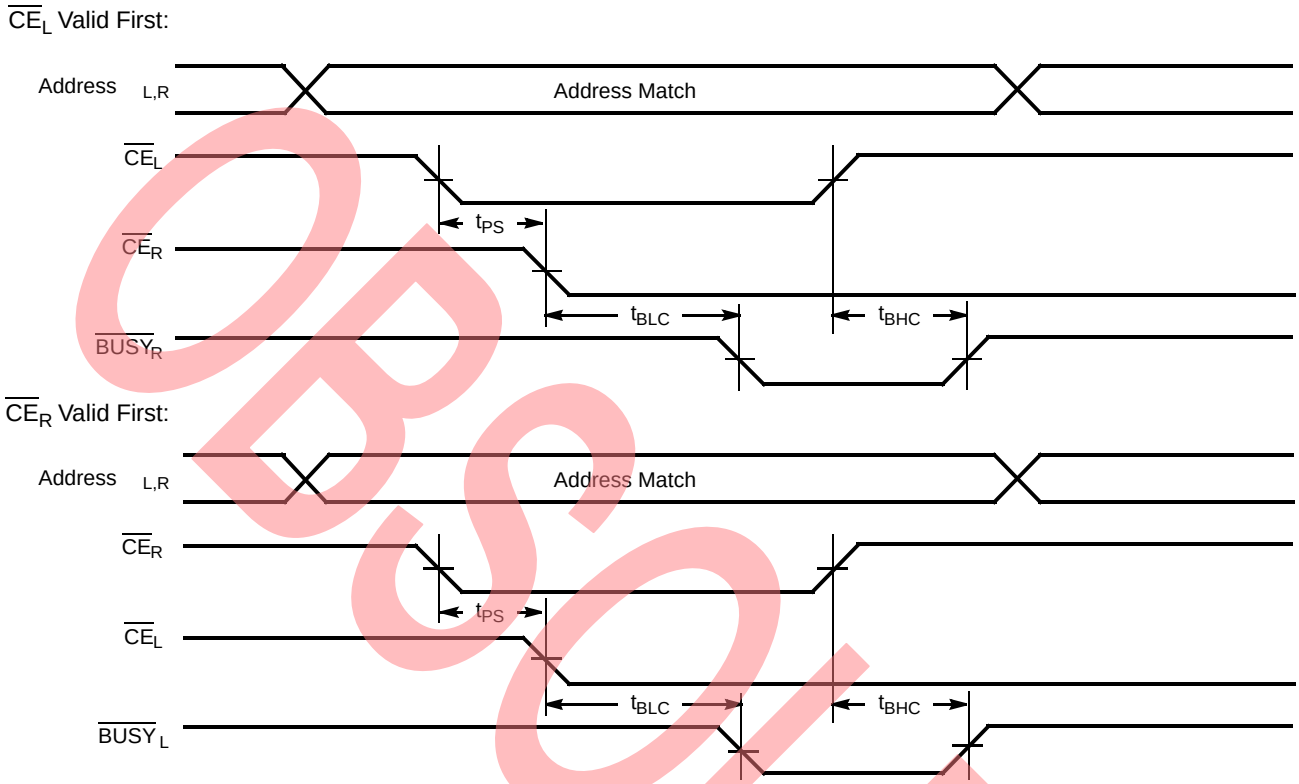
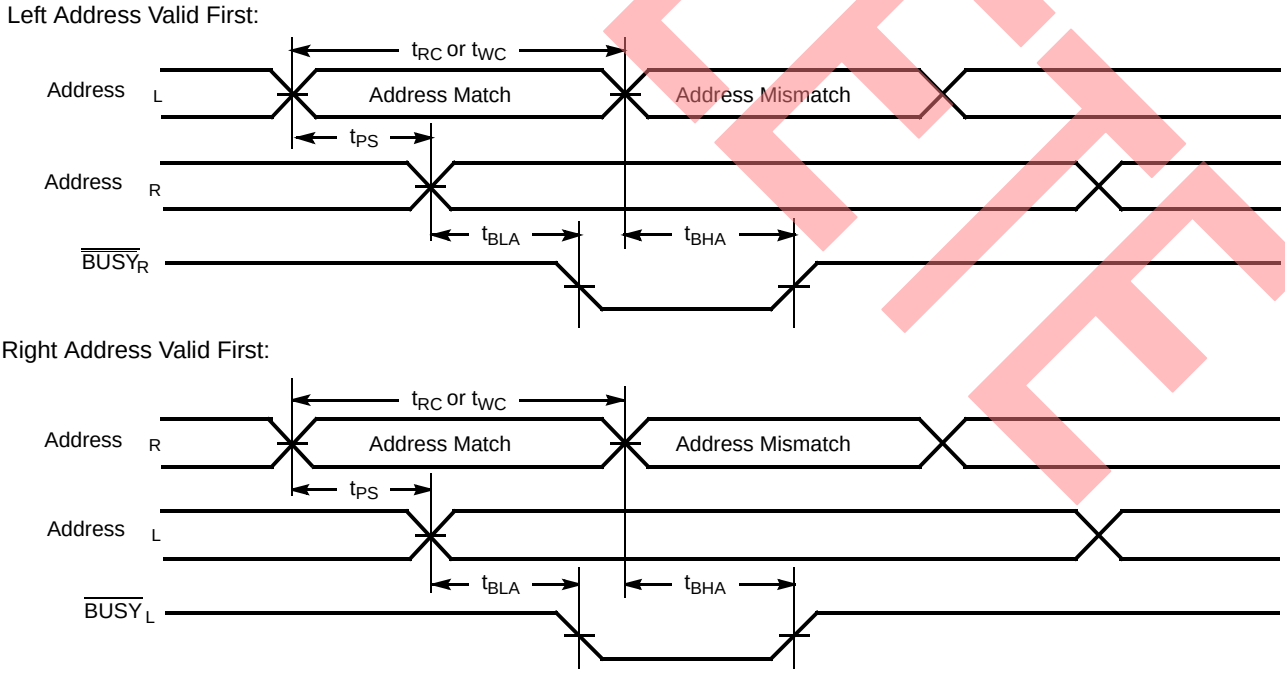


Figure 13. Busy Timing Diagram No. 2 (Address Arbitration)[33]



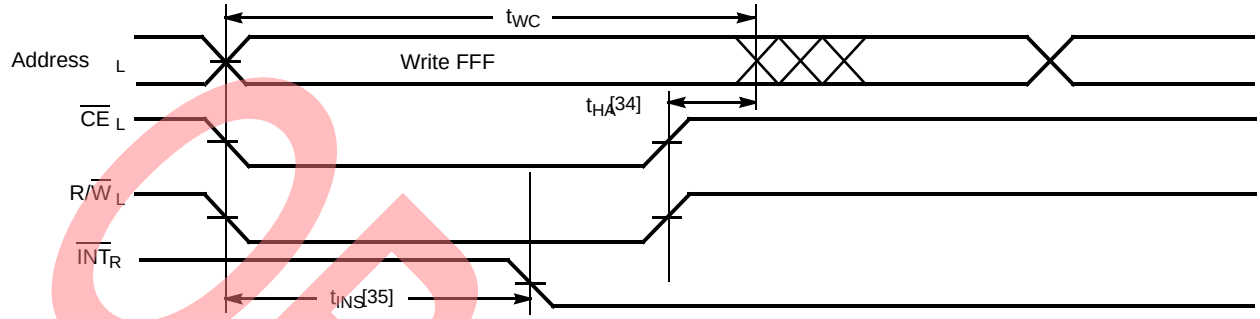
Note

33. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

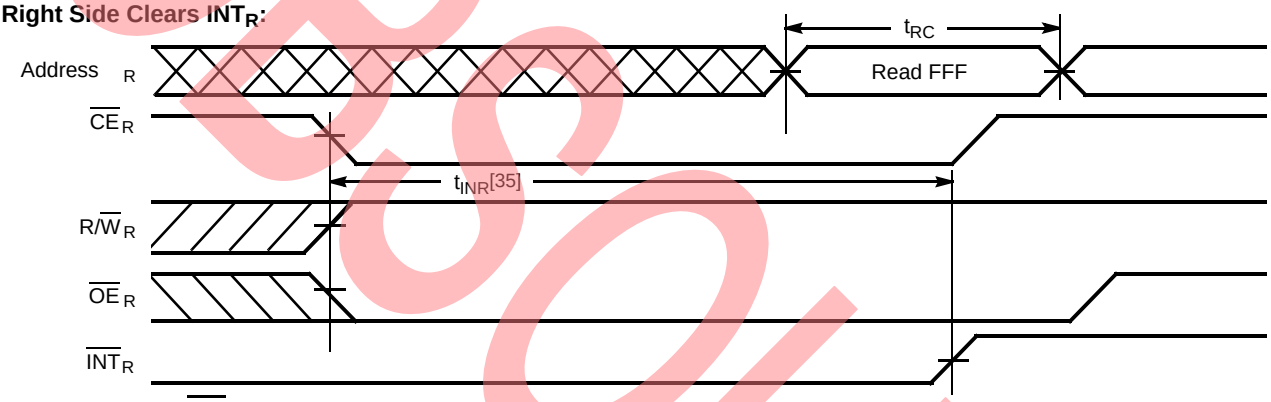
Switching Waveforms (continued)

Figure 14. Interrupt Timing Diagrams

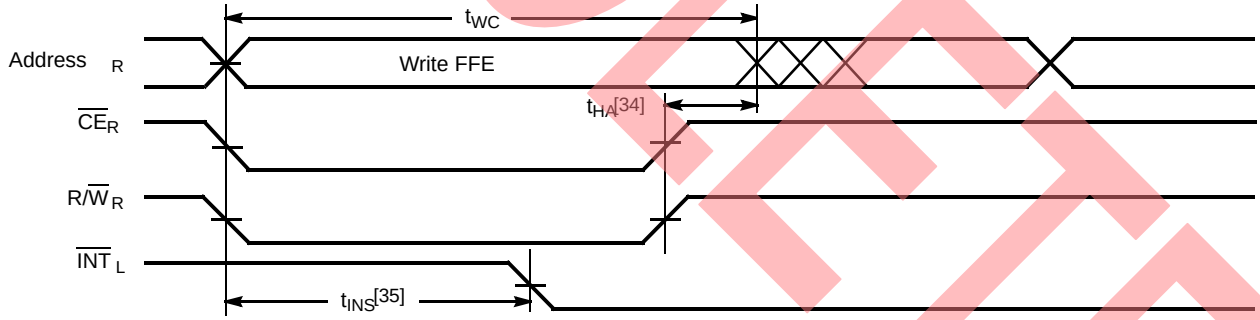
Left Side Sets $\overline{INT}_R$:



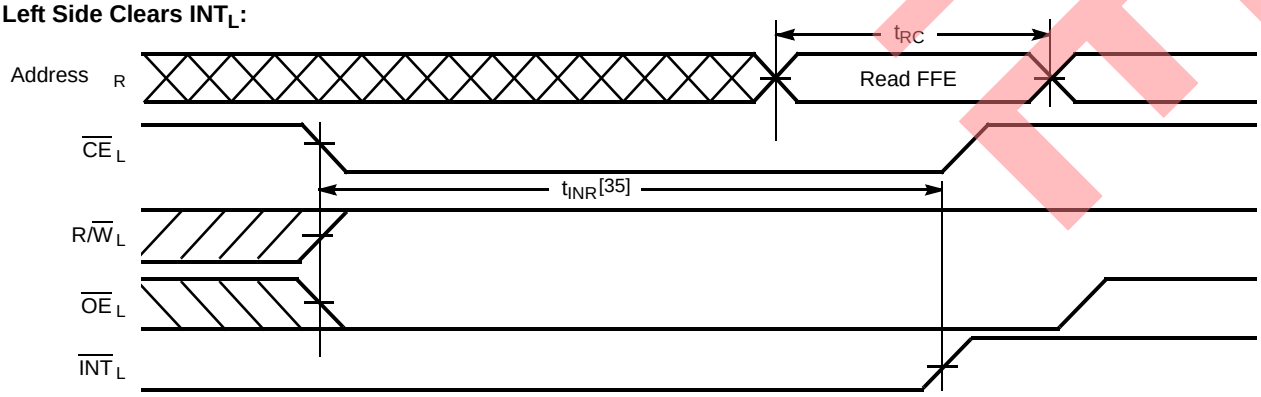
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes

34. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
35. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7C138 consists of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes and reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be used for port–to–port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the CY7C138 can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The CY7C138 has an automatic power-down feature controlled by CE. Each port is provided with its own output enable control (OE), which enables data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the OE pin (see Write Cycle No. 1 waveform) or the R/W pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the OE is deasserted or t_{HZWE} after the falling edge of R/W. Required inputs for non-contention operations are summarized in Table 3.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data is available t_{ACE} after CE or t_{DOE} after OE is asserted. If the user of the CY7C138 wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin.

Interrupts

The interrupt flag (INT) permits communications between ports.When the left port writes to location FFF, the right port's interrupt flag (INT_R) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (INT_L) is accomplished when the right port writes to location FFE. This flag is cleared when the left port reads location FFE. The message at FFF or FFE is user-defined. See Table 4 for input requirements for INT. INT_R and INT_L are push-pull outputs and do not require pull-up resistors to operate. $BUSY_L$ and $BUSY_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C138 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within t_{PS} of each other the Busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location, but it is not guaranteed which one. BUSY will be asserted t_{BLA} after an address match or t_{BLC} after CE is taken LOW.

Master/Slave

A M/S pin is provided to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This enables the device to interface to a master device with no external components.Writing of slave devices must be delayed until after the BUSY input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation.When presented as a HIGH input, the M/S pin allows the device to be used as a master and therefore the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C138 provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the a semaphore.If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting SEM LOW. The SEM pin functions as a chip enable for the semaphore latches (CE must remain HIGH during SEM LOW). $A_{0–2}$ represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to 1 for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port immediately owns the semaphore after the left port releases it. Table 5 shows sample semaphore operations.

When reading a semaphore, all eight or nine data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a 1 written into them at initialization from both sides to assure that they are free when needed.

Table 3. Non-Contending Read/Write

Inputs				Outputs	Operation
CE	R/W	OE	SEM	I/O_{0-7}	
H	X	X	H	High Z	Power-down
H	H	L	L	Data out	Read data in semaphore
X	X	H	X	High Z	I/O lines disabled
H	⎍	X	L	Data in	Write to semaphore
L	H	L	H	Data ut	Read
L	L	X	H	Data in	Write
L	X	X	L		Illegal condition

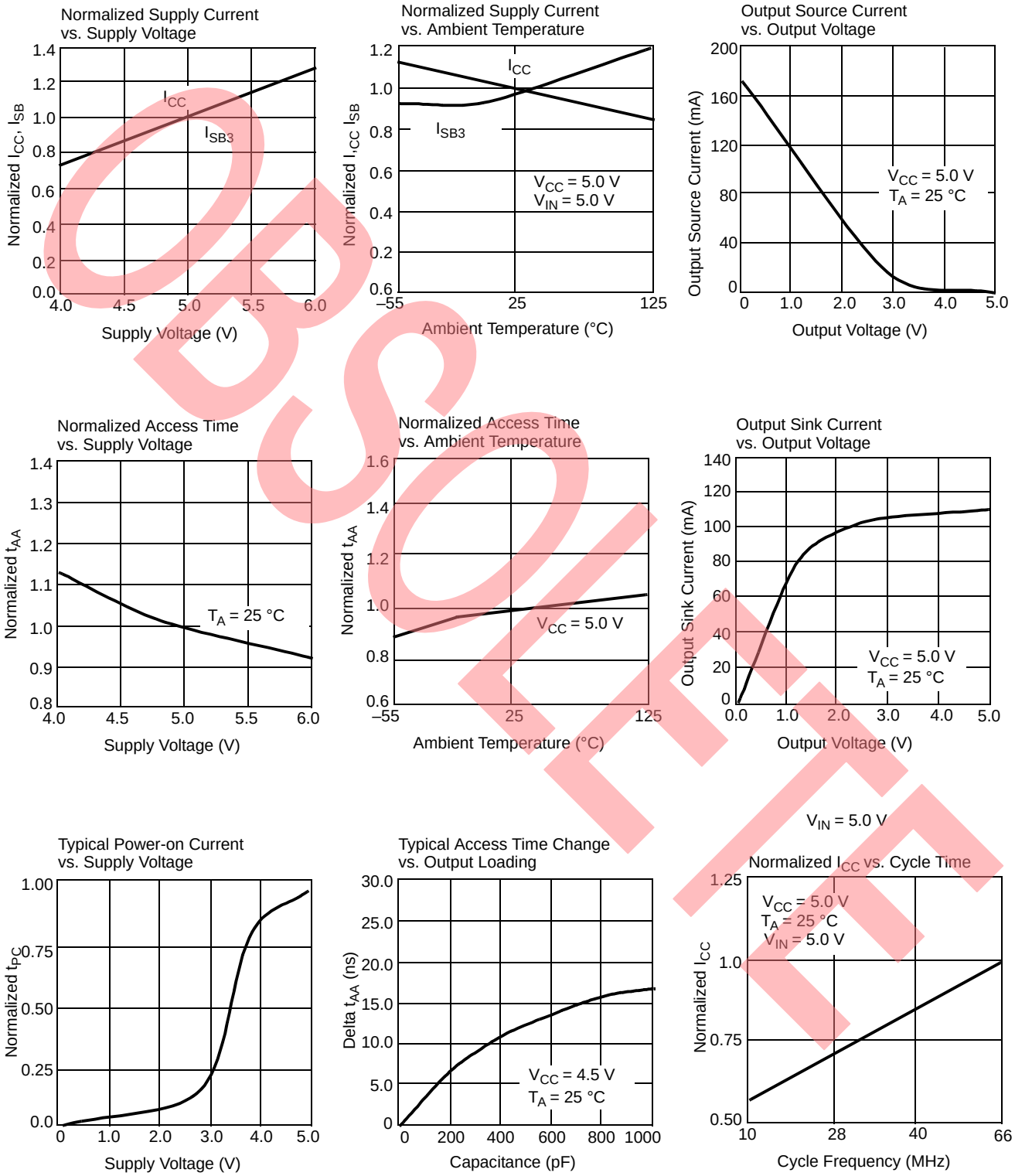
Table 4. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

	Left Port					Right Port				
Function	R/W	CE	OE	A_{0-11}	INT	R/W	CE	OE	A_{0-11}	INT
Set left $\overline{INT}$	X	X	X	X	L	L	L	X	FFE	X
Reset left $\overline{INT}$	X	L	L	FFE	H	X	X	X	X	X
Set right $\overline{INT}$	L	L	X	FFF	X	X	X	X	X	L
Reset right $\overline{INT}$	X	X	X	X	X	X	L	L	FFF	H

Table 5. Semaphore Operation Example

Function	I/O_{0-7} Left	I/O_{0-7} Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Figure 15. Typical DC and AC Characteristics

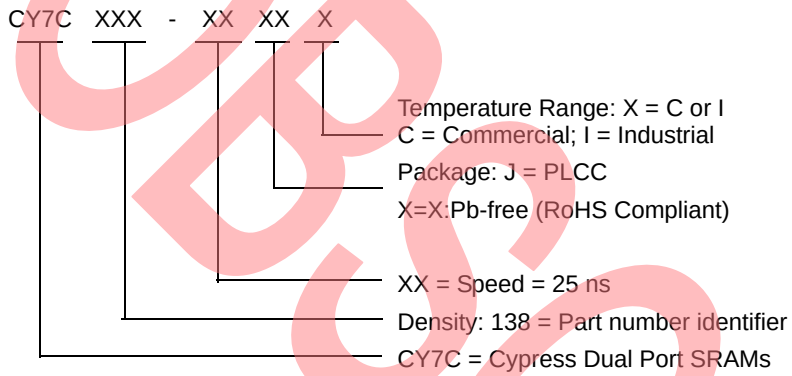


Ordering Information

4K x8 Dual-Port SRAM

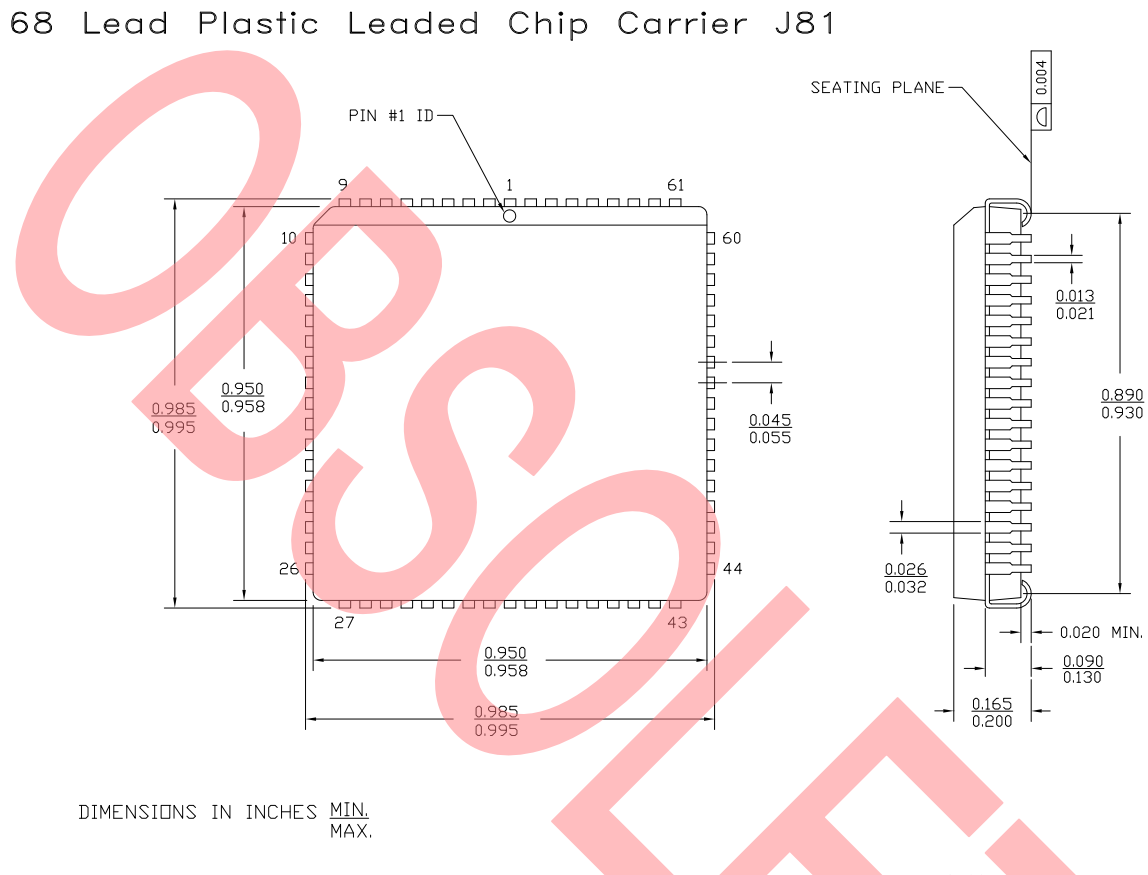
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY7C138-25JXC	51-85005	68-Pin Plastic Leaded Chip Carrier (Pb-free)	Commercial
	CY7C138-25JXI	51-85005	68-Pin Plastic Leaded Chip Carrier (Pb-free)	Industrial

Ordering Code Definition



Package Diagram

Figure 16. 68-Pin Plastic Leaded Chip Carrier (51-85005)



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
TQFP	thin quad plastic flatpack
I/O	input/output
SRAM	static random access memory
PLCC	plastic leaded chip carrier
TTL	transistor transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
Ω	Ohms
mV	milli Volts
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

Document History Page

Document Title: CY7C138 4K x 8/9 Dual-Port Static RAM with Sem, Int, Busy Document Number: 38-06037				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110180	SZV	09/29/01	Change from Spec number: 38-00536 to 38-06037
*A	122287	RBI	12/27/02	power-up requirements added to Maximum Ratings Information
*B	393403	YIM	See ECN	Added Pb-Free Logo Added Pb-Free parts to ordering information: CY7C138-15JXC, CY7C138-25JXC, CY7C139-25JXC
*C	2623658	VKN/PYRS	12/17/08	Added CY7C138-25JXI part Removed CY7C139 from the Ordering information table
*D	2672737	GNKK	03/12/2009	Corrected title in the Document History table
*E	2714768	VKN/AESA	06/04/2009	Corrected defective Logic Block diagram, Pinouts and Package diagrams
*F	2898564	RAME	03/24/10	Removed inactive parts. Updated package diagram.
*G	3099184	ADMU	12/02/2010	Removed information for CY7C139 parts. Removed speed bins -15,-35,-55. Updated datasheet as per new template Added Acronyms and Units of Measure table Added Ordering Code Definition Updated all footnotes.
*H	3402051	ADMU	10/12/2011	Obsolete spec.

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