

## bq28z560 Single Cell Li-Ion Battery Gas Gauge and Protection

Check for Samples: [bq28z560](#)

### FEATURES

- **A Comprehensive Single Cell Li-Ion Battery Manager Integrates All Essential Functions:**
  - Gas Gauge
  - Low-Side N-CH FET Protection Control
  - JEITA/Enhanced Charging
  - Authentication
- **Impedance Track™ Gas Gauging**
- **Protection Functions Help to Prevent:**
  - Short-Circuit
  - Overcurrent Charge and Discharge
  - Overvoltage Charge (Overcharge)
  - Undervoltage (Over-Discharge)

- **Firmware Control of Discharge FET**
- **SHA-1/HMAC Battery Authentication**
- **I<sup>2</sup>C Communications Interface or HDQ Single Wire**
- **12-pin, 2.5-mm x 4.0-mm SON Package**

### APPLICATIONS

- **Tablet PCs**
- **Slates**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

### DESCRIPTION

The Texas Instruments bq28z560 device is a battery gas gauge with current and voltage protection, and secure, SHA-1/HMAC authentication for single-cell Li-Ion battery packs. Designed for battery pack integration, the bq28z560 requires host microcontroller firmware support for implementation. A system processor communicates with the bq28z560 using one of two options: an I<sup>2</sup>C™ serial interface or an HDQ single-wire configuration to obtain remaining battery capacity, system run-time predictions, and other critical battery information.

The bq28z560 uses the accurate Texas Instruments Impedance Track™ gas gauging algorithm to report the status of the cell. The gauge provides information such as state-of-charge (%), run-time to empty (min.), charge time to full (min.), battery voltage (V), and pack temperature (°C).

The bq28z560 also features integrated support for secure battery pack authentication, using the SHA-1/HMAC authentication algorithm.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Impedance Track is a trademark of Texas Instruments.

I<sup>2</sup>C is a trademark of NXP B.V. Corporation.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup>

| T <sub>A</sub> | PART NUMBER  | PACKAGE                     | TAPE AND REEL QUANTITY |
|----------------|--------------|-----------------------------|------------------------|
| -40°C to 85°C  | bq28z560DRZR | 12-pin, 2.5-mm × 4.0-mm SON | 3000                   |
|                | bq28z560DRZT |                             | 250                    |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com ([www.ti.com](http://www.ti.com)).

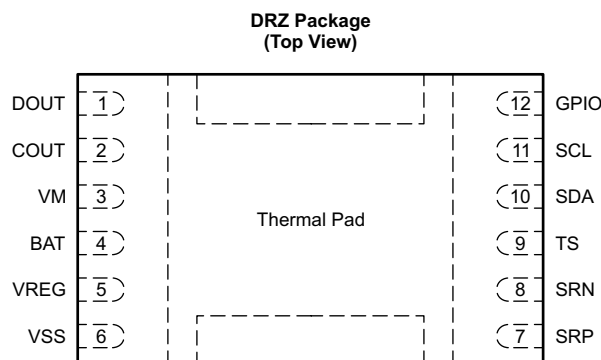
### THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> |   | bq28z560 |       |
|-------------------------------|---|----------|-------|
|                               |   | SON      |       |
|                               |   | 12 PINS  |       |
|                               |   |          | UNITS |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 186.4    | °C/W  |
| $\theta_{JC(top)}$            | Junction-to-case(top) thermal resistance <sup>(3)</sup>     | 90.4     |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance <sup>(4)</sup>         | 110.7    |       |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter <sup>(5)</sup>   | 96.7     |       |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter <sup>(6)</sup> | 90       |       |
| $\theta_{JC(bottom)}$         | Junction-to-case(bottom) thermal resistance <sup>(7)</sup>  | n/a      |       |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://SPRA953).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\Psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\Psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.



## PIN DETAILS

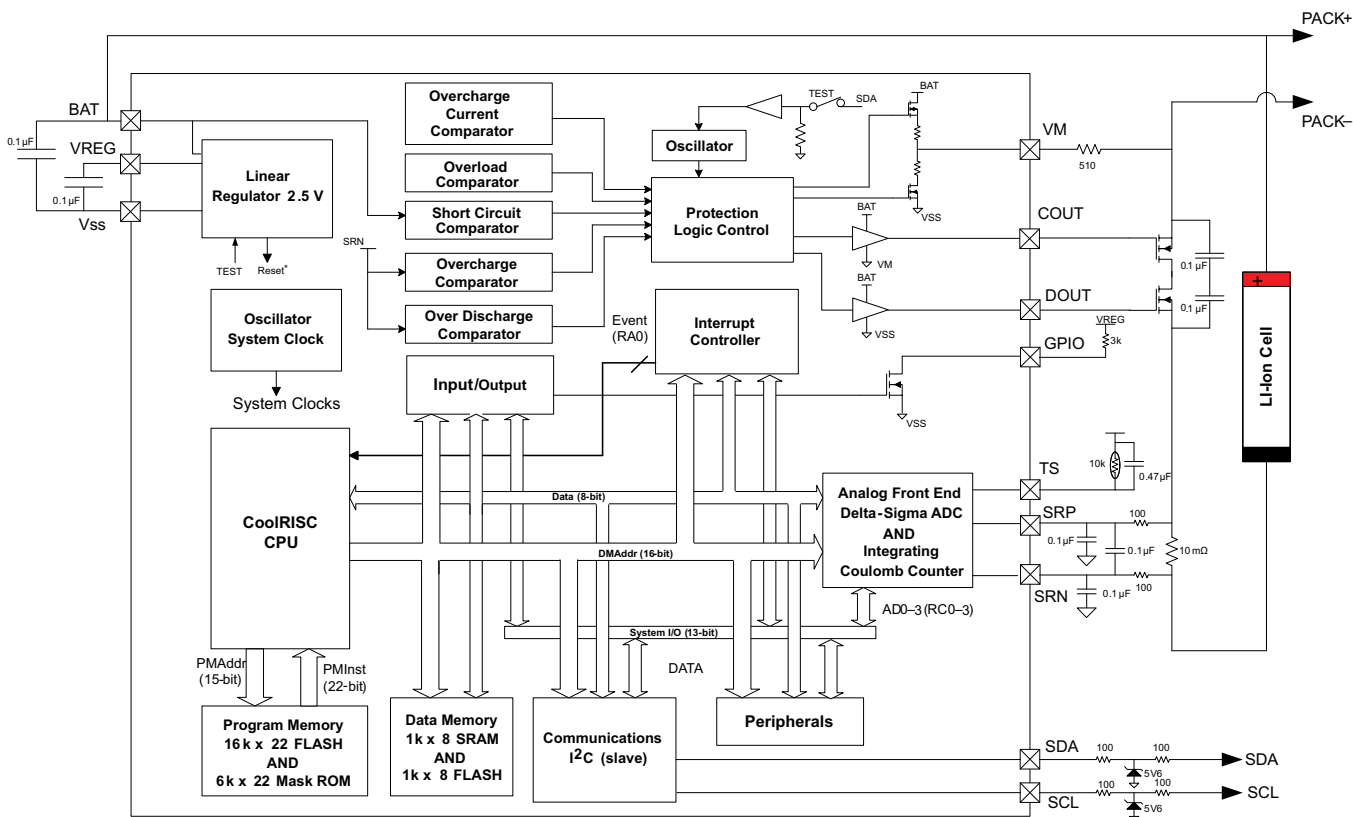


**Table 1. Pin Descriptions**

| PIN NUMBER | PIN NAME | I/O <sup>(1)</sup> | DESCRIPTION  |
|------------|----------|--------------------|--|
| 1          | DOUT     | IA                 | The output of gate drive for discharge FET   |
| 2          | COUT     | IA                 | The output of gate drive for charge FET  |
| 3          | VM       | IA                 | Analog input pin connected to the PACKN through a 510-Ω resistor. Overcurrent and short-circuit protection circuits use the voltage across VM and VSS to detect if excessive charge or discharge current is flowing through the protection FETs. |
| 4          | BAT      | IA                 | Cell voltage measurement input. ADC input. Connect a 0.1-μF ceramic capacitor to VSS.  |
| 5          | VREG     | P                  | 2.5-V output voltage of the internal integrated LDO. Connect a 0.1-μF ceramic capacitor to VSS.  |
| 6          | VSS      | P                  | Device ground  |
| 7          | SRP      | IA                 | Analog input pin connected to the internal coulomb counter where SRP is nearest the CELL-connection. Connect to a 5-mΩ to 20-mΩ sense resistor.  |
| 8          | SRN      | IA                 | Analog input pin connected to the internal coulomb counter where SRN is nearest the PACKN connection. Connect to a 5-mΩ to 20-mΩ sense resistor.   |
| 9          | TS       | IA                 | Pack thermistor voltage sense (use 103AT-type thermistor), ADC input   |
| 10         | SDA      | I/O                | Serial Data interface for SMBus  |
| 11         | SCL      | I                  | Serial Clock interface for SMBus   |
| 12         | GPIO     | I/O                | General Purpose control output for configuration as CFET control OR Alert output OR HDQ interface  |
| 13         | PWPD     | I/O                | Thermal Pad. Connect to VSS externally on PCB.   |

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

**BLOCK DIAGRAM**



**Figure 3. Block Diagram**

**ABSOLUTE MAXIMUM RATINGS**

All voltages are referenced to the VSS pin. Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

| PARAMETER   | VALUE   | UNIT |
|---|---|------|
| V <sub>BAT</sub> Input voltage, BAT (Pin 4)               | -0.3 to 12                                      | V    |
| V <sub>VM</sub> VM terminal voltage (Pin 3)               | V <sub>BAT</sub> - 32 to V <sub>BAT</sub> + 0.3 | V    |
| V <sub>COUT</sub> COUT terminal input voltage (Pin 2)     | V <sub>BAT</sub> - 32 to V <sub>BAT</sub> + 0.3 | V    |
| V <sub>DOUT</sub> DOUT terminal input voltage (Pin 1)     | V <sub>SS</sub> - 0.3 to V <sub>BAT</sub> + 0.3 | V    |
| V <sub>IOD</sub> All other pins (Pins 5, 7, 8, 9, and 12) | -0.3 to 6                                       | V    |
| V <sub>SDATA</sub> SDA (Pin 10)                           | V <sub>SS</sub> - 0.3 to V <sub>BAT</sub> + 0.3 | V    |
| V <sub>SCLK</sub> SCL (Pin 11)                            | V <sub>SS</sub> - 0.3 to V <sub>BAT</sub> + 0.3 | V    |
| ESD Human body model                                      | ±2  | kV   |
| ESD Machine model   | ±200  | V    |
| T <sub>A</sub> Operating free-air temperature range       | -40°C to 85                                     | °C   |
| T <sub>stg</sub> Storage temperature range                | -65°C to 150                                    | °C   |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

$T_A = 25^\circ\text{C}$ ,  $V_{\text{BAT}} = 3.6\text{ V}$  (unless otherwise noted)

| PARAMETER          |   | TEST CONDITIONS   | MIN                    | TYP | MAX  | UNIT          |
|--------------------|---|---|------------------------|-----|------|---------------|
| $V_{\text{BAT}}$   | BAT pin 4 input                         |   | 2.45                   |     | 5.5  | V             |
| $I_{\text{BAT}}$   | Normal operating mode                   | Gas gauge in NORMAL mode. $I_{\text{LOAD}} > \text{Sleep Current}$        |                        | 141 |      | $\mu\text{A}$ |
|                    | Low-power                               | Gas gauge in SLEEP mode. $I_{\text{LOAD}} < \text{Sleep Current}$         |                        | 70  |      |               |
|                    | Sleep                                   | Gas gauge in FULLSLEEP mode. $I_{\text{LOAD}} < \text{Sleep Current}$     |                        | 31  |      |               |
|                    | Hibernate                               | Gas gauge in HIBERNATE mode. $I_{\text{LOAD}} < \text{Hibernate Current}$ |                        | 16  |      |               |
|                    | Shutdown                                | Gas gauge in SHUTDOWN mode  |                        | 1   |      |               |
| $I_{\text{SS}}$    | Maximum current                         |   |                        |     | 20   | mA            |
| $C_{\text{REG}}$   | Regulator output capacitor              |   | 0.1                    |     |      | $\mu\text{F}$ |
| $C_{\text{BAT}}$   | $V_{\text{BAT}}$ input filter capacitor |   |                        | 0.1 |      | $\mu\text{F}$ |
| $R_{\text{PACKN}}$ | Resistor from VM to PACKN               |   |                        | 510 |      | $\Omega$      |
| $R_{\text{PU}_-}$  | SDA pull up resistor                    |   |                        | 1.3 | 3.3  | k $\Omega$    |
| $V_{\text{PU}_-}$  | SDA pull up voltage                     |   | 1.8                    |     | 4.2  | V             |
| $V_{\text{IL}_-}$  | SDA, SCL OR GPIO Input voltage low      |   | -0.3                   |     | 0.6  | V             |
| $V_{\text{IH}_-}$  | SDA, SCL OR GPIO Input voltage high     |   | 1.2                    |     | 6    | V             |
| $V_{\text{OL}_-}$  | SDA or GPIO output voltage low          | $I_{\text{OL}} = 3\text{ mA}$ (open drain)                                | 0                      |     | 0.4  | V             |
| $C_1$              | Capacitance for each I/O pin            | SDA and SCL input capacitance   |                        |     | 10   | pF            |
| $t_{\text{PUCD}}$  | Power Up Communication Delay            |   |                        | 250 |      | ms            |
| $V_{\text{AI}2}$   | Input voltage range (SRP, SRN)          |   | $V_{\text{SS}} - 0.25$ |     | 0.25 | V             |

## BATTERY PROTECTION

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{\text{BAT}} = 1.5\text{ V}$  to  $5.5\text{ V}$ ; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 3.6\text{ V}$  (unless otherwise noted)

| PARAMETER          |  | TEST CONDITION  | MIN | NOM  | MAX  | UNIT       |
|--------------------|--|---|-----|------|------|------------|
| $V_{\text{ST}}$    | Minimum operating voltage for 0 V charging         | $V_{\text{ST}} = V_{\text{BAT}} - V_{\text{M}}$                     |     |      | 1.2  | V          |
| $R_{\text{SHORT}}$ | Overcurrent release resistance                     | $V_{\text{BAT}} = 4.0\text{ V}$ , $V_{\text{M}} = 1\text{ V}$       | 30  | 50   | 100  | k $\Omega$ |
| $R_{\text{DS}}$    | DS pin pull-down resistance                        | $V_{\text{BAT}} = 4.0\text{ V}$                                     | 6.5 | 13.0 | 26.0 | k $\Omega$ |
| $V_{\text{OL}1}$   | COUT Low Level Output voltage (referenced to VM)   | $I_{\text{OL}} = 30\ \mu\text{A}$ , $V_{\text{BAT}} = 4.5\text{ V}$ |     | 0.4  | 0.5  | V          |
| $V_{\text{OH}1}$   | COUT High Level Output voltage (referenced to VM)  | $I_{\text{OH}} = 30\ \mu\text{A}$ , $V_{\text{BAT}} = 4.0\text{ V}$ | 3.4 | 3.7  |      | V          |
| $V_{\text{OL}2}$   | DOUT Low Level Output voltage (referenced to Vss)  | $I_{\text{OL}} = 30\ \mu\text{A}$ , $V_{\text{BAT}} = 2.0\text{ V}$ |     | 0.2  | 0.5  | V          |
| $V_{\text{OH}2}$   | DOUT High Level Output voltage (referenced to Vss) | $I_{\text{OH}} = 30\ \mu\text{A}$ , $V_{\text{BAT}} = 4.0\text{ V}$ | 3.4 | 3.7  |      | V          |

## BATTERY PROTECTION (continued)

 $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{\text{BAT}} = 1.5$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 3.6$  V (unless otherwise noted)

| PARAMETER          |  | TEST CONDITION  | MIN                    | NOM                    | MAX                    | UNIT          |
|--------------------|--|---|------------------------|------------------------|------------------------|---------------|
| $V_{\text{DET1}}$  | Overcharge detection                       | $T_A = 25^\circ\text{C}$ detection voltage              | 4.230                  | 4.250                  | 4.270                  | V             |
|                    |  | $T_A = -10$ to $60^\circ\text{C}$                       | 4.225                  | 4.250                  | 4.275                  |               |
|                    |  | $T_A = -40$ to $85^\circ\text{C}$                       | 4.200                  | 4.250                  | 4.300                  |               |
| $V_{\text{REL1}}$  | Overcharge release voltage                 | $T_A = 25^\circ\text{C}$                                | 4.040                  | 4.070                  | 4.100                  | V             |
|                    |  | $T_A = -10$ to $60^\circ\text{C}$                       | 4.025                  | 4.070                  | 4.115                  |               |
|                    |  | $T_A = -40$ to $85^\circ\text{C}$                       | 4.010                  | 4.070                  | 4.130                  |               |
| $t_{\text{DET1}}$  | Overcharge detection delay time            | $V_{\text{BAT}} = 3.5$ V $\geq$ 4.5 V                   | 0.60                   | 1.00                   | 1.50                   | s             |
| $t_{\text{REL1}}$  | Overcharge release delay time              | $V_{\text{BAT}} = 4.5$ V $\geq$ 3.5 V                   | 4.8                    | 8.0                    | 12.0                   | ms            |
| $V_{\text{DET2}}$  | Over-discharge detection voltage           | $T_A = 25^\circ\text{C}$                                | 2.265                  | 2.300                  | 2.335                  | V             |
|                    |  | $T_A = -10$ to $60^\circ\text{C}$                       | 2.242                  | 2.300                  | 2.358                  |               |
|                    |  | $T_A = -40$ to $85^\circ\text{C}$                       | 2.220                  | 2.300                  | 2.380                  |               |
| $t_{\text{DET2}}$  | Over-discharge detection delay time        | $V_{\text{BAT}} = 3.5$ V $\geq$ 2.00 V                  | 14.4                   | 24.0                   | 36.0                   | ms            |
| $t_{\text{REL2}}$  | Over-discharge release delay time          | $V_{\text{BAT}} = 3$ V<br>$V_M = 3$ V $\geq$ 0 V        | 2.4                    | 4.0                    | 6.0                    | ms            |
| $V_{\text{DET3}}$  | Overcurrent detection voltage on discharge | $V_{\text{BAT}} = 4$ V                                  | 0.130                  | 0.150                  | 0.170                  | V             |
| $V_{\text{DET4}}$  | Overcurrent detection voltage on charging  | $V_{\text{BAT}} = 4$ V                                  | -0.137                 | -0.112                 | -0.087                 | V             |
| $t_{\text{OCD}}$   | Overcurrent detection delay time           | $V_{\text{BAT}} = 3$ V<br>$V_M = 0$ V $\geq$ 1V         | 7.2                    | 12.0                   | 18.0                   | ms            |
| $t_{\text{OCR}}$   | Overcurrent release delay time             | $V_{\text{BAT}} = 3$ V<br>$V_M = 3$ V $\geq$ 0 V        | 2.4                    | 4.0                    | 6.0                    | ms            |
| $V_{\text{SHORT}}$ | Short detection voltage                    | $V_{\text{BAT}} = 4$ V, $R_{\text{PACKN}} = 510 \Omega$ | $V_{\text{BAT}} - 1.2$ | $V_{\text{BAT}} - 0.9$ | $V_{\text{BAT}} - 0.6$ | V             |
| $t_{\text{SHORT}}$ | Short detection delay time                 | $V_{\text{BAT}} = 3$ V<br>$V_M = 0$ V $\geq$ 3 V        | 200                    | 400                    | 800                    | $\mu\text{s}$ |

## VOLTAGE REGULATOR

 $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{\text{BAT}} = 1.5$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 3.6$  V (unless otherwise noted)

| PARAMETER                        |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT                  |
|----------------------------------|--|---|------|------|------|-----------------------|
| $V_{\text{REG}}$                 | Output voltage                         | $2.7$ V $<$ $V_{\text{BAT}} <$ 5.5 V, $I_{\text{OUT}} = 16$ mA  | 2.45 | 2.50 | 2.55 | V                     |
|                                  |  | $2.45$ V $<$ $V_{\text{BAT}} <$ 2.7 V, $I_{\text{OUT}} = 3$ mA  | 2.40 |      |      |                       |
| $\Delta V_{\text{LINE}}$         | Line regulation                        | $2.7$ V $<$ $V_{\text{BAT}} <$ 5.5 V, $I_{\text{OUT}} = 16$ mA  |      | 100  | 200  | mV                    |
| $\Delta V_{\text{LOAD}}$         | Load regulation                        | $V_{\text{REG}} = 2.45$ V, $100 \mu\text{A} <$ $I_{\text{OUT}} <$ 3 mA  |      | 30   | 50   | mV                    |
|                                  |  | $V_{\text{BAT}} = 2.7$ V, $3$ mA $<$ $I_{\text{OUT}} <$ 16 mA   |      | 30   | 50   |                       |
| VDO                              | Dropout voltage                        | $V_{\text{BAT}} = 2.45$ V, $I_{\text{OUT}} = 3$ mA  |      | 30   | 50   | mV                    |
|                                  |  | $V_{\text{BAT}} = 2.7$ V, $I_{\text{OUT}} = 16$ mA  |      | 30   | 50   |                       |
| $\Delta V_{\text{REG}}/\Delta T$ | Output voltage temperature coefficient | $V_{\text{BAT}} = 3.5$ V, $I_{\text{OUT}} = 100 \mu\text{A}$  |      | 100  |      | ppm/ $^\circ\text{C}$ |
| $\Delta I_{\text{LINE}}$         | Current limit                          | $V_{\text{BAT}} = 3.5$ V, $I_{\text{REG}} = 2.0$ V  | 16   |      | 130  | mA                    |
|                                  |  | $V_{\text{BAT}} = 3.5$ V, $I_{\text{REG}} = 0$ V  | 10   | 35   | 60   |                       |
| $V_{\text{OFF}}$                 | Regulator off voltage                  |   | 7.0  | 8.0  | 9.0  | V                     |
| $t_{\text{VOFF}}$                | Regulator off voltage delay time       | $V_{\text{BAT}} = 3.6$ V $\rightarrow$ 5.5 V, $R_{\text{load}} = 100 \Omega$<br>$V_{\text{REG}} = 2.5$ V $\rightarrow$ 2.3 V, $C_{\text{load}} = 0.1 \mu\text{F}$ ,<br>$T_A = 25^\circ\text{C}$ |      | 50   | 100  | $\mu\text{s}$         |

## POWER-ON RESET

$T_A = -40$  to  $+85^\circ\text{C}$ ; Typical Values at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                                   | MIN   | TYP   | MAX   | UNIT |
|-----------|---|-------|-------|-------|------|
| $V_{IT+}$ | Positive-going battery voltage input at $V_{REG}$ | 2.125 | 2.200 | 2.275 | V    |
| $V_{HYS}$ | No external loading on $V_{REG}$                  | 75    | 125   | 175   | mV   |

## INTERNAL TEMPERATURE SENSOR CHARACTERISTICS

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{BAT} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = 3.6$  V (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                 | MIN | TYP  | MAX | UNIT                 |
|------------|---------------------------------|-----|------|-----|----------------------|
| $G_{TEMP}$ | Temperature sensor voltage gain |     | -2.0 |     | mV/ $^\circ\text{C}$ |

## HIGH FREQUENCY OSCILLATOR

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{BAT} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = 3.6$  V (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS                     | MIN   | TYP   | MAX  | UNIT |   |
|-------------|-------------------------------------|---|-------|------|------|---|
| $f_{(OSC)}$ | Operating frequency                 |   | 2.097 |      | MHz  |   |
| $f_{(EIO)}$ | Frequency error <sup>(1), (2)</sup> | $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$   | -2.0  | 0.38 | 2.0  | % |
|             |                                     | $T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$ | -3.0  | 0.38 | 3.0  | % |
|             |                                     | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | -4.5  | 0.38 | 4.5  | % |
| $t_{(SXO)}$ | Start-up time <sup>(3)</sup>        |   | 2.5   | 5    | ms   |   |

(1) The frequency error is measured from 2.097 MHz.

(2) The frequency drift is included and measured from the trimmed frequency at  $V_{CC} = 2.5$  V,  $T_A = 25^\circ\text{C}$ .

(3) The startup time is defined as the time it takes for the oscillator output frequency to be  $\pm 3\%$ .

## LOW FREQUENCY OSCILLATOR

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{BAT} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = 3.6$  V (unless otherwise noted)

| PARAMETER    | TEST CONDITIONS                     | MIN   | TYP    | MAX  | UNIT          |   |
|--------------|-------------------------------------|---|--------|------|---------------|---|
| $f_{(LOSC)}$ | Operating frequency                 |   | 32.768 |      | kHz           |   |
| $f_{(LEIO)}$ | Frequency error <sup>(1), (2)</sup> | $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$   | -1.5   | 0.25 | 1.5           | % |
|              |                                     | $T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$ | -2.5   | 0.25 | 2.5           | % |
|              |                                     | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | -4.0   | 0.25 | 4.0           | % |
| $t_{(LSXO)}$ | Start-up time <sup>(3)</sup>        |   |        | 500  | $\mu\text{s}$ |   |

(1) The frequency drift is included and measured from the trimmed frequency at  $V_{CC} = 2.5$  V,  $T_A = 25^\circ\text{C}$ .

(2) The frequency error is measured from 32.768 kHz.

(3) The startup time is defined as the time it takes for the oscillator output frequency to be  $\pm 3\%$ .

## INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{BAT} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = 3.6$  V (unless otherwise noted)

| PARAMETER      | TEST CONDITIONS                            | MIN                     | TYP         | MAX         | UNIT          |
|----------------|--|-------------------------|-------------|-------------|---------------|
| $V_{IN(SR)}$   | Input voltage range, $V(SRN)$ and $V(SRP)$ | $VSR = V(SRN) - V(SRP)$ |             | 0.125       | V             |
| $t_{CONV(SR)}$ | Conversion time                            |                         | 1           |             | s             |
|                | Resolution                                 | 14                      |             | 15          | bits          |
| $V_{OS(SR)}$   | Input offset                               |                         | 10          |             | $\mu\text{V}$ |
| INL            | Integral non-linearity error               |                         | $\pm 0.007$ | $\pm 0.034$ | FSR           |
| $Z_{IN(SR)}$   | Effective input resistance <sup>(1)</sup>  | 2.5                     |             |             | M $\Omega$    |
| $I_{kg(SR)}$   | Input leakage current <sup>(1)</sup>       |                         |             | 0.3         | $\mu\text{A}$ |

(1) Specified by design. Not production tested.



## ADC (TEMPERATURE AND CELL VOLTAGE) CHARACTERISTICS

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{\text{BAT}} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 3.6$  V (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS                     | MIN  | TYP | MAX | UNIT |
|---|-------------------------------------|------|-----|-----|------|
| $V_{\text{IN(ADC)}}$ Input voltage range                            |                                     | -0.2 |     | 1   | V    |
| $t_{\text{CONV(ADC)}}$ Conversion time                              |                                     |      |     | 125 | ms   |
| Resolution  |                                     | 14   |     | 15  | bits |
| $V_{\text{OS(ADC)}}$ Input offset                                   |                                     |      | 1   |     | mV   |
| $Z_{\text{(ADC1)}}$ Effective input resistance (TS) <sup>(1)</sup>  |                                     | 8    |     |     | MΩ   |
| $Z_{\text{(ADC2)}}$ Effective input resistance (BAT) <sup>(1)</sup> | bq28z560 not measuring cell voltage | 8    |     |     | MΩ   |
|   | bq28z560 measuring cell voltage     |      | 100 |     | kΩ   |
| $I_{\text{lkq(ADC)}}$ Input leakage current <sup>(1)</sup>          |                                     |      |     | 0.3 | μA   |

(1) Specified by design. Not production tested.

## DATA FLASH MEMORY CHARACTERISTICS

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{\text{BAT}} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 3.6$  V (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS | MIN    | TYP | MAX | UNIT   |
|---|-----------------|--------|-----|-----|--------|
| $t_{\text{DR}}$ Data retention <sup>(1)</sup>                 |                 | 10     |     |     | Years  |
| Flash programming write-cycles <sup>(1)</sup>                 |                 | 20,000 |     |     | Cycles |
| $t_{\text{WORDPROG}}$ Word programming time <sup>(1)</sup>    |                 |        |     | 2   | ms     |
| $I_{\text{CCPROG}}$ Flash-write supply current <sup>(1)</sup> |                 |        | 5   | 10  | mA     |

(1) Specified by design. Not production tested.

## HDQ COMMUNICATION TIMING CHARACTERISTICS

$T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{\text{BAT}} = 2.7$  V to 5.5 V; Typical values stated, where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 3.6$  V (unless otherwise noted). Capacitance on GPIO is 10 pF unless otherwise specified <sup>(1)</sup>.

| PARAMETER   | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| $t_{\text{(CYCH)}}$ Cycle time, host to bq28z560            |                 | 190 |     |     | μs   |
| $t_{\text{(CYCD)}}$ Cycle time, bq28z560 to host            |                 | 190 | 205 | 250 | μs   |
| $t_{\text{(HW1)}}$ Host sends 1 to bq28z560                 |                 | 0.5 |     | 50  | μs   |
| $t_{\text{(DW1)}}$ bq28z560 sends 1 to host                 |                 | 32  |     | 50  | μs   |
| $t_{\text{(HW0)}}$ Host sends 0 to bq28z560                 |                 | 86  |     | 145 | μs   |
| $t_{\text{(DW0)}}$ bq28z560 sends 0 to host                 |                 | 80  |     | 145 | μs   |
| $t_{\text{(RSPS)}}$ Response time, bq28z560 to host         |                 | 190 |     | 950 | μs   |
| $t_{\text{(B)}}$ Break Time                                 |                 | 190 |     |     | μs   |
| $t_{\text{(BR)}}$ Break Recovery Time                       |                 | 40  |     |     | μs   |
| $t_{\text{(RISE)}}$ HDQ Line Rising Time to Logic 1 (1.2 V) |                 |     |     | 950 | ns   |

(1) Parameters specified by worst-case test program execution in fast mode.

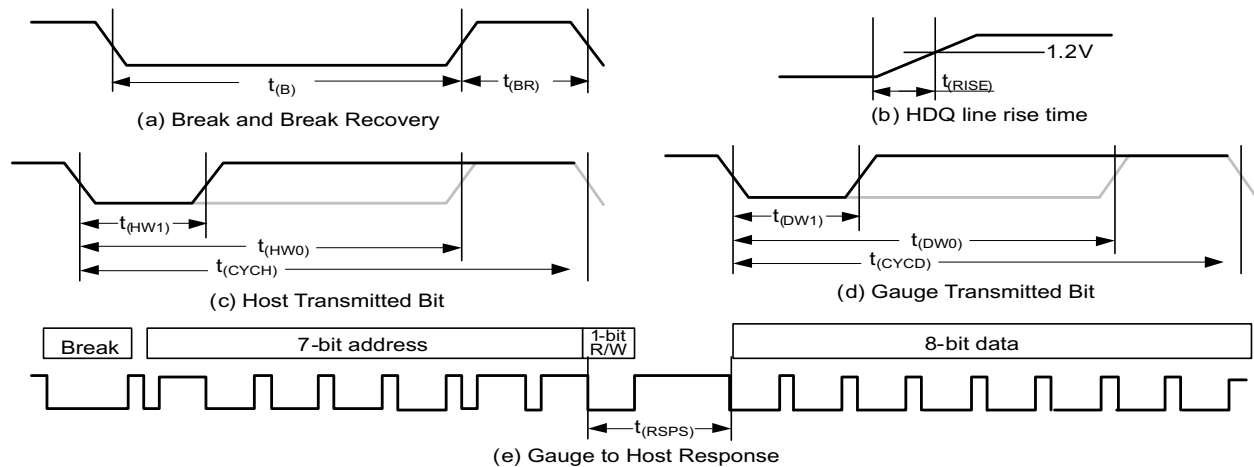


Figure 4. HDQ Timing

### I<sup>2</sup>C SERIAL COMMUNICATION TIMING CHARACTERISTICS

T<sub>A</sub> = -40 to +85°C, V<sub>BAT</sub> = 2.7 V to 5.5 V; Typical values stated, where T<sub>A</sub> = 25°C and V<sub>BAT</sub> = 3.6 V (unless otherwise noted). Capacitance on serial interface pins SCL and SDA are 10 pF unless otherwise specified <sup>(1)</sup>.

| PARAMETER             | TEST CONDITIONS                      | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------------|-----|-----|-----|------|
| t <sub>r</sub>        | SCL/SDA rise time                    |     |     | 300 | ns   |
| t <sub>f</sub>        | SCL/SDA fall time                    |     |     | 300 | ns   |
| t <sub>w(H)</sub>     | SCL pulse width (high)               | 600 |     |     | ns   |
| t <sub>w(L)</sub>     | SCL pulse width (low)                | 1.3 |     |     | µs   |
| t <sub>su(STA)</sub>  | Setup for repeated start             | 600 |     |     | ns   |
| t <sub>d(STA)</sub>   | Start to first falling edge of SCL   | 600 |     |     | ns   |
| t <sub>su(DAT)</sub>  | Data setup time                      | 1   |     |     | µs   |
| t <sub>h(DAT)</sub>   | Data hold time                       | 0   |     |     | ns   |
| t <sub>su(STOP)</sub> | Setup time for stop                  | 600 |     |     | ns   |
| t <sub>(BUF)</sub>    | Bus free time between stop and start | 1.3 |     |     | µs   |
| f <sub>(SCL)</sub>    | Clock frequency                      |     |     | 100 | kHz  |

(1) Parameters specified by worst-case test program execution in fast mode.

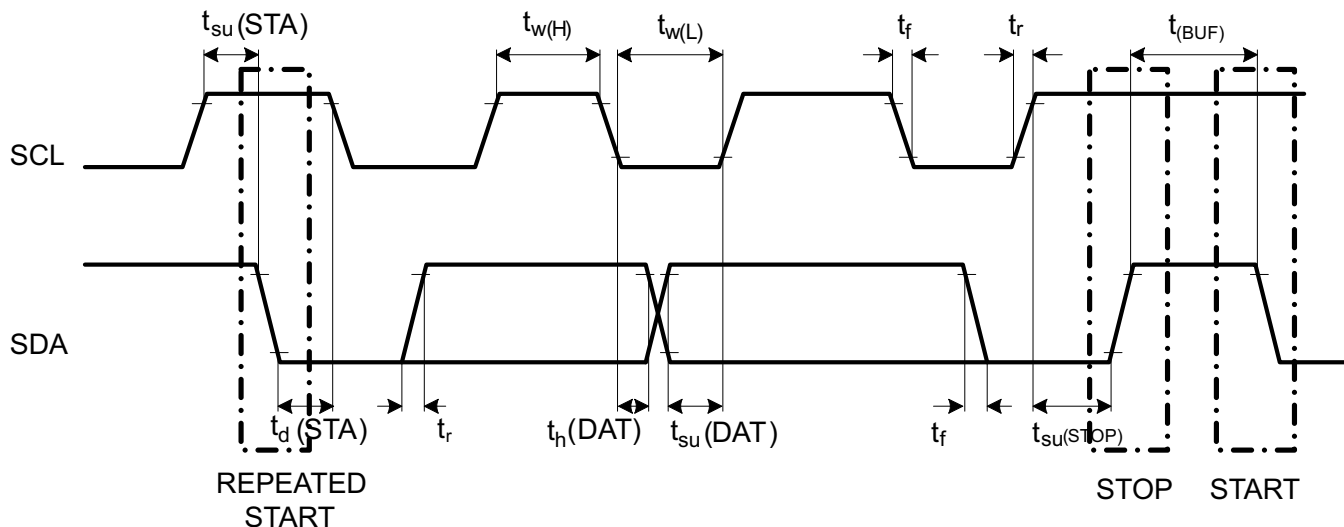


Figure 5. I<sup>2</sup>C Serial Communication Timing

## I<sup>2</sup>C BUS COMMUNICATION

The 2-wire communication bus supports a slave-only device in a single- or multi-slave configuration with a single- or multi-master configuration. The device can be part of a shared bus by the unique setting of the 7-bit slave address. The 2-wire communication is bi-directional, consisting of a serial data line (SDA) and serial clock line (SCL). In RECEIVE mode, the SDA terminal operates as an input; whereas, when the device is returning data to the master, the SDA operates as an open drain output with an external resistive pull-up. The master device controls the initiation of the transaction on the bus line.

**Data Transfer:** Each data bit is transferred during an SCL clock cycle (transition from low-to-high and then high-to-low). The data signal on the SDA (logic level) must be stable during the high period of the SCL clock pulse. A change in the SDA logic when SCL is high is interpreted as a START or STOP control signal. If a transfer is interrupted by a STOP condition, the partial byte transmission shall not be latched. Only the prior messages transmitted and acknowledged are latched.

**Data Format:** The data is an 8-bit format with the most significant bit (MSB) first, and the least significant bit (LSB) followed by an Acknowledge bit. If the slave cannot receive or transmit any byte of data until it services a priority interrupt, it can pull the SCL line low to force the master device into wait state. The slave, once ready to resume data transfer, can release the SCL line (get out of wait state).

**Bus Idle:** The bus is considered idle or busy when no master device has control of this device. The SDA and SCL lines are high when the bus is idle. The appropriate method to go into the STOP condition is to ensure the bus returns to idle state.

**START (S) and STOP (P) Conditions:** To initiate communications, the master device transitions the SDA line from high-to-low when the SCL is high. Conversely, to STOP the communication, the SDA goes low-to-high when the SCL is high. To continue communication without termination of one transaction and beginning another, a repeated START (Sr) method can be used without a STOP condition being initiated. These are the only conditions (START or STOP) when SDA transitions when SCL is high.

**Acknowledge Bits:** An Acknowledge bit (A) is required after each data transfer byte to ensure correct communications. This occurs when the receiving device pulls the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keeps it low until the SCL returns low. There is also a No-Acknowledge bit (N), which occurs when the receiver releases the SDA line (high) before the rising edge of acknowledge-related clock pulse, and maintains the SDA line high until SCL returns low. The Acknowledge bit indicates if a successful data transfer has occurred between the master and slave device. Monitoring this bit also indicates an unsuccessful data transfer due to the receiving device being busy or as system fault occurrence.

### Communication Format

A **START** command immediately followed by a **STOP** command is an illegal format.

| MSB |               |     |   |      |   |
|-----|---------------|-----|---|------|---|
| S   | Slave Address | R/W | A | Data | P |

S = START Command

R/W = Read from slave device ("1") or Write to slave device ("0")

A = Acknowledge bit

P = STOP Command

Slave Address = 7-bit address field for register address

Data = 8-bit data field

## GENERAL DESCRIPTION

The bq28z560 accurately predicts the battery capacity and other operational characteristics of a single Li-Ion based rechargeable cell, while also providing a state-of-the-art protection function against short circuit, overcurrent, and overvoltage. The device can be integrated by a system processor to provide cell information, such as state-of-charge (SOC), Remaining Capacity, and Full Charge Capacity (FCC).

### NOTE

FORMATTING CONVENTIONS IN THIS DOCUMENT:

**Commands:** Italics with parentheses and no breaking spaces; for example, *RemainingCapacity()*.

**Data Flash:** Italics, bold, and breaking spaces; for example, ***Design Capacity***.

**Register Bits and Flags:** Brackets only; for example, [TDA]

**Data Flash Bits:** Italic and bold; for example, ***[NR]***

**Modes and States:** All capitals; for example, SEALED mode.

## DATA ACQUISITION

### Cell Voltage

The bq28z560 samples the single cell voltage from the BAT input terminal. The cell voltage is sampled and updated every 1 s in normal mode. To ensure accurate cell measurement, the VSS ground connection of the bq28z560 should be connected to the negative terminal of the single cell and *not* to the positive side of the sense resistor.

### Charge Measurement

The device samples the charge into and out of the single cell using a low value sense resistor. The resistor (typically 5 mΩ to 20 mΩ) is connected between SRP and SRN to form a differential input to an integrating ADC (coulomb counter). Charge activity is detected when  $V_{SR} = V_{SRP} - V_{SRN}$  is positive and discharge activity is detected when  $V_{SR} = V_{SRP} - V_{SRN}$  is negative. This data is integrated over a period of time using an internal counter, and updates *RemainingCapacity* with charge and discharge amounts every 1 s in normal mode.

### Current Measurement

The device has a FIFO buffer, which uses the last four coulomb counter readings to calculate the current. The current is updated every 1 s in NORMAL mode.

## CELL DETECTION

### Internal Short Detection

The device can detect an internal battery short by setting the [SE\_ISD] bit in Pack Configuration Register B. The bq28z560 compares the self-discharge current calculated based on *StateOfCharge()* in RELAX mode and *AverageCurrent()* measured in the system. The self-discharge is measured at 1-hour intervals. When the battery *SelfDischargeCurrent()* is less than a predefined ISD Current threshold, the ISD flag bit is set high.

### Tab Disconnection Detection

The bq28z560 detects tab disconnection by change in *StateOfHealth()*. This feature is enabled by setting the [SE\_TDD] bit in Pack Configuration Register B. The [TDD] bit is set in flag register when the ratio of current *StateOfHealth()* divided by the previous *StateOfHealth()* reported is less than TDD SOH percent.

## TEMPERATURE MEASUREMENT AND THE TS INPUT

The bq28z560 measures external temperature via the TS pin in order to supply battery temperature status information to the gas gauging algorithm and charger-control sections of the gauge. Alternatively, the gauge can also measure internal temperature via its on-chip temperature sensor. Refer to the ***Pack Configuration[TEMPS]*** control bit.

Regardless of which sensor is used for measurement, a system processor can request the current battery temperature by calling the *Temperature()* function. The temperature information is updated every 1 s in normal mode.

The bq28z560 external temperature sensing is optimized with the use of a high accuracy negative temperature coefficient (NTC) thermistor with  $R_{25} = 10\text{ K}\Omega \pm 1\%$  and  $B_{25/85} = 3435\text{ K}\Omega \pm 1\%$  (such as Semitec 103AT for measurement). [REFERENCE SCHEMATIC](#) shows additional circuit information on connecting this thermistor to the bq28z560.

## OVERTEMPERATURE INDICATION

### Overtemperature: Charge

If during charging *Temperature()* reaches the threshold of **OT Chg** for a period of **OT Chg Time** and *AverageCurrent()* > **Chg Current Threshold**, then based on System Configuration the following occurs:

- If the GPIO is set for CFET control, the GPIO output will transition low and with the associated external circuitry the CHG FET is turned OFF. When the temperature falls to **OT Chg Recovery**, the GPIO will transition high again and allow the charge FET to turn on.
- If **OT Chg Time** = 0, the feature is completely disabled.
- If GPIO is configured as Alert output and if the OTC\_EN bit in the Alert Configuration register is set to 1, the Alert pin (Pin 12) will transition low to signify a fault has occurred. The polarity of the alert output can be selected by setting the ALRT\_POL bit in the Alert Configuration register. The fault is cleared on read.

### Overtemperature: Discharge

If during discharging *Temperature()* reaches the threshold of **OT Dsg** for a period of **OT Dsg Time**, and *AverageCurrent()*  $\leq$  **Dsg Current Threshold**, then based on system Configuration the following occurs:

- If the above condition is satisfied, then the Dsg FET is turned off. When the temperature falls to **OT Dsg Recovery**, the Dsg FET is turned on.
- If **OT Dsg Time** = 0, the feature is completely disabled.
- If GPIO is configured as Alert output and if the OTD\_EN bit in the Alert Configuration register is set to 1, the Alert pin (Pin 12) will transition low to signify a fault has occurred. The polarity of the alert output can be selected by setting the ALRT\_POL bit in the Alert Configuration register. The fault is cleared on read.

## PROTECTION

### Overcharge Detector

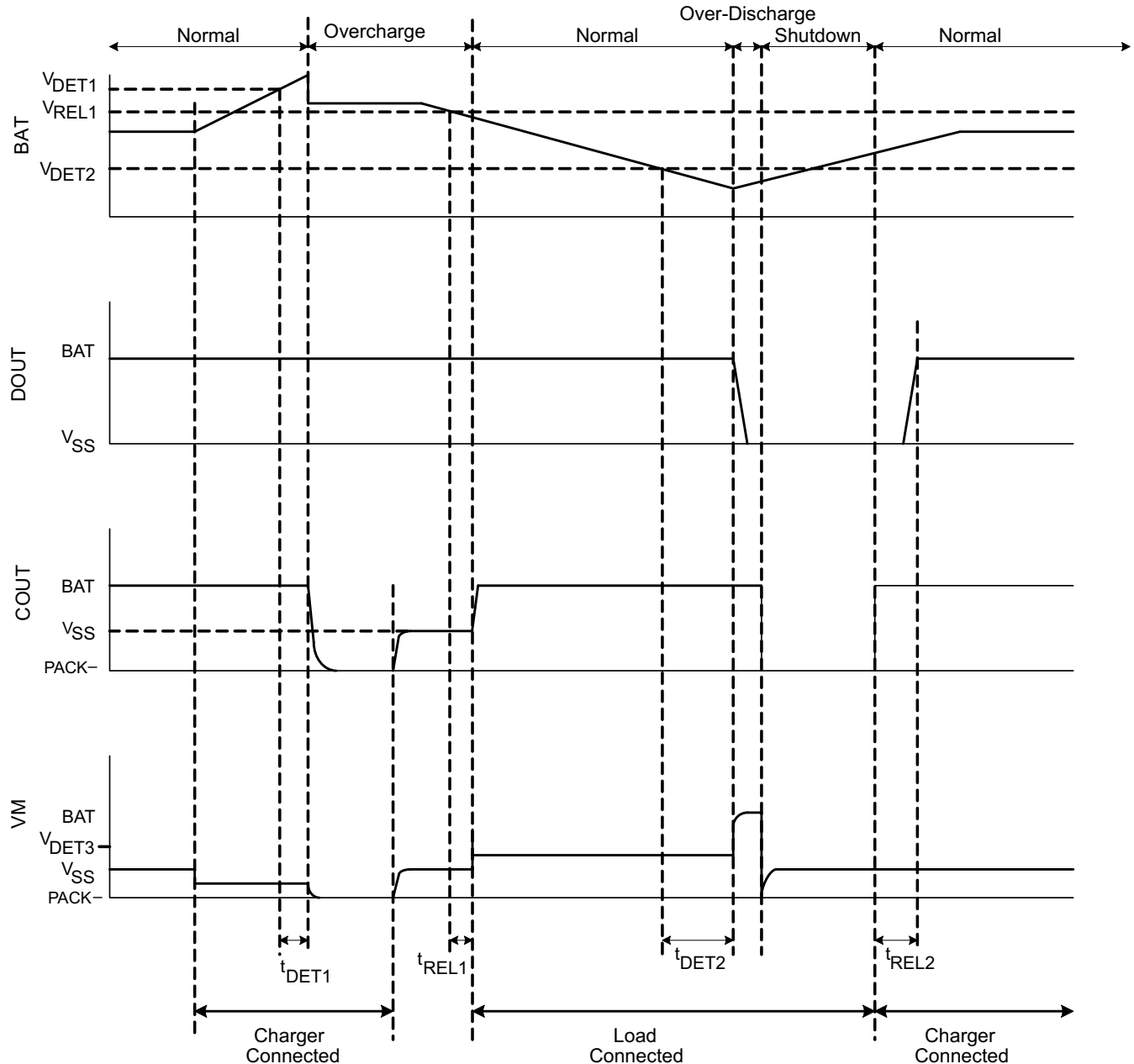
When charging a battery, if the  $V_{BAT}$  voltage becomes greater than the overcharge detection voltage ( $V_{DET1} = 4.25\text{ V typ}$ ) for a period up to the overcharge detection delay time ( $t_{DET1} = 1.00\text{ s typ}$ ), the bq28z560 detects the overcharge state of the battery, and the COUT pin transitions to a low level. This prohibits charging the battery by turning off the external charge control N-channel MOSFET.

In the overcharge state, if a charger is removed and a load is connected, the external charge control MOSFET conducts the load current through its parasitic body diode. If the  $V_{BAT}$  voltage becomes lower than the overcharge release voltage ( $V_{REL1} = 4.07\text{ V typ}$ ) for a period up to the overcharge release delay time ( $t_{REL1} = 8\text{ ms typ}$ ), the COUT pin transitions to a high level, enabling charge of the battery by turning on the external charge control N-channel MOSFET.

### Over-Discharge Detector

When discharging a battery, if the  $V_{BAT}$  voltage becomes lower than the over-discharge detection voltage ( $V_{DET2} = 2.3\text{ V typ}$ ) for a period up to the over-discharge detection delay time ( $t_{DET2} = 24\text{ ms typ}$ ), the bq28z560 detects the over-discharge state of the battery, and the DOUT pin transitions to a low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

In the over-discharge state, if a charger is connected, the external discharge control MOSFET conducts the charge current through its parasitic body diode. If the  $V_{BAT}$  voltage becomes greater than the over-discharge detection voltage ( $V_{DET2} = 2.3\text{ V typ}$ ) for a period up to the overcharge release delay time ( $t_{REL2} = 4\text{ ms typ}$ ), the DOUT pin transitions to a high-level enabling discharge of the battery by turning on the external discharge control N-channel MOSFET. After detecting over-discharge, the device stops all operations and enters standby, which reduces the current consumed by the IC to its lowest mode (standby current).

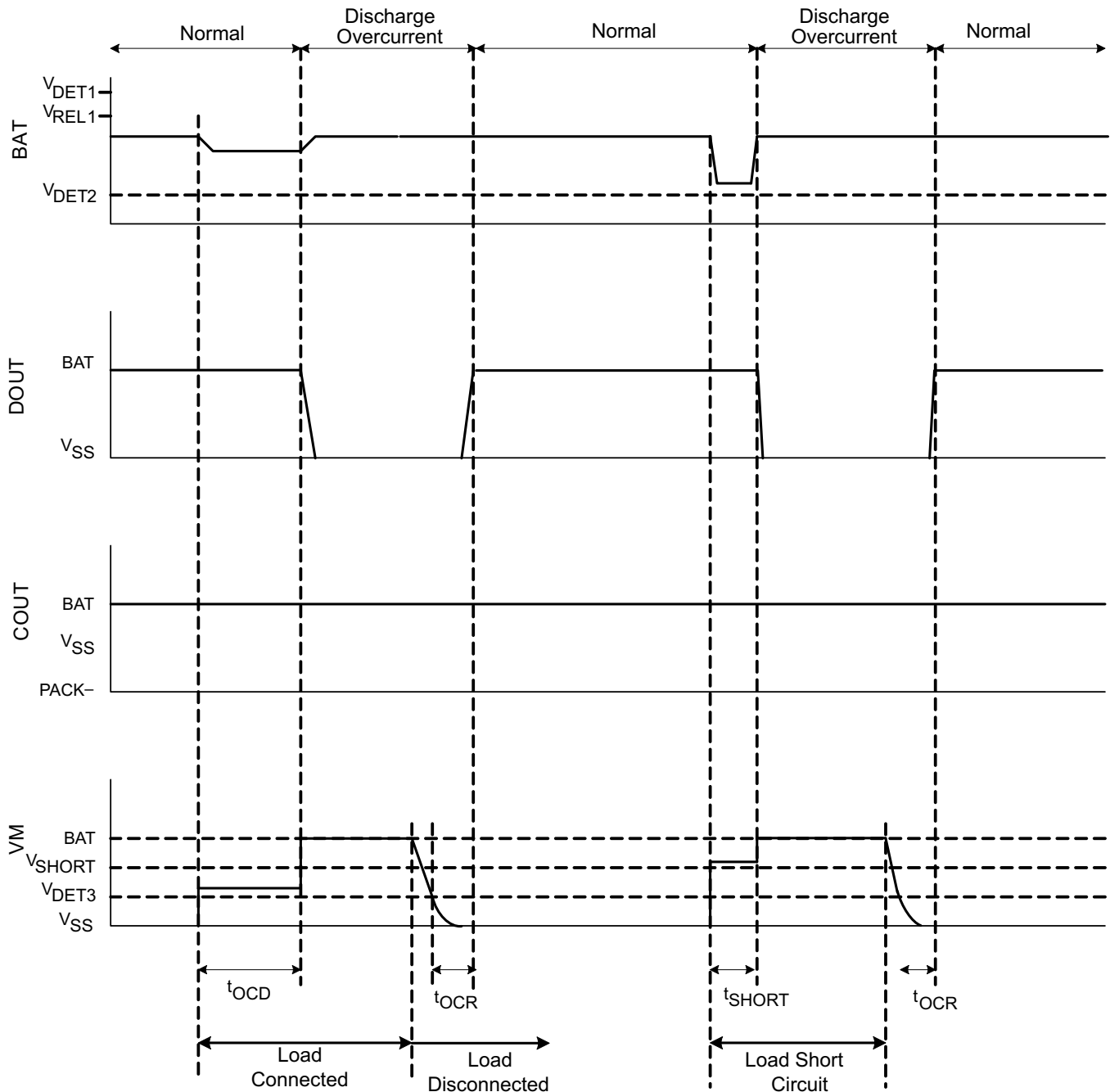


### Discharge Overcurrent Detector and Short-Circuit Detector

If the voltage across both protection MOSFETs ( $V_M - V_{SS}$ ) becomes higher than the discharge overcurrent detection voltage ( $V_{DET3} = 0.150\text{ V typ}$ ) for a period of up to the discharge overcurrent detection delay time ( $t_{DET3} = 12\text{ ms typ}$ ), the bq28z560 detects the discharge overcurrent state of the battery and the DOUT pin transitions to a low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

Additionally, if the voltage across both protection MOSFETs ( $V_M - V_{SS}$ ) becomes higher than the short-circuit voltage ( $V_{SHORT} = V_{BAT} - 0.9\text{ V typ}$ ) for a period of up to the discharge short-circuit detection delay time ( $t_{SHORT} = 400\ \mu\text{s typ}$ ), the bq28z560 detects short-circuit of the battery and the DOUT pin transitions to a low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

In both the discharge overcurrent and short-circuit states, an internal discharge overcurrent release resistor (20 k $\Omega$  typ) is turned on (switched in between VM and VSS), allowing the VM pin to be pulled down to the VSS potential if the load is released. If the  $V_M - V_{SS}$  voltage becomes lower than the discharge overcurrent release voltage ( $V_{DET3} = 0.150\text{ V typ}$ ) for a period up to the discharge overcurrent release delay time ( $t_{REL3} = 4\text{ ms typ}$ ), the discharge overcurrent release resistor is turned off and the DOUT pin transitions to a high level, enabling discharge of the battery by turning on the external discharge control N-channel MOSFET.





## Charge Overcurrent Detector

If the voltage across both protection MOSFETs ( $V_M - V_{SS}$ ) becomes more negative than the charge overcurrent detection voltage ( $V_{DET4} = -0.112\text{ V typ}$ ) for a period up to the charge overcurrent detection delay time ( $t_{DET4} = 12\text{ ms typ}$ ) due to an abnormal charging current or abnormal charging voltage, the bq28z560 detects the overcurrent charge state of the battery and the COUT pin transitions to a low level. This prohibits charging the battery by turning off the external charge control N-channel MOSFET. The bq28z560 releases from the charge overcurrent detection state on by detecting the connection of a load for a period up to the overcharge release delay time ( $t_{REL4} = 4\text{ ms typ}$ ).

**Table 2. Hardware Control Due to Fault Detection**

| Fault Condition                            | DOUT | COUT | Delay (typ) | Comment  |
|--|------|------|-------------|--|
| Over Charge Voltage Protection             | ON   | OFF  | 1 s         | Once BATHI occurs for longer than the specified duration (1s typ), the CHG FET is turned OFF, and bus communication is <i>not</i> valid, the system will support power to the load with current flow through the CHG FET parasitic diode. This can cause the cell to discharge. Once the cell voltage reaches the overcharge release voltage for the specified duration (8 ms typ) the CHG FET is turned ON and bus communication is valid.  |
| Over Current Protection during Charging    | ON   | OFF  | 12 ms       | If the cell is being charged with excessive current, the threshold will be based on a hardware limit measurement of $-112\text{ mV typ}$ across the CHG + DSG FET ( $V_M - V_{SS}$ ) for a duration longer than 12 ms (typ), the CHG FET is turned OFF and bus communication is <i>not</i> valid. This will prevent further charging of the cell. The setting of the CHG bit in the control Status register is dependent on the OC bit setting in the Flags Bit Definition register selection.<br>The FET bit in the Control between the charger is removed and cell voltage falls below the threshold for greater than 8 ms (typ). COUT is turned back ON. Once the host MCU takes corrective action OR if the battery charger is removed AND there is a load detected for a period of 4 ms (typ), the CHG FET is turned ON bus communication is valid. |
| Over Discharging Voltage Protection        | OFF  | ON   | 24 ms       | If the cell voltage falls to lower than 2.3 V for a duration of 24 ms (typ), the DSG FET is turned OFF, and bus communication is <i>not</i> valid. The system requires if the charger is connected and cell voltage rises above threshold for greater than 4 ms (typ). DOUT is turned back ON and bus communication is valid.  |
| Over Current Protection during Discharging | OFF  | ON   | 12 ms       | If the cell is being discharged with excessive current, the threshold will be based on a hardware limit measurement of $150\text{ mV typ}$ across the DSG + CHG FET ( $V_M - V_{SS}$ ) for a duration longer than 12 ms (typ), the DSG FET is turned OFF, and bus communication is <i>not</i> valid. This prevents further discharging of the cell, and the DSG bit in the control Status register will be set. If the drop across the DSG + CHG FET is less than the threshold OR there is <i>no</i> load detected for a duration of 4 ms (typ), the DSG FET is turned ON and bus communication is valid.   |
| Short-Circuit Protection                   | OFF  | ON   | 400 $\mu$ s | Detection of cell short circuit is measured at VM input. Shorted cell detection is $V_{BAT} - 0.9\text{ V}$ for greater than 400 $\mu$ s at VM terminal, and the DSG FET is turned OFF and bus communication is <i>not</i> valid. The DSG bit in the control Status register will be set. The system will turn the DSG FET ON if the voltage at VM is below 150 mV OR <i>no</i> load is detected.  |

## Gas Gauge Control of Discharge DOUT Pin

### Firmware Control of DOUT for Protection

The gas gauge firmware can override the hardware-based protection by forcing DOUT low to turn OFF the discharge FET. However, the firmware cannot override the hardware protection to force discharge.

The following conditions can enable firmware to force DOUT low:

1. BATLOW—Under Voltage protection using CUV settings. If the cell voltage drops below the firmware setting the DOUT pin transitions to a low to turn off the discharge FET. The Discharge FET is turned back on once the cell voltage rises above the set hysteresis.
2. OCD condition—If the average discharge current is greater than the set OCD current, the DOUT pin transitions low to turn of the Discharge FET. The Discharge FET is turned back on once the average current decreases below the set level.
3. OTD condition—The DOUT will transition low if the discharge current is flowing and the temperature is above th set OTD threshold.

4. The HOST\_DISCONNECT (DSG FET OFF) subcommand—This feature is useful for the system to disable the discharge FET from the battery pack if it fails to authenticate.

***The conditions stated above are ignored if there is charge current flow (body diode protection).***

### Gas Gauge Control of Charge FET

#### ***Firmware Control of Charge FET for Protection***

The gas gauge firmware control of the charge FET is achieved by using the GPIO with external circuitry. Typically the COUT pin is high and so to override this, the GPIO pin transitions low and the CHG FET gate drive is pulled low to turn OFF the Charge FET. The output of the GPIO pin will be released once the fault condition is removed.

The following parameters can be controlled through firmware (GPIO pin) providing the set thresholds are within the range of the hardware limits set by the protector.

1. BATHI—Overvoltage protection using COV settings. If the cell voltage exceeds the firmware setting the GPIO output transitions low to turn off the Charge FET. The Charge FET is turned back on once the cell voltage decays below the set hysteresis (GPIO output transitions high).
2. OCC condition—If the average current is greater than the set OCC current, the GPIO output transitions low to turn of the Charge FET. The Charge FET is turned back on once the average current decreases to the set level.
3. OTC condition—The CFET output will transition low if the charge current is flowing and the temperature is above the set OTC threshold or Charge Inhibit Temperature Hi. Alternatively, the CFET will *not* be allowed to turn ON if the temperature is above the set OTC or Charge Inhibit Temperature Hi thresholds and charge inhibit flag is set.

***The conditions stated above are ignored if there is discharge current flow (body diode protection).***

### Zero Voltage Charging

When the cell voltage is 0 V and if the charger voltage is above the minimum operating voltage for 0 V charging (1.2 V max), the COUT output transitions to a high level and charge current can flow.

### FET Control Protection

[Figure 6](#) shows an overview of the FET Control Protection operation.

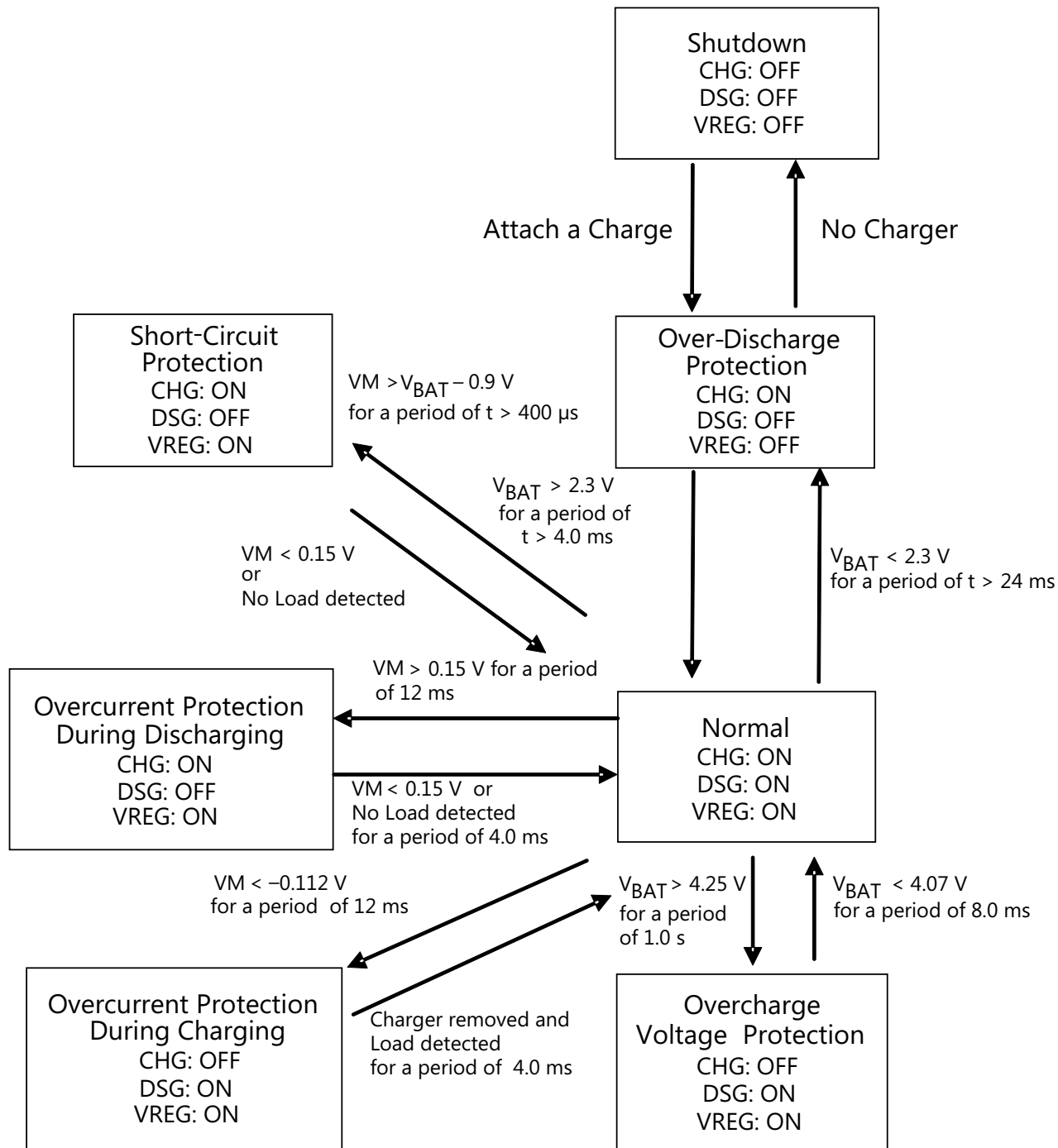


Figure 6. FET Control Protection

**NOTE**

When the CHG FET or DSG FET is turned OFF due to fault conditions, bus communication is *not* valid. The bus communication will only be activated by removal of the fault condition (see Table 2).

**Regulator**

Regulator out voltage is fixed at typically 2.5 V with a minimum output capacitance of 0.1  $\mu\text{F}$  (0.47  $\mu\text{F}$  typ). There is an internal current limit designed for 60 mA (typ) when output is shorted to GND. When  $V_{\text{BAT}}$  is over 8.0 V (typ), the regulator is turned off for the safety of the package dissipation.

## DATA COMMANDS

### STANDARD DATA COMMANDS

The bq28z560 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in [Table 3](#). Each protocol has specific means to access the data at each Command Code. DataRAM is updated and read by the gauge only once per second. Standard commands are accessible in normal operation mode.

**Table 3. Standard Commands**

| NAME                              |         | COMMAND CODE | UNITS       | SEALED ACCESS |
|-----------------------------------|---------|--------------|-------------|---------------|
| <i>Control()</i>                  | CNTL    | 0x00 / 0x01  | N/A         | R/W           |
| <i>AtRate()</i>                   | AR      | 0x02 / 0x03  | mA          | R/W           |
| <i>AtRateTimeToEmpty()</i>        | ARTTE   | 0x04 / 0x05  | Minutes     | R             |
| <i>Temperature()</i>              | TEMP    | 0x06 / 0x07  | 0.1K        | R             |
| <i>Voltage()</i>                  | VOLT    | 0x08 / 0x09  | mV          | R             |
| <i>Flags()</i>                    | FLAGS   | 0x0a / 0x0b  | N/A         | R             |
| <i>NominalAvailableCapacity()</i> | NAC     | 0x0c / 0x0d  | mAh         | R             |
| <i>FullAvailableCapacity()</i>    | FAC     | 0x0e / 0x0f  | mAh         | R             |
| <i>RemainingCapacity()</i>        | RM      | 0x10 / 0x11  | mAh         | R             |
| <i>FullChargeCapacity()</i>       | FCC     | 0x12 / 0x13  | mAh         | R             |
| <i>AverageCurrent()</i>           | AI      | 0x14 / 0x15  | mA          | R             |
| <i>TimeToEmpty()</i>              | TTE     | 0x16 / 0x17  | Minutes     | R             |
| <i>TimeToFull()</i>               | TTF     | 0x18 / 0x19  | Minutes     | R             |
| <i>StandbyCurrent()</i>           | SI      | 0x1a / 0x1b  | mA          | R             |
| <i>StandbyTimeToEmpty()</i>       | STTE    | 0x1c / 0x1d  | Minutes     | R             |
| <i>MaxLoadCurrent()</i>           | MLI     | 0x1e / 0x1f  | mA          | R             |
| <i>MaxLoadTimeToEmpty()</i>       | MLTTE   | 0x20 / 0x21  | Minutes     | R             |
| <i>AvailableEnergy()</i>          | AE      | 0x22 / 0x23  | mWhr / cWhr | R             |
| <i>AveragePower()</i>             | AP      | 0x24 / 0x25  | mW / cW     | R             |
| <i>TTEatConstantPower()</i>       | TTECP   | 0x26 / 0x27  | Minutes     | R             |
| <i>Internal_Temp()</i>            | INTTEMP | 0x28 / 0x29  | 0.1°K       | R             |
| <i>CycleCount()</i>               | CC      | 0x2a / 0x2b  | Counts      | R             |
| <i>StateOfCharge()</i>            | SOC     | 0x2c / 0x2d  | %           | R             |
| <i>StateOfHealth()</i>            | SOH     | 0x2e / 0x2f  | % / num     | R             |
| <i>PassedCharge()</i>             | PCHG    | 0x34 / 0x35  | mAh         | R             |
| <i>DOD0()</i>                     | DOD0    | 0x36 / 0x37  | HEX#        | R             |
| <i>SelfDischargeCurrent()</i>     | SDSG    | 0x38 / 0x39  | mA          | R             |

#### Control(): 0x00/0x01

Issuing a *Control()* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control()* command allows the system to control specific features of the bq28z560 during normal operation and additional features when the bq28z560 is in different access modes, as described in [Table 4](#).

**Table 4. Control() Subcommands**

| CNTL FUNCTION  | CNTL DATA | SEALED ACCESS | DESCRIPTION   |
|----------------|-----------|---------------|---|
| CONTROL_STATUS | 0x0000    | Yes           | Reports the status of DF Checksum, Hibernate, IT, etc.  |
| DEVICE_TYPE    | 0x0001    | Yes           | Reports the device type of 0x0541 (indicating bq28z560) |

**Table 4. Control() Subcommands (continued)**

| CNTL FUNCTION      | CNTL DATA | SEALED ACCESS | DESCRIPTION   |
|--------------------|-----------|---------------|---|
| FW_VERSION         | 0x0002    | Yes           | Reports the firmware version on the device type   |
| HW_VERSION         | 0x0003    | Yes           | Reports the hardware version of the device type   |
| Reserved           | 0x0004    | No            | Not to be used  |
| RESET_DATA         | 0x0005    | No            | Returns reset data  |
| Reserved           | 0x0006    | No            | Not to be used  |
| PREV_MACWRITE      | 0x0007    | No            | Returns previous MAC command code   |
| CHEM_ID            | 0x0008    | Yes           | Reports the chemical identifier of the Impedance Track configuration                    |
| BOARD_OFFSET       | 0x0009    | No            | Forces the device to measure and store the board offset                                 |
| CC_OFFSET          | 0x000A    | No            | Forces the device to measure and internal CC offset                                     |
| CC_OFFSET_SAVE     | 0x000B    | No            | Forces the device to store the internal CC offset                                       |
| DF_VERSION         | 0x000C    | Yes           | Reports the data flash version on the device  |
| SET_FULLSLEEP      | 0x0010    | No            | Set the <i>[FULLSLEEP]</i> bit in Control Status register to 1                          |
| SET_HIBERNATE      | 0x0011    | Yes           | Forces CONTROL_STATUS <i>[HIBERNATE]</i> to 1   |
| CLEAR_HIBERNATE    | 0x0012    | Yes           | Forces CONTROL_STATUS <i>[HIBERNATE]</i> to 0   |
| SET_SHUTDOWN       | 0x0013    | Yes           | Forces CONTROL_STATUS <i>[SHUTDOWN]</i> to 1. Allows system to enter into SHUTDOWN mode |
| CLEAR_SHUTDOWN     | 0x0014    | Yes           | Forces CONTROL_STATUS <i>[SHUTDOWN]</i> to 0  |
| SET_HDQINTEN       | 0x0015    | Yes           | Forces CONTROL_STATUS <i>[HDQIntEn]</i> to 1  |
| CLEAR_HDQINTEN     | 0x0016    | Yes           | Forces CONTROL_STATUS <i>[HDQIntEn]</i> to 0  |
| STATIC_CHEM_CHKSUM | 0x0017    | Yes           | Calculates chemistry checksum   |
| HOST_DISCONNECT    | 0x0018    | Yes           | Forces the DOUT pin low to disable discharge.   |
| HOST_CONNECT       | 0x0019    | Yes           | Clears DSGFETOFF, allowing DOUT to go high if no other conditions force it low          |
| SEALED             | 0x0020    | No            | Places the bq28z560 in SEALED access mode   |
| IT_ENABLE          | 0x0021    | No            | Enables the Impedance Track algorithm   |
| CAL_ENABLE         | 0x002d    | No            | Toggle bq28z560 calibration mode  |
| RESET              | 0x0041    | No            | Forces a full reset of the bq28z560   |
| EXIT_CAL           | 0x0080    | No            | Exit bq28z560 calibration mode  |
| ENTER_CAL          | 0x0081    | No            | Enter bq28z560 calibration mode   |
| OFFSET_CAL         | 0x0082    | No            | Reports internal CC offset in calibration mode  |

**CONTROL\_STATUS: 0x0000**

Instructs the gas gauge to return status information to Control addresses 0x00/0x01. The status word includes the following information.

**Table 5. CONTROL\_STATUS Flags**

|           | Bit 7     | Bit 6     | Bit 5     | Bit 4   | Bit 3 | Bit 2   | Bit 1 | Bit 0    |
|-----------|-----------|-----------|-----------|---------|-------|---------|-------|----------|
| High Byte | DSGFETOFF | FAS       | SS        | CALMODE | CCA   | BCA     | CSV   | HDQIntEn |
| Low Byte  | SHUTDOWN  | HIBERNATE | FULLSLEEP | SLEEP   | LDMD  | RUP_DIS | VOK   | QEN      |

DSGFETOFF = State bit indicating the DISCHARGE FET has been disabled by HOST (HOST\_DISCONNECT).

FAS = Status bit indicating the bq28z560 is in FULL ACCESS SEALED state. Active when set.

SS = Status bit indicating the bq28z560 is in the SEALED state. Active when set.

CALMODE = Status bit indicating the calibration function is active. True when set. Default is 0.

CCA = Status bit indicating the bq28z560 coulomb counter Calibration routine is active. The CCA routine will take place approximately 1 minute after the initialization and periodically as gauging conditions change. Active when set.

BCA = Status bit indicating the bq28z560 Board Calibration routine is active. Active when set.

CSV = Status bit indicating a valid data flash checksum has been generated. Active when set.

- HDQIntEn = Status bit indicating the HDQ interrupt function is active. True when set. Default is 0.
- SHUTDOWN = Status bit indicating the bq28z560 is in SHUTDOWN mode. True when set. Default is 0.
- HIBERNATE = Status bit indicating a request for entry into HIBERNATE from SLEEP mode has been issued. True when set. Default is 0. Control bit when set will put the bq28z560 into the lower power state of SLEEP mode. It is not possible to monitor this bit.
- FULLSLEEP = Status bit indicating the bq28z560 is in FULLSLEEP mode. True when set. The state can be detected by monitoring the power used by the bq28z560 because any communication will automatically clear it.
- SLEEP = Status bit indicating the bq28z560 is in SLEEP mode. True when set.
- LDMD = Status bit indicating the bq28z560 Impedance Track algorithm using *constant-power* mode. True when set. Default is 0 (*constant-current* mode).
- RUP\_DIS = Status bit indicating the bq28z560 Ra table updates are disabled. True when set.
- VOK = Status bit indicating cell voltages are OK for Qmax updates. True when set.
- QEN = Status bit indicating the bq28z560 Qmax updates are enabled. True when set.

### Control(): 0x00/0x01

Issuing a *Control()* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control()* command allows the system to control specific features of the bq28z560 during normal operation and additional features when the device is in access modes as described in [Table 6](#).

**Table 6. Control() Subcommands**

| CNTL FUNCTION   | CNTL DATA | SEALED ACCESS | DESCRIPTION   |
|-----------------|-----------|---------------|---|
| SET_FULLSLEEP   | 0x0010    | Yes           | Set the [FULLSLEEP] bit in Control Status register to 1                       |
| SET_HIBERNATE   | 0x0011    | Yes           | Forces CONTROL_STATUS [HIBERNATE] to 1  |
| CLEAR_HIBERNATE | 0x0012    | Yes           | Forces CONTROL_STATUS [HIBERNATE] to 0  |
| SET_SHUTDOWN    | 0x0013    | Yes           | Forces CONTROL_STATUS [SHUTDOWN] to 1   |
| CLEAR_SHUTDOWN  | 0x0014    | Yes           | Forces CONTROL_STATUS [SHUTDOWN] to 0   |
| HOST_DISCONNECT | 0x0018    | Yes           | Forces the DOUT pin low to disable discharge.                                 |
| HOST_CONNECT    | 0x0019    | Yes           | Clears DSGFETOFF allowing DOUT to go high if no other conditions force it low |

### DEVICE\_TYPE: 0x0001

Instructs the gas gauge to return the device type to addresses 0x00/0x01.

### FW\_VERSION: 0x0002

Instructs the gas gauge to return the firmware version to addresses 0x00/0x01. The bq28z560 firmware version return is 0x0214.

### HW\_VERSION: 0x0003

Instructs the gas gauge to return the hardware version to addresses 0x00/0x01. For bq28z560, 0x0060 is returned. For a firmware upgrade from bq28z560, 0x0000 or 0x0060 is returned.

### RESET\_DATA: 0x0005

Instructs the gas gauge to return the number of resets performed to addresses 0x00/0x01.

### PREV\_MACWRITE: 0x0007

Instructs the gas gauge to return the previous command written to addresses 0x00/0x01. The value returned is limited to less than 0x0020.

### CHEM\_ID: 0x0008

Instructs the gas gauge to return the chemical identifier for the Impedance Track configuration to addresses 0x00/0x01.

**BOARD\_OFFSET: 0x0009**

Instructs the gas gauge to calibrate board offset. During board offset calibration the *[BCA]* bit is set.

**CC\_OFFSET: 0x000A**

Instructs the gas gauge to calibrate coulomb counter offset. During calibration the *[CCA]* bit is set.

**CC\_OFFSET\_SAVE: 0x000B**

Instructs the gas gauge to save the calibration coulomb counter offset after calibration.

**DF\_VERSION: 0x000C**

Instructs the gas gauge to return the data flash version to addresses 0x00/0x01.

**SET\_FULLSLEEP: 0x0010**

Instructs the gas gauge to set the FULLSLEEP bit in Control Status register to 1. This allows the gauge to enter the FULLSLEEP power mode after the transition to SLEEP power state is detected. In FULLSLEEP mode, less power is consumed by disabling an oscillator circuit used by the communication engines. For HDQ communication one host message will be dropped. For I<sup>2</sup>C communications the first I<sup>2</sup>C message will incur a 6–8 millisecond clock stretch while the oscillator is started and stabilized. A communication to the device in FULLSLEEP will force the part back to the SLEEP mode.

**SET\_HIBERNATE: 0x0011**

Instructs the gas gauge to force the CONTROL\_STATUS [HIBERNATE] bit to 1. This enables the gauge to enter the HIBERNATE power mode after the transition to SLEEP power state is detected and the required conditions are met. The [HIBERNATE] bit is automatically cleared upon exiting from HIBERNATE mode.

**CAUTION**

Do not use the *Control()* subcommand SET\_HIBERNATE to disable HIBERNATE mode. To disable HIBERNATE mode, Hibernate Voltage and Current must be set to 0 in the data flash.

If HIBERNATE mode is initiated, always ensure that the bus line is pulled high by an external resistor. It is important to prevent the bus line from being pulled low by an external signal on the line when in HIBERNATE mode; otherwise, the device may latch and a cold power cycle is required.

**CLEAR\_HIBERNATE: 0x0012**

Instructs the gas gauge to force the **CONTROL\_STATUS [HIBERNATE]** bit to 0. This prevents the gauge from entering the HIBERNATE power mode after the transition to SLEEP power state is detected. It can also be used to force the gauge out of HIBERNATE mode.

**SET\_SHUTDOWN: 0x0013**

Sets the **CONTROL\_STATUS [SHUTDOWN]** bit to 1, thereby enabling the gas gauge to enter SHUTDOWN mode, depending on whether the conditions are met for gas gauge shutdown or not. The delay for shutdown is 1 s, providing there is no charging current detected.

**CLEAR\_SHUTDOWN: 0x0014**

Disables the shutdown by setting this bit to 1, thereby forcing **CONTROL\_STATUS [SHUTDOWN]** to 0.

**SET\_HDQINTEN: 0x0015**

Instructs the gas gauge to set the **CONTROL\_STATUS [HDQIntEn]** bit to 1. This enables the HDQ Interrupt function. When this subcommand is received, the device will detect any of the interrupt conditions and assert the interrupt at 1-s intervals until the CLEAR\_HDQINTEN command is received or the count of HDQHostIntrTries has lapsed (default 3).



**CLEAR\_HDQINTEN: 0x0016**

Instructs the gas gauge to set the **CONTROL\_STATUS [HDQIntEn]** bit to 0. This disables the HDQ Interrupt function.

**STATIC\_CHEM\_DF\_CHKSUM: 0x0017**

Instructs the gas gauge to calculate chemistry checksum as a 16-bit unsigned integer sum of all static chemistry data. The most significant bit (MSB) of the checksum is masked yielding a 15-bit checksum. This checksum is compared with value stored in the data flash *Static Chem DF Checksum*. If the value matches, the MSB will be cleared to indicate pass. If it does not match, the MSB will be set to indicate failure.

**DSG FET OFF (HOST\_DISCONNECT): 0x0018**

Instructs the gas gauge to force the protection DOUT pin to low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

**DSG FET ON (HOST\_CONNECT): 0x0019**

Instructs the gas gauge to release the DOUT high if no other conditions exist to force the pin low. This allows discharging the battery by turning on the external discharge control N-channel MOSFET.

**SEALED: 0x0020**

Instructs the gas gauge to transition from UNSEALED state to SEALED state. The gas gauge should always be set to SEALED state for use in customers' end equipment.

**IT ENABLE: 0x0021**

This command forces the gas gauge to begin the Impedance Track algorithm, sets Bit 2 of **UpdateStatus**, and causes the [VOK] and [QEN] flags to be set in the CONTROL\_STATUS register. [VOK] is cleared if the voltages are not suitable for a Qmax update. Once set, [QEN] cannot be cleared. This command is only available when the gas gauge is UNSEALED and is typically enabled at the last step of production after a system test is completed.

The CFET and DFET are *not* automatically enabled until the IT Enable bit is sent. Prior to this, to control these FETs, a command must be sent to set the CHGFET and DSGFET bits in the Flags Bit Definitions Register to enable the COUT and DOUT, respectively.

**CAL\_ENABLE: 0x002D**

This command toggles the CalEn bit in the PACK Configuration register.

**RESET: 0x0041**

This command instructs the gas gauge to perform a full reset. This command is only available when the gas gauge is UNSEALED.

**EXIT\_CAL: 0x0080**

This command instructs the gas gauge to exit CALIBRATION mode.

**ENTER\_CAL: 0x0081**

This command instructs the gas gauge to enter CALIBRATION mode.

**OFFSET\_CAL: 0x0082**

This command instructs the gas gauge to perform offset calibration.

**AtRate(): 0x02/0x03**

The *AtRate()* read-/write-word function is the first half of a two-function command call-set used to set the AtRate value in calculations made by the *AtRateTimeToEmpty()* function. The *AtRate()* units are in mA.

The *AtRate()* value is a signed integer with negative values interpreted as a discharge current value. The *AtRateTimeToEmpty()* function returns the predicted operating time at the *AtRate* value of discharge. The default value for *AtRate()* is zero and will force *AtRateTimeToEmpty()* to return 65,535. Both the *AtRate()* and *AtRateTimeToEmpty()* commands should only be used in NORMAL mode.

#### **AtRateTimeToEmpty(): 0x04/0x05**

This read-only function returns an unsigned integer value of the predicted remaining operating time if the battery is discharged at the *AtRate()* value in minutes with a range of 0 to 65,534. A value of 65,535 indicates *AtRate()* = 0. The gas gauge updates *AtRateTimeToEmpty()* within 1 s after the system sets the *AtRate()* value. The gas gauge automatically updates *AtRateTimeToEmpty()* based on the *AtRate()* value every 1 s. The *AtRate()* and *AtRateTimeToEmpty()* commands should only be used in NORMAL mode.

#### **Temperature(): 0x06/0x07**

This read-only function returns an unsigned integer value of the battery temperature in units of 0.1K measured by the gas gauge.

#### **Voltage(): 0x08/0x09**

This read-only function returns an unsigned integer value of the measured cell-pack voltage in mV with a range of 0 to 6000 mV.

#### **Flags(): 0x0a/0x0b**

This read-only function returns the contents of the gas-gauge status register, depicting the current operating status.

**Table 7. Flags Bit Definitions**

|           | <b>Bit 7</b> | <b>Bit 6</b> | <b>Bit 5</b> | <b>Bit 4</b> | <b>Bit 3</b> | <b>Bit 2</b> | <b>Bit 1</b> | <b>Bit 0</b> |
|-----------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| High Byte | OT           | OC           | BATHI        | BATLO        | CHG_INH      | ALRT         | FC           | CHG          |
| Low Byte  | OCVTAKEN     | ISD          | TDD          | CHGFET       | DSGFET       | SOC1         | SOCF         | DSG          |

These fault flags will only clear if the fault condition is removed:

- OT = Over-Temperature in Charge or Discharge condition is detected. True when set.
- OC = Overcurrent in Charge or Discharge condition is detected. True when set.
- BATHI = Battery High bit indicating a high battery voltage condition. Refer to the data flash **BATTERY HIGH** parameters for threshold settings.
- BATLO = Battery Low bit indicating a low battery voltage condition. Refer to the data flash **BATTERY LOW** parameters for threshold settings.
- CHG\_INH = Charge Inhibit indicates the temperature is outside the range [*Charge Inhibit Temp Low, Charge Inhibit Temp High*]. True when set.
- ALRT = Indicates there is an Alert in the system. True when set.
- FC = Full-charged is detected. FC is set when charge termination is reached and *FC Set%* = -1 (see [CHARGING AND CHARGE TERMINATION INDICATION](#) for details) or State of Charge is larger than *FC Set%* and *FC Set%* is not -1. True when set.
- CHG = (Fast) charging allowed. True when set.
- OCVTAKEN = Cleared on entry to RELAX mode and set to 1 when OCV measurement is performed in RELAX.
- ISD = Internal Short is detected. True when set.
- TDD = Tab Disconnect is detected. True when set.
- CHGFET= Indicates the state of the firmware CFET control. True when set to 1.
- DSGFET= Indicates the state of the firmware DFET control. True when set to 1.
- SOC1 = State-of-Charge-Threshold 1 (**SOC1 Set**) reached. True when set.
- SOCF = State-of-Charge-Threshold Final (**SOCF Set %**) reached. True when set.
- DSG = Discharging detected. True when set.

**NominalAvailableCapacity(): 0x0c/0x0d**

This read-only command pair returns the uncompensated (less than C/20 load) battery capacity remaining. Units are mAh.

**FullAvailableCapacity(): 0x0e/0x0f**

This read-only command pair returns the uncompensated (less than C/20 load) capacity of the battery when fully charged. Units are mAh. *FullAvailableCapacity()* is updated at regular intervals, as specified by the Impedance Track algorithm.

**RemainingCapacity(): 0x10/0x11**

This read-only command pair returns the compensated battery capacity remaining. Units are mAh.

**FullChargeCapacity(): 0x12/13**

This read-only command pair returns the compensated capacity of the battery when fully charged. Units are mAh. *FullChargeCapacity()* is updated at regular intervals, as specified by the Impedance Track algorithm.

**AverageCurrent(): 0x14/0x15**

This read-only command pair returns a signed integer value that is the average current flow through the sense resistor. It is updated every 1 s. Units are mA.

**TimeToEmpty(): 0x16/0x17**

This read-only function returns an unsigned integer value of the predicted remaining battery life at the present rate of discharge, in minutes. A value of 65,535 indicates battery is not being discharged.

**TimeToFull(): 0x18/0x19**

This read-only function returns an unsigned integer value of predicted remaining time until the battery reaches full charge, in minutes, based upon *AverageCurrent()*. The computation accounts for the taper current time extension from the linear TTF computation based on a fixed *AverageCurrent()* rate of charge accumulation. A value of 65,535 indicates the battery is not being charged.

**StandbyCurrent(): 0x1a/0x1b**

This read-only function returns a signed integer value of the measured standby current through the sense resistor. The *StandbyCurrent()* is an adaptive measurement. Initially it reports the standby current programmed in **Initial Standby**, and after spending some time in standby, reports the measured standby current.

The register value is updated every 1 s when the measured current is above the **Deadband** and is less than or equal to 2 x **Initial Standby**. The first and last values that meet this criteria are not averaged in, since they may not be stable values. To approximate a 1-minute time constant, each new *StandbyCurrent()* value is computed by taking approximate 93% weight of the last standby current and approximate 7% of the current measured average current.

**StandbyTimeToEmpty(): 0x1c/0x1d**

This read-only function returns an unsigned integer value of the predicted remaining battery life at the standby rate of discharge, in minutes. The computation uses *Nominal Available Capacity* (NAC), the uncompensated remaining capacity, for this computation. A value of 65,535 indicates the battery is not being discharged.

**MaxLoadCurrent(): 0x1e/0x1f**

This read-only function returns a signed integer value, in units of mA, of the maximum load conditions. The *MaxLoadCurrent()* is an adaptive measurement, which is initially reported as the maximum load current programmed in **Initial Max Load Current**. If the measured current is ever greater than **Initial Max Load Current**, then *MaxLoadCurrent()* updates to the new current. *MaxLoadCurrent()* is reduced to the average of the previous value and **Initial Max Load Current** whenever the battery is charged to full after a previous discharge to an SOC less than 50%. This prevents the reported value from maintaining an unusually high value.

**MaxLoadTimeToEmpty(): 0x20/0x21**

This read-only function returns an unsigned integer value of the predicted remaining battery life at the maximum load current discharge rate, in minutes. A value of 65,535 indicates that the battery is not being discharged.

**AvailableEnergy(): 0x22/0x23**

This read-only function returns an unsigned integer value of the predicted charge or energy remaining in the battery. The value is reported in units of mW (**Design Energy Scale = 1**) or cW (**Design Energy Scale = 10**).

**AveragePower(): 0x24/0x25**

This read-word function returns an unsigned integer value of the average power of the current discharge. It is negative during discharge and positive during charge. A value of 0 indicates that the battery is not being discharged. The value is reported in units of mW (**Design Energy Scale = 1**) or cW (**Design Energy Scale = 10**).

**TimeToEmptyAtConstantPower(): 0x26/0x27**

This read-only function returns an unsigned integer value of the predicted remaining operating time if the battery is discharged at the *AveragePower()* value in minutes. A value of 65,535 indicates *AveragePower()* = 0. The gas gauge automatically updates *TimeToEmptyatConstantPower()* based on the *AveragePower()* value every 1 s.

**Internal\_Temp(): 0x28/0x29**

This read-only function returns an unsigned integer value of the measured internal temperature of the device in units of 0.1K measured by the gas gauge.

**CycleCount(): 0x2a/0x2b**

This read-only function returns an unsigned integer value of the number of cycles the battery has experienced with a range of 0 to 65,535. One cycle occurs when accumulated discharge  $\geq$  **CC Threshold**.

**StateOfCharge(): 0x2c/0x2d**

This read-only function returns an unsigned integer value of the predicted remaining battery capacity expressed as a percentage of *FullChargeCapacity()*, with a range of 0 to 100%.

**StateOfHealth(): 0x2e/0x2f**

0x2e SOH percentage: This read-only function returns an unsigned integer value, expressed as a percentage of the ratio of predicted *FCC(25°C, SOH current rate)* over the *DesignCapacity()*. The *FCC(25°C, SOH current rate)* is the calculated full charge capacity at 25°C and the SOH current rate, which is specified in the data flash (State of Health Load). The range of the returned SOH percentage is 0x00 to 0x64, indicating 0 to 100%, correspondingly.

**PassedCharge(): 0x34/0x35**

This signed integer indicates the amount of charge passed through the sense resistor since the last Impedance Track simulation in mAh.

**DOD0(): 0x36/0x37**

This unsigned integer indicates the depth of discharge during the most recent OCV reading.

**SelfDischargeCurrent(): 0x38/0x39**

This read-only command pair returns the signed integer value that estimates the battery self discharge current.

## EXTENDED DATA COMMANDS

Extended commands offer additional functionality beyond the standard set of commands. They are used in the same manner; however, unlike standard commands, extended commands are not limited to 2-byte words. The number of command bytes for a given extended command ranges in size from single to multiple bytes, as specified in [Table 8](#). For details on the SEALED and UNSEALED states, see [ACCESS MODES](#).

**Table 8. Extended Commands**

| NAME  |          | COMMAND CODE | UNITS | SEALED ACCESS <sup>(1)</sup> <sup>(2)</sup> | UNSEALED ACCESS <sup>(1)</sup> <sup>(2)</sup> |
|---|----------|--------------|-------|---|---|
| Reserved  | RSVD     | 0x38...0x39  | N/A   | R   | R   |
| <i>PackConfig()</i>   | PCR      | 0x3a / 0x3b  | HEX#  | R   | R   |
| <i>DesignCapacity()</i>   | DCAP     | 0x3c / 0x3d  | mAh   | R   | R   |
| <i>DataFlashClass()</i> <sup>(2)</sup>                            | DFCLS    | 0x3e         | N/A   | N/A   | R/W   |
| <i>DataFlashBlock()</i> <sup>(2)</sup>                            | DFBLK    | 0x3f         | N/A   | R/W   | R/W   |
| <i>BlockData()</i> / <i>Authenticate()</i> <sup>(3)</sup>         | A/DF     | 0x40...0x53  | N/A   | R/W   | R/W   |
| <i>BlockData()</i> / <i>AuthenticateChecksum()</i> <sup>(3)</sup> | ACKS/DFD | 0x54         | N/A   | R/W   | R/W   |
| <i>BlockData()</i>  | DFD      | 0x55...0x5f  | N/A   | R   | R/W   |
| <i>BlockDataChecksum()</i>  | DFDCKS   | 0x60         | N/A   | R/W   | R/W   |
| <i>BlockDataControl()</i>   | DFDCNTL  | 0x61         | N/A   | N/A   | R/W   |
| Reserved  | RSVD     | 0x62...0x69  | N/A   | R   | R   |
| <i>BatAlertConfig()</i>   | BAC      | 0x6a/0x6b    | N/A   | R/W   | R/W   |
| <i>BatAlertStatus()</i>   | BAS      | 0x6c/0x6d    | N/A   | R/W   | R/W   |
| Reserved  | RSVD     | 0x6e...0x7f  | N/A   | R   | R   |

(1) SEALED and UNSEALED states are entered via commands to *Control()* 0x00/0x01.

(2) In SEALED mode, data flash CANNOT be accessed through commands 0x3e and 0x3f.

(3) The *BlockData()* command area shares functionality for accessing general data flash and for using Authentication. See [AUTHENTICATION](#) for details.

### **PackConfig(): 0x3a/0x3b**

SEALED and UNSEALED Access: This command returns the value stored in **Pack Configuration**, which is expressed in hex value.

### **DesignCapacity(): 0x3c/0x3d**

SEALED and UNSEALED Access: This command returns the value stored in **Design Capacity**, which is expressed in mAh. This is intended to be the theoretical or nominal capacity of a new pack, but has no bearing on the operation of the gas gauge functionality.

### **DataFlashClass(): 0x3e**

This command sets the data flash class to be accessed. The class to be accessed should be entered in hexadecimal.

SEALED Access: This command is not available in SEALED mode.

### **DataFlashBlock(): 0x3f**

UNSEALED Access: This command sets the data flash block to be accessed. When 0x00 is written to *BlockDataControl()*, *DataFlashBlock()* holds the block number of the data flash to be read or written. Example: writing a 0x00 to *DataFlashBlock()* specifies access to the first 32-byte block, and a 0x01 specifies access to the second 32-byte block, and so on.

Example of reading Device Name

To read the **DeviceName** in UNSEALED mode, set the *BlockDataControl()* (command 0x61) to a 1. This is similar to how the manufacturer information block works. Since the Device Name is 20 bytes, the device name will be followed by null bytes.

**SEALED Access:** This command directs which data flash block will be accessed by the *BlockData()* command. Writing a 0x00 to *DataFlashBlock()* specifies the *BlockData()* command will transfer authentication data. Issuing a 0x01, 0x02, or 0x03 instructs the *BlockData()* command to transfer **Manufacturer Info Block A or B**, respectively.

Example of reading Device Name

To read the **DeviceName** when in SEALED mode, set the *DataFlashBlock()* (command 0x3f) to 0x05, and read the device name from the *BlockData()* commands.

In general, there will be at least 12 null characters since the data flash field is limited to 20 bytes and the seal mode block has 32 bytes of space

### **BlockData(): 0x40...0x5f**

This command range is used to transfer data for data flash class access. This command range is the 32-byte data block used to access **Manufacturer Info Block A or B**. **Manufacturer Info Block A** is read-only for the sealed access. UNSEALED access is read/write.

### **BlockDataChecksum(): 0x60**

The host system should write this value to inform the device that new data is ready for programming into the specified data flash class and block.

**UNSEALED Access:** This byte contains the checksum on the 32 bytes of block data read or written to data flash. The least-significant byte of the sum of the data bytes written must be complemented ( $[255 - x]$  for  $x$  the 8-bit summation of the *BlockData()* (0x40 to 0x5F) on a byte-by-byte basis) before being written to 0x60.

**SEALED Access:** This byte contains the checksum for the 32 bytes of block data written to **Manufacturer Info Block A or B**. The least-significant byte of the sum of the data bytes written must be complemented ( $[255 - x]$  for  $x$  the 8-bit summation of the *BlockData()* (0x40 to 0x5F) on a byte-by-byte basis) before being written to 0x60.

### **BlockDataControl(): 0x61**

**UNSEALED Access:** This command is used to control data flash access mode. The value determines the data flash to be accessed. Writing 0x00 to this command enables *BlockData()* to access general data flash.

**SEALED Access:** This command is not available in SEALED mode.

### **Reserved(): 0x62...0x69**

Reserved.

### **BatAlertConfig(): 0x6a/0x6b**

The *BatAlertConfig()* register can be written to set which faults once detected will trigger an Alert. The data flash value for *BatAlertConfig()* is used to initialize this value.

**Table 9. BatAlertConfig() Definitions**

| High Byte        | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|------------------|--------|--------|--------|--------|--------|--------|-------|-------|
| BatAlertConfig() | UTC_EN | UTD_EN | RSVD   | RSVD   | RSVD   | RSVD   | RSVD  | RSVD  |

| Low Byte         | Bit 7  | Bit 6  | Bit 5    | Bit 4    | Bit 3 | Bit 2   | Bit 1  | Bit 0  |
|------------------|--------|--------|----------|----------|-------|---------|--------|--------|
| BatAlertConfig() | OTC_EN | OTD_EN | BATHI_EN | BATLO_EN | RSVD  | SOC1_EN | OCC_EN | OCD_EN |

UTC\_EN = Enables alert for Over Temperature Charge Current when set to 1. Default is 1.

UTD\_EN = Enables alert for Over Temperature Discharge Current when set to 1. Default is 1.

RSVD = Reserved. Default = 0.

OTC\_EN = Enables alert for Over Temperature Charge Current when set to 1. Default is 1.

OTD\_EN = Enables alert for Over Temperature Discharge Current when set to 1. Default is 1.

BATHI\_EN= Enables alert for Battery High Condition when set to 1. Default is 0.

BATLO\_EN = Enables alert for Battery Low Condition when set to 1. Default is 0.



RSVD = Reserved. Default = 0.

SOC1\_EN = Enables alert for State-of-Charge-Threshold 1 (SOC1 Set) reached. True when set. Default is 1

OCC\_EN = Enables alert for Over Current Charge Condition when set to 1. Default is 0.

OCD\_EN= Enables alert for Over Current DISCHARGE Condition when set to 1. Default is 0.

### ***BatAlertStatus(): 0x6c/0x6d***

The *BatAlertStatus()* register allows reading the safety conditions that triggered the alert. If the Pack Configuration [CLR\_READ] is set to 1, *BatAlertStatus()* will be reset, and the alert assertion removed immediately. Otherwise, the *BatAlertStatus()* flags will clear only after the safety flag has reset, and the alert assertion clears once all flags in *BatAlertStatus()* have cleared.

**Table 10. BatAlertStatus() Definitions**

| High Byte        | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|------------------|--------|--------|--------|--------|--------|--------|-------|-------|
| BatAlertStatus() | UTC    | UTD    | RSVD   | RSVD   | RSVD   | RSVD   | RSVD  | RSVD  |

| Low Byte         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| BatAlertStatus() | OTC   | OTD   | BATHI | BATLO | RSVD  | SOC1  | OCC   | OCD   |

The following functions can be detected for fault conditions when set in the BatAlert Configuration register. The fault can be indicated on Alert pin (if configured) but *not* differentiated because of the OR logic.

UTC = Detected Under Temperature Charge Current when set to 1.

UTD = Detected Under Temperature Discharge Current when set to 1.

RSVD = Reserved. Default = 0.

OTC = Detected Over Temperature Charge Current when set to 1.

OTD = Detected Over Temperature Discharge Current when set to 1.

BATHI= Detected Battery High Condition when set to 1.

BATLO = Detected Battery Low Condition when set to 1.

RSVD = Reserved. Default = 0.

SOC1 = Detected State-of-Charge-Threshold 1 (SOC1 Set) reached.

OCC = Detected Over Current Charge Condition when set to 1.

OCD= Detected Over Current DISCHARGE Condition when set to 1.

### **Reserved – 0x6e – 0x7f**

## DATA FLASH INTERFACE

### ACCESSING THE DATA FLASH

The bq28z560 data flash is a non-volatile memory that contains initialization, default, cell status, calibration, configuration, and user information. The data flash can be accessed in several different ways, depending on what mode the bq28z560 is operating in and what data is being accessed.

Commonly accessed data flash memory locations, frequently read by a system, are conveniently accessed through specific instructions, as described in [DATA COMMANDS](#). These commands are available when the bq28z560 is either in UNSEALED or SEALED modes.

Most data flash locations, however, are only accessible in UNSEALED mode by use of the bq28z560 evaluation software or by data flash block transfers. These locations should be optimized and/or fixed during the development and manufacture processes. They become part of a golden image file and can then be written to multiple battery packs. Once established, the values generally remain unchanged during end-equipment operation.

To access data flash locations individually, the block containing the desired data flash location(s) must be transferred to the command register locations where they can be read to the system or changed directly. This is accomplished by sending the set-up command *BlockDataControl()* (0x61) with data 0x00. Up to 32 bytes of data can be read directly from the *BlockData()* (0x40...0x5f), externally altered, then rewritten to the *BlockData()* command space. Alternatively, specific locations can be read, altered, and rewritten if their corresponding offsets are used to index into the *BlockData()* command space. Finally, the data residing in the command space is transferred to data flash, once the correct checksum for the whole block is written to *BlockDataChecksum()* (0x60).

Occasionally, a data flash CLASS will be larger than the 32-byte block size. In this case, the *DataFlashBlock()* command is used to designate which 32-byte block the desired locations reside. The correct command address is then given by  $0x40 + \text{offset} \text{ modulo } 32$ . For example, to access **Terminate Voltage** in the *Gas Gauging* class, *DataFlashClass()* is issued 80 (0x50) to set the class. Because the offset is 67, it must reside in the third 32-byte block. Hence, *DataFlashBlock()* is issued 0x02 to set the block offset, and the offset used to index into the *BlockData()* memory area is  $0x40 + 67 \text{ modulo } 32 = 0x40 + 16 = 0x40 + 0x03 = 0x43$ .

Reading and writing subclass data are block operations up to 32 bytes in length. If the data length exceeds the maximum block size during a write, then the data is ignored.

---

#### NOTE

None of the data written to memory are bounded by the bq28z560: The values are not rejected by the gas gauge. Writing an incorrect value may result in hardware failure due to firmware program interpretation of the invalid data. The written data is persistent, so a power-on reset does not resolve the fault.

---



## FUNCTIONAL DESCRIPTION

### FUEL GAUGING

The bq28z560 measures the cell voltage, temperature, and current to determine the battery SOC based on the Impedance Track algorithm (refer to the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* Application Report [SLUA450] for more information). The bq28z560 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in series with the cell. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge.

The total battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When an application load is applied, the impedance of the cell is measured by comparing the OCV obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and chemical capacity (Qmax). The initial Qmax values are taken from a cell manufacturers' data sheet multiplied by the number of parallel cells. It is also used for the value in **Design Capacity**. The bq28z560 acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the Qmax value, to determine *FullChargeCapacity()* and *StateOfCharge()*, specifically for the present load and temperature. *FullChargeCapacity()* is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage()* reaches **Terminate Voltage**. *NominalAvailableCapacity()* and *FullAvailableCapacity()* are the uncompensated (no or light load) versions of *RemainingCapacity()* and *FullChargeCapacity()*, respectively.

The bq28z560 has two flags accessed by the *Flags()* function that warn when the battery's SOC has fallen to critical levels. When *RemainingCapacity()* falls below the first capacity threshold specified in **SOC1 Set Threshold**, the [SOC1] (*State of Charge Initial*) flag is set. The flag is cleared once *RemainingCapacity()* rises above **SOC1 Clear Threshold**. All units are in mAh.

When *RemainingCapacity()* falls below the second capacity threshold (**SOCF Set Threshold**), the [SOCF] (*State of Charge Final*) flag is set, serving as a final discharge warning. If **SOCF Set Threshold** = -1, the flag is inoperative during discharge. Similarly, when *RemainingCapacity()* rises above **SOCF Clear Threshold** and the [SOCF] flag has already been set, the [SOCF] flag is cleared. All units are in mAh.

The bq28z560 has two additional flags accessed by the *Flags()* function that warns of internal battery conditions. The gas gauge monitors the cell voltage during relaxed conditions to determine if an internal short has been detected. When this condition occurs, [ISD] will be set. The bq28z560 also has the capability to detect when a tab is disconnected in a 2-cell parallel system by actively monitoring the SOH. When this conditions occurs, [TDD] will be set.

### IMPEDANCE TRACK VARIABLES

The bq28z560 has several data flash variables that permit the user to customize the Impedance Track algorithm for optimized performance. These variables are dependent upon the power characteristics of the application as well as the cell itself.

#### Load Mode

*Load Mode* is used to select either the *Constant-Current Mode* or *Constant-Power Mode* for the Impedance Track algorithm as used in **Load Select** (see **Load Select**). When **Load Mode** is 0, the *Constant-Current Mode* is used (default). When **Load Mode** is 1, the *Constant-Power Mode* is used. The [LDMD] bit of CONTROL\_STATUS reflects the status of **Load Mode**.

#### Load Select

**Load Select** defines the type of power or current mode to be used to compute load-compensated capacity in the Impedance Track algorithm. If **Load Mode** = 0 (*Constant Current*), then the options presented in [Table 11](#) are available.

**Table 11. Constant-Current Mode Used when Load Mode = 0**

| LoadSelect Value | Current Mode Used   |
|------------------|---|
| 0                | Average discharge current from previous cycle. There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register. |
| 1 (default)      | Present average discharge current. This is the average discharge current from the beginning of this discharge cycle until present time.   |
| 2                | Average current: based off the <i>AverageCurrent()</i>  |
| 3                | Current: based off of a low-pass-filtered version of <i>AverageCurrent()</i> ( $\tau = 14$ s)   |
| 4                | Design capacity / 5: C Rate based off of Design Capacity /5 or a C / 5 rate in mA.  |
| 5                | Use the value specified by <i>AtRate()</i>  |
| 6                | Use the value in <i>User_Rate-mA</i> . This gives a completely user-configurable method.  |

If **Load Mode = 1** (*Constant Power*), then the following options are available:

**Table 12. Constant-Power Mode Used When Load Mode = 1**

| LoadSelect Value | Power Mode Used   |
|------------------|---|
| 0 (default)      | Average discharge power from previous cycle. There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register. |
| 1                | Present average discharge power. This is the average discharge power from the beginning of this discharge cycle until present time.   |
| 2                | Average current x voltage: based off the <i>AverageCurrent()</i> and <i>Voltage()</i> .   |
| 3                | Current x voltage: based off of a low-pass-filtered version of <i>AverageCurrent()</i> ( $\tau = 14$ s) and <i>Voltage()</i>  |
| 4                | Design energy / 5: C Rate based off of Design Energy /5 or a C / 5 rate in mA.  |
| 5                | Use the value specified by <i>AtRate()</i>  |
| 6                | Use the value in <i>User_Rate-mW/cW</i> . This gives a completely user- configurable method.  |

### Reserve Cap-mAh

**Reserve Cap-mAh** determines how much actual remaining capacity exists after reaching 0 *RemainingCapacity()*, before **Terminate Voltage** is reached. A loaded rate or no-load rate of compensation can be selected for *Reserve Cap* by setting the [RESCAP] bit in the Pack Configuration register.

### Reserve Cap-mWh/cWh

**Reserve Cap-mWh** determines how much actual remaining capacity exists after reaching 0 *AvailableEnergy()*, before **Terminate Voltage** is reached. A loaded rate or no-load rate of compensation can be selected for *Reserve Cap* by setting the [RESCAP] bit in the Pack Configuration register.

### Design Energy Scale

**Design Energy Scale** is used to select the scale/unit of a set of data flash parameters. The value of **Design Energy Scale** can be either 1 or 10 only.

**Table 13. Data Flash Parameter Scale/Unit-Based on Design Energy Scale**

| Data Flash                       | Design Energy Scale = 1 (default) | Design Energy Scale = 10 |
|----------------------------------|-----------------------------------|--------------------------|
| <i>Design Energy</i>             | mWh                               | cWh                      |
| <i>Reserve Capacity -mWh/cWh</i> | mWh                               | cWh                      |
| <i>Avg Power Last Run</i>        | mW                                | cW                       |
| <i>User Rate-mW/cW</i>           | mWh                               | cWh                      |
| <i>T Rise</i>                    | No Scale                          | Scaled by x10            |

### Dsg Current Threshold

This register is used as a threshold by many functions in the bq28z560 to determine if actual discharge current is flowing into or out of the cell. The default for this register should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

## Chg Current Threshold

This register is used as a threshold by many functions in the bq28z560 to determine if actual charge current is flowing into or out of the cell. The default for this register should be sufficient for most applications. This threshold should be set low enough to be below any normal charge current but high enough to prevent noise or drift from affecting the measurement.

## Quit Current, Dsg Relax Time, Chg Relax Time, and Quit Relax Time

The **Quit Current** is used as part of the Impedance Track algorithm to determine when the bq28z560 enters RELAX mode from a current flowing mode in either the charge direction or the discharge direction. The value of Quit Current is set to a default value that should be above the standby current of the system.

Either of the following criteria must be met to enter RELAX mode:

1.  $|AverageCurrent()| < |Quit\ Current|$  for **Dsg Relax Time**.
2.  $|AverageCurrent()| < |Quit\ Current|$  for **Chg Relax Time**.

After about 6 minutes in RELAX mode, the bq28z560 attempts to take accurate OCV readings. An additional requirement of  $dV/dt < 4\ \mu V/sec$  is required for the bq28z560 to perform Qmax updates. These updates are used in the Impedance Track algorithms. It is critical that the battery voltage be relaxed during OCV readings and that the current is not higher than C/20 when attempting to go into RELAX mode.

**Quit Relax Time** specifies the minimum time required for *AverageCurrent()* to remain above the **QuitCurrent** threshold before exiting RELAX mode.

## Qmax

**Qmax** contains the maximum chemical capacity of the active cell profiles, and is determined by comparing states of charge before and after applying the load with the amount of charge passed. They also correspond to capacity at a low rate of discharge, such as C/20 rate. For high accuracy, this value is periodically updated by the bq28z560 during operation. Based on the battery cell capacity information, the initial value of chemical capacity should be entered in the **Qmax** field. The Impedance Track algorithm updates this value and maintains it in the **Pack** profile.

## Update Status

The Update Status register indicates the status of the Impedance Track algorithm.

**Table 14. Update Status Definitions**

| UPDATE STATUS | STATUS  |
|---------------|---|
| 0x02          | Qmax and Ra data are learned, but Impedance Track is not enabled. This should be the standard setting for a golden image.                           |
| 0x04          | Impedance Track is enabled but Qmax and Ra data are not learned.  |
| 0x05          | Impedance Track is enabled and only Qmax has been updated during a learning cycle.  |
| 0x06          | Impedance Track is enabled. Qmax and Ra data are learned after a successful learning cycle. This should be the operation setting for end equipment. |

This register should only be updated by the bq28z560 during a learning cycle or when *IT\_ENABLE()* subcommand is received. Refer to the application note *How to Generate Golden Image for a Single-Cell Impedance Track™ Device* ([SLUA544](#)) for learning cycle details.

## Avg I Last Run

The bq28z560 logs the current averaged from the beginning to the end of each discharge cycle. It stores this average current from the previous discharge cycle in this register. This register should never need to be modified. It is only updated by the bq28z560 when required.

## Avg P Last Run

The bq28z560 logs the power averaged from the beginning to the end of each discharge cycle. It stores this average power from the previous discharge cycle in this register. To get a correct average power reading, the bq28z560 continuously multiplies instantaneous current times *Voltage()* to get power. It then logs this data to derive the average power. This register should never need to be modified. It is only updated by the bq28z560 when required.

## Delta Voltage

The bq28z560 stores the maximum difference of *Voltage()* during short load spikes and normal load, so the Impedance Track algorithm can calculate remaining capacity for pulsed loads.

---

### NOTE

It is not recommended to change this value.

---

## Ra Tables and Ra Filtering Related Parameters

These tables contain encoded data and are automatically updated during device operation. The bq28z560 has a filtering process to eliminate unexpected fluctuations in Ra values while the Ra values are being updated. The DF parameters RaFilter, RaMaxDelta, MaxResfactor, and MinResfactor control the Filtering process of Ra values. RaMaxDelta Limits the change in Ra values to an absolute magnitude. MinResFactor and MaxResfactor parameters are cumulative filters which limit the change in Ra values to a scale on a per discharge cycle basis. These values are data flash configurable. No further user changes should be made to Ra values except for reading/writing the values from a pre-learned pack (part of the process for creating golden image files).

## MaxScaleBackGrid

The MaxScaleBackGrid parameter limits the resistance grid point after which back scaling will not be performed. This variable ensures that the resistance values in the lower resistance grid points remain accurate while the battery is at a higher DoD state.

## Max DeltaV, Min DeltaV

This is the Maximal/Minimal value allowed for delta V, which will be subtracted from simulated voltage during remaining capacity simulation.

## Qmax Max Delta %

This is the maximal change of Qmax during one update, as a percentage of Design Capacity. If the gauge attempts to change the Qmax value and this delta change value exceeds the Qmax Max delta % limit, the change value will be capped to the old value  $\pm$  DesignCapacity\*QmaxMaxDelta/100.

## Fast Resistance Scaling

This new algorithm improves convergency of Remaining Capacity and terminates voltage at end of discharge. The algorithm is enabled when cell voltage goes below (Terminate Voltage + Term V Delta) or *StateofCharge()* goes below Fast Scale Start SOC. For most applications, the default value of Term V Delta and Fast Scale Start SOC are recommended.

## Fast Qmax Update

This new algorithm improvement provides a fast Qmax update feature that can compute Qmax based on full charge and end of discharge conditions without battery relaxation. The feature can be enabled by setting the [FASTQMAX] bit in **Pack Configuration C**. Several data flash parameters (**Fast Qmax Start DOD%**, **Fast Qmax End DOD%**, and **Fast Qmax Start Voltage Delta**) are used to configure the algorithm, and default settings are recommended. Please note that the Fast Qmax Update algorithm is not used during learning cycle.

## DeltaV Max Delta

This is the maximal change of the Delta V value. If an attempted change of the value exceeds this limit, the change value will be capped to old value  $\pm$ DeltaV Max Delta.

## Lifetime Data Logging Parameters

### NOTE

IT\_ENABLE must be enabled (Command 0x0021) for Lifetime Data logging functions to be active.

The Lifetime Data logging function helps development and diagnosis with the bq28z560. The bq28z560 device logs the Lifetime Data as specified in the **Lifetime Data** and **Lifetime Temp Samples** data flash subclasses. The data log recordings are controlled by the **Lifetime Resolution** data flash subclass.

The Lifetime Data Logging can be started by setting the IT\_ENABLE bit and setting the Update Time register to a non-zero value.

Once the Lifetime Data Logging function is enabled, the measured values are compared to what is already stored in the data flash. If the measured value is higher than the maximum or lower than the minimum value stored in the data flash by more than the "Resolution" set for at least one parameter, the entire data flash Lifetime registers are updated after at least LTUpdateTime.

LTUpdateTime sets the minimum update time between DF writes. When a new max/min is detected, an LT Update window of [update time] second is enabled and the DF writes occur at the end of this window. Any additional max/min value detected within this window will also be updated. The first new max/min value detected after this window will trigger the next LT Update window.

Internal to bq28z560, there exists a RAM max/min table in addition to the DF max/min table. The RAM table is updated independent of the resolution parameters. The DF table is updated only if at least one of the RAM parameters exceeds the DF value by more than the resolution associated with it. When DF is updated, the entire RAM table is written to DF. Consequently, it is possible to see a new max/min value for a certain parameter even if the value of this parameter never exceeds the maximum or minimum value stored in the data flash for this parameter value by the resolution amount.

The Lifetime Data Logging of one or more parameters can be reset or restarted by writing new default (or starting) values to the corresponding data flash registers through sealed or unsealed access as described below. However, when using unsealed access, new values will only take effect after device reset.

The logged data can be accessed as R/W in UNSEALED mode from the Lifetime Data SubClass (SubClass ID=59) of data flash. Lifetime Data may be accessed (R/W) when sealed using a process identical in Manufacturer Info Block B and C. The DataFlashBlock command code is 4. Note that only the first 32 bytes of Lifetime Data (not resolution parameters) can be R/W when sealed. See [MANUFACTURER INFORMATION BLOCKS](#) for sealed access. The logging settings such as Temperature Resolution, Voltage Resolution, Current Resolution, and Update Time can be configured only in UNSEALED mode by writing to the Lifetime Resolution subclass (SubClassID=66) of the data flash.

The Lifetime resolution registers contain the parameters that set the limits related to how much a data parameter must exceed the previously logged Max/Min value to be updated in the lifetime log. For example, V must exceed MaxV by more than Voltage Resolution to update MaxV in the data flash.

## DETAILED CONFIGURATION REGISTER DESCRIPTIONS

### The Pack Configuration Register

Some bq28z560 pins are configured via the **Pack Configuration** data flash register, as indicated in [Table 15](#). This register is programmed/read via the methods described in [ACCESSING THE DATA FLASH](#). The register is located at subclass = 64, offset = 0.

**Table 15. Pack Configuration Bit Definition**

|           | Bit 7  | Bit 6       | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1 | Bit 0 |
|-----------|--------|-------------|-------|-------|----------|----------|-------|-------|
| High Byte | RESCAP | CalEn       | RSVD  | RSVD  | RSVD     | IWAKE    | RSNS1 | RSNS0 |
| Low Byte  | GNDSEL | RESFACTSTEP | SLEEP | RMFCC | CLR_READ | ALRT_POL | RSVD  | TEMPS |

RESCAP = No-load rate of compensation is applied to the reserve capacity calculation. True when set. Default is 0.

CalEn = bq28z560 Calibration mode is enabled. Default is 0.

RSVD = Reserved. Default = 0

RSVD = Reserved. Default = 0.

RSVD = Reserved. Default = 0.

GNDSEL = The ADC ground select control. The  $V_{SS}$  (Pin 6) is selected as ground reference when the bit is clear. Pin 7 is selected when the bit is set. Default is 0.

IWAKE/RSNS1/RSNS0 = These bits configure the current wake function. Default is 0/0/1.

GNDSEL = The ADC ground select control. The  $V_{SS}$  (Pin 6) is selected as ground reference when the bit is clear. Pin 7 is selected when the bit is set. Default is 0.

ResFactStep = Enables Ra step up/down to Max/Min Res Factor before disabling Ra updates. Default is 1.

SLEEP = The gas gauge can enter sleep, if operating conditions allow. True when set. Default is 1.

RMFCC = RM is updated with the value from FCC, on valid charge termination. True when set. Default is 1.

CLR\_READ = Clear on Read the Fault Flag register. True when set. Default = 0

ALRT\_POL = Set polarity of Alert output. Set to 1 means active high, so any faults detected will change output from low to high. Default = 0, which means any fault detected will change output from high to low.

RSVD = Reserved. Default = 0

TEMPS = Selects external thermistor for *Temperature()* measurements. True when set. Default is 1.

### Pack Configuration B Register

Some bq28z560 pins are configured via the **Pack Configuration B** data flash register, as indicated in [Table 16](#). This register is programmed/read via the methods described in [ACCESSING THE DATA FLASH](#). The register is located at subclass = 64, offset = 2.

**Table 16. Pack Configuration B Bit Definition**

| Bit 7     | Bit 6  | Bit 5   | Bit 4  | Bit 3 | Bit 2    | Bit 1 | Bit 0   |
|-----------|--------|---------|--------|-------|----------|-------|---------|
| ChgDoDEoC | SE_TDD | VconsEN | SE_ISD | JEITA | LFPRelax | DoDWT | FConvEn |

ChgDoDEoC = Enable DoD at EoC during charging only. True when set. Default is 1. Default setting is recommended.

SE\_TDD = Enable Tab Disconnection Detection. True when set. Default is 1.

VconsEN = Enable voltage consistency check. True when set. Default is 1. Default setting is recommended.

SE\_ISD = Enable Internal Short Detection. True when set. Default is 1.

JEITA = Enable JEITA Temperature Charging function. True when set. Default is 1.

LFPRelax = Enable LiFePO4 long RELAX mode when chemical ID 400 series is selected. True when set. Default is 1.

DoDWT = Enable Dod weighting for LiFePO4 support when chemical ID 400 series is selected. True when set. Default is 1.

FConvEn = Enable fast convergence algorithm. Default is 1. Default setting is recommended.

### Pack Configuration C Register

Some bq28z560 algorithm settings are configured via the **Pack Configuration C** data flash register, as indicated in [Table 17](#). This register is programmed/read via the methods described in [ACCESSING THE DATA FLASH](#). The register is located at subclass = 64, offset = 3.

**Table 17. Pack Configuration C Bit Definition**

| Bit 7    | Bit 6   | Bit 5   | Bit 4   | Bit 3        | Bit 2 | Bit 1     | Bit 0     |
|----------|---------|---------|---------|--------------|-------|-----------|-----------|
| FastQmax | RSVDSBS | PIN12F1 | PIN12F0 | SleepWakeChg | RSVD  | CFET_INIT | DFET_INIT |

FastQmax = Enable Fast Qmax Update mode. True when set. Default is 0. Default setting is recommended.

RSVDSBS = Reserved for SBS command set. True when set. Default is 0.

PIN12F1 = In combination with PIN12F0 will set the operation mode of pin 12 (see below)

PIN12F0 = In combination with PIN12F1 will set the operation mode of pin 12 (see below)

SleepWakeChg = if set to 1 will accumulate the charge as if it was active for 10 s ( instead of 20 s)



RSVD = Reserved. Default = 0

CFET\_INIT= Sets initial state of CHG FET at reset condition. 0 = CHG FET OFF, 1 = CHG FET ON

DFET\_INIT= Sets initial state of DSG FET at reset condition. 0 = DSG FET OFF, 1 = DSG FET ON

| PIN12F1 | PIN12F0 | State               |
|---------|---------|---------------------|
| 0       | 0       | NC or HDQ (default) |
| 0       | 1       | CHG FET             |
| 1       | 0       | Bat Alert           |
| 1       | 1       | RSVD                |

### Battery Alert Default Configuration Register

When the system is configured as an interrupt indication, the bq28z560 allows settings to be configured based on which faults are OR'ed for indication on the Alert output [Table 18](#). This register is programmed/read via the methods described in [ACCESSING THE DATA FLASH](#). The register is located at subclass = 64, offset = 4.

**Table 18. Battery Alert Default Configuration Bit Definition**

| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|--------|--------|--------|--------|--------|--------|-------|-------|
| UTC_EN | UTD_EN | RSVD   | RSVD   | RSVD   | RSVD   | RSVD  | RSVD  |

| Bit 7  | Bit 6  | Bit 5 | Bit 4 | Bit 3 | Bit 2   | Bit 1  | Bit 0  |
|--------|--------|-------|-------|-------|---------|--------|--------|
| OTC_EN | OTD_EN | BH_EN | BL_EN | RSVD  | SOC1_EN | OCC_EN | OCD_EN |

UTC\_EN = Allows detection of Under Temperature Charging when set to 1. Default is 0.

UTD\_EM = Allows detection of Under Temperature Discharging when set to 1. Default is 0.

RSVD = Reserved. Default = 0.

OTC\_EN = Allows detection of Over Temperature Charging when set to 1. Default is 0.

OTD\_EN = Allows detection of Over Temperature Discharging when set to 1. Default is 0.

BH\_EN = Allows detection of Battery High when set to 1. Default is 0.

BL\_EN = Allows detection of Battery Low when set to 1. Default is 0.

RSVD = Reserved. Default = 0.

SOC1\_EN Allows detection of SOC low when set to 1. Default is 0.

OCC\_EN = Allows detection of Over Current in Charge mode when set to 1. Default is 0.

OCD\_EN = Allows detection of Over Current in Discharge mode when set to 1. Default is 0.

Important: The enable flags (Bits 7 to 4) are the reset values. Changing the data flash will *not* take effect until the gas gauge is re-started. Read/Write of the BatAlert\_Configuration I<sup>2</sup>C data controls the runtime alert mask.

### MANUFACTURER INFORMATION BLOCKS

The bq28z560 contains 64 bytes of user programmable data flash storage: **Manufacturer Info Block A** and **Manufacturer Info Block B**. The method for accessing these memory locations is slightly different, depending on whether the device is in UNSEALED or SEALED modes.

When in UNSEALED mode and when 0x00 has been written to *BlockDataControl()*, accessing the Manufacturer Info Blocks is identical to accessing general data flash locations. First, a *DataFlashClass()* command is used to set the subclass, then a *DataFlashBlock()* command sets the offset for the first data flash address within the subclass. The *BlockData()* command codes contain the referenced data flash data. When writing the data flash, a checksum is expected to be received by *BlockDataChecksum()*. Only when the checksum is received and verified is the data actually written to data flash.

As an example, the data flash location for **Manufacturer Info Block B** is defined as having a Subclass = 58 and an Offset = 32 through 63 (32 byte block). The specification of Class = System Data is not needed to address **Manufacturer Info Block B**, but is used instead for grouping purposes when viewing data flash info in the bq28z560 evaluation software.

When in SEALED mode or when 0x01 *BlockDataControl()* does not contain 0x00, data flash is no longer available in the manner used in UNSEALED mode. Rather than issuing subclass information, a designated Manufacturer Information Block is selected with the *DataFlashBlock()* command. Issuing a 0x01, 0x02, or 0x03 with this command causes the corresponding information block (A, B, or C, respectively) to be transferred to the command space 0x40...0x5f for editing or reading by the system. Upon successful writing of checksum information to *BlockDataChecksum()*, the modified block is returned to data flash.

---

**NOTE**

**Manufacturer Info Block A** is read-only when in SEALED mode.

---

## ACCESS MODES

The bq28z560 provides three security modes (FULL ACCESS, UNSEALED, and SEALED) that control data flash access permissions according to [Table 19](#). *Data flash* refers to those data flash locations specified in [Table 20](#), that are accessible to the user. *Manufacturer Information* refers to the three 32-byte blocks.

**Table 19. Data Flash Access**

| SECURITY MODE | DATA FLASH | MANUFACTURER INFORMATION |
|---------------|------------|--------------------------|
| FULL ACCESS   | R/W        | R/W                      |
| UNSEALED      | R/W        | R/W                      |
| SEALED        | None       | R (A); R/W (B,C)         |

Although FULL ACCESS and UNSEALED modes appear identical, only FULL ACCESS mode allows the bq28z560 to write access-mode transition keys.

## SEALING/UNSEALING DATA FLASH

The bq28z560 implements a key-access scheme to transition between SEALED, UNSEALED, and FULL-ACCESS modes. Each transition requires that a unique set of two keys be sent to the bq28z560 via the *Control()* control command. The keys must be sent consecutively, with no other data being written to the *Control()* register in between. Note that to avoid conflict, the keys must be different from the codes presented in the *CNTL DATA* column of [Table 4](#) subcommands.

When in SEALED mode the *[SS]* bit of *CONTROL\_STATUS* is set, but when the UNSEAL keys are correctly received by the bq28z560, the *[SS]* bit is cleared. When the full-access keys are correctly received the *CONTROL\_STATUS [FAS]* bit is cleared.

Both **Unseal Key** and **Full-Access Key** have two words and are stored in data flash. The first word is Key 0 and the second word is Key 1. The order of the keys sent to bq28z560 are Key 1 followed by Key 0. The order of the bytes for each key entered through the *Control()* command is the reverse of what is read from the part. For an example, if the Unseal Key is 0x56781234, key 1 is 0x1234 and key 0 is 0x5678. Then *Control()* should supply 0x3412 and 0x7856 to unseal the part. The **Unseal Key** and the **Full-Access Key** can only be updated when in FULL-ACCESS mode.



## DATA FLASH SUMMARY

Table 20 provides a summary of data flash locations available to the user, including their default, minimum, and maximum values.

**Table 20. Data Flash Summary**

| Class         | Subclass ID | Subclass           | Offset | Name                  | Data Type | Min Value | Max Value | Default Value | Units (EVSW Units)* |
|---------------|-------------|--------------------|--------|-----------------------|-----------|-----------|-----------|---------------|---------------------|
| Configuration | 1           | Safety Current     | 0      | OC Chg                | I2        | 0         | 20000     | 6000          | mA                  |
| Configuration | 1           | Safety Current     | 2      | OC Chg Time           | U1        | 0         | 60        | 2             | s                   |
| Configuration | 1           | Safety Current     | 3      | OC Chg Recovery       | I2        | 0         | 20000     | 200           | mA                  |
| Configuration | 1           | Safety Current     | 5      | OC Dsg                | I2        | -20000    | 0         | -6000         | mA                  |
| Configuration | 1           | Safety Current     | 7      | OC Dsg Time           | U1        | 0         | 60        | 2             | s                   |
| Configuration | 1           | Safety Current     | 8      | OC Dsg Recovery       | I2        | -20000    | 0         | -200          | mA                  |
| Configuration | 1           | Safety Current     | 9      | Current Recovery Time | U1        | 0         | 255       | 8             | s                   |
| Configuration | 2           | Safety Temperature | 0      | OT Chg                | I2        | 0         | 1200      | 550           | 0.1°C               |
| Configuration | 2           | Safety Temperature | 2      | OT Chg Time           | U1        | 0         | 60        | 2             | s                   |
| Configuration | 2           | Safety Temperature | 3      | OT Chg Recovery       | I2        | 0         | 1200      | 500           | 0.1°C               |
| Configuration | 2           | Safety Temperature | 5      | OT Dsg                | I2        | 0         | 1200      | 600           | 0.1°C               |
| Configuration | 2           | Safety Temperature | 7      | OT Dsg Time           | U1        | 0         | 60        | 2             | s                   |
| Configuration | 2           | Safety Temperature | 8      | OT Dsg Recovery       | I2        | 0         | 1200      | 550           | 0.1°C               |
| Configuration | 2           | Safety Temperature | 10     | UT Chg                | I2        | -400      | 1200      | 0             | 0.1°C               |
| Configuration | 2           | Safety Temperature | 12     | UT Chg Time           | U1        | 0         | 60        | 2             | s                   |
| Configuration | 2           | Safety Temperature | 13     | UT Chg Recovery       | I2        | -400      | 1200      | 50            | 0.1°C               |
| Configuration | 2           | Safety Temperature | 15     | UT Dsg                | I2        | -400      | 1200      | 0             | 0.1°C               |
| Configuration | 2           | Safety Temperature | 17     | UT Dsg Time           | U1        | 0         | 60        | 2             | s                   |
| Configuration | 2           | Safety Temperature | 18     | UT Dsg Recovery       | I2        | -400      | 1200      | 50            | 0.1°C               |
| Configuration | 32          | Charge Inhibit Cfg | 0      | Chg Inhibit Temp Low  | I2        | -400      | 1200      | 0             | 0.1°C               |
| Configuration | 32          | Charge Inhibit Cfg | 2      | Chg Inhibit Temp High | I2        | -400      | 1200      | 450           | 0.1°C               |
| Configuration | 32          | Charge Inhibit Cfg | 4      | Temp Hys              | I2        | 0         | 100       | 50            | 0.1°C               |
| Configuration | 33          | Pre-Charge         | 0      | Pre-Charge Voltage    | I2        | 0         | 4600      | 3000          | mV                  |
| Configuration | 33          | Pre-Charge         | 2      | Pre-Charge Current    | I2        | 0         | 32767     | 150           | mA                  |
| Configuration | 36          | Charge Termination | 0      | Taper Current         | I2        | 0         | 1000      | 100           | mA                  |
| Configuration | 36          | Charge Termination | 2      | Min Taper Capacity    | I2        | 0         | 1000      | 25            | mAh                 |
| Configuration | 36          | Charge Termination | 4      | Taper Voltage         | I2        | 0         | 1000      | 100           | mV                  |
| Configuration | 36          | Charge Termination | 6      | Current Taper Window  | U1        | 0         | 60        | 40            | s                   |
| Configuration | 36          | Charge Termination | 7      | TCA Set %             | I1        | -1        | 100       | 99            | %                   |
| Configuration | 36          | Charge Termination | 8      | TCA Clear %           | I1        | -1        | 100       | 95            | %                   |
| Configuration | 36          | Charge Termination | 9      | FC Set %              | I1        | -1        | 100       | 100           | %                   |
| Configuration | 36          | Charge Termination | 10     | FC Clear %            | I1        | -1        | 100       | 98            | %                   |
| Configuration | 36          | Charge Termination | 11     | DODatEOC Delta T      | I2        | 0         | 1000      | 100           | 0.1°C               |
| Configuration | 48          | Data               | 0      | Rem Cap Alarm         | I2        | 0         | 700       | 100           | mA                  |
| Configuration | 48          | Data               | 8      | Initial Standby       | I1        | -256      | 0         | -10           | mA                  |
| Configuration | 48          | Data               | 9      | Initial MaxLoad       | I2        | -32767    | 0         | -500          | mA                  |
| Configuration | 48          | Data               | 17     | Cycle Count           | U2        | 0         | 65535     | 0             | num                 |
| Configuration | 48          | Data               | 19     | CC Threshold          | I2        | 100       | 32767     | 900           | mAh                 |
| Configuration | 48          | Data               | 23     | Design Capacity       | I2        | 0         | 32767     | 1000          | mA                  |
| Configuration | 48          | Data               | 25     | Design Energy         | I2        | 0         | 32767     | 5400          | mWh/cWh             |
| Configuration | 48          | Data               | 27     | SOH Load I            | I2        | -32767    | 0         | -400          | mA                  |
| Configuration | 48          | Data               | 29     | TDD SOH Percent       | I1        | 0         | 100       | 90            | %                   |
| Configuration | 48          | Data               | 30     | TA CV T1-T2           | U1        | 0         | 225       | 120           | 10 mV               |
| Configuration | 48          | Data               | 31     | TA CV T2-T3           | U1        | 0         | 225       | 120           | 10 mV               |
| Configuration | 48          | Data               | 32     | TA CV T3-T4           | U1        | 0         | 225       | 110           | 10 mV               |
| Configuration | 48          | Data               | 33     | TA CC T1-T2           | U1        | 0         | 100       | 10            | %                   |
| Configuration | 48          | Data               | 34     | TA CC T2-T3           | U1        | 0         | 100       | 50            | %                   |
| Configuration | 48          | Data               | 35     | TA CC T3-T4           | U1        | 0         | 100       | 30            | %                   |
| Configuration | 48          | Data               | 36     | JEITA T1              | I1        | -128      | 127       | 0             | °C                  |
| Configuration | 48          | Data               | 37     | JEITA T2              | I1        | -128      | 127       | 10            | °C                  |

**Table 20. Data Flash Summary (continued)**

| Class         | Subclass ID | Subclass              | Offset | Name                       | Data Type | Min Value | Max Value | Default Value | Units (EVSW Units)* |
|---------------|-------------|-----------------------|--------|----------------------------|-----------|-----------|-----------|---------------|---------------------|
| Configuration | 48          | Data                  | 38     | JEITA T3                   | I1        | -128      | 127       | 45            | °C                  |
| Configuration | 48          | Data                  | 39     | JEITA T4                   | I1        | -128      | 127       | 55            | °C                  |
| Configuration | 48          | Data                  | 40     | ISD Current                | I2        | 0         | 32767     | 10            | HourRate            |
| Configuration | 48          | Data                  | 42     | ISD I Filter               | U1        | 0         | 255       | 127           | num                 |
| Configuration | 48          | Data                  | 43     | Min ISD Time               | U1        | 0         | 255       | 7             | Hour                |
| Configuration | 48          | Data                  | 44     | Design Energy Scale        | U1        | 0         | 255       | 1             | num                 |
| Configuration | 48          | Data                  | 45     | Device Name                | S21       | x         | x         | bq28z560      | —                   |
| Configuration | 49          | Discharge             | 0      | SOC1 Set Threshold         | U2        | 0         | 65535     | 150           | mAh                 |
| Configuration | 49          | Discharge             | 2      | SOC1 Clear Threshold       | U2        | 0         | 65535     | 175           | mAh                 |
| Configuration | 49          | Discharge             | 4      | SOCF Set Threshold         | U2        | 0         | 65535     | 75            | mAh                 |
| Configuration | 49          | Discharge             | 6      | SOCF Clear Threshold       | U2        | 0         | 65535     | 100           | mAh                 |
| Configuration | 49          | Discharge             | 9      | BL Set Volt Threshold      | I2        | 0         | 16800     | 0             | mV                  |
| Configuration | 49          | Discharge             | 11     | BL Set Volt Time           | U1        | 0         | 60        | 0             | s                   |
| Configuration | 49          | Discharge             | 12     | BL Clear Volt Threshold    | I2        | 0000      | 16800     | 5             | mV                  |
| Configuration | 49          | Discharge             | 14     | BH Set Volt Threshold      | I2        | 0         | 16800     | 4300          | mV                  |
| Configuration | 49          | Discharge             | 16     | BH Volt Time               | U1        | 0         | 60        | 2             | s                   |
| Configuration | 49          | Discharge             | 17     | BH Clear Volt Threshold    | I2        | 0000      | 16800     | 5             | mV                  |
| Configuration | 56          | Manufacturer Data     | 0      | Pack Lot Code              | H2        | 0x0       | 0xffff    | 0x0           | —                   |
| Configuration | 56          | Manufacturer Data     | 2      | PCB Lot Code               | H2        | 0x0       | 0xffff    | 0x0           | —                   |
| Configuration | 56          | Manufacturer Data     | 4      | Firmware Version           | H2        | 0x0       | 0xffff    | 0x0           | —                   |
| Configuration | 56          | Manufacturer Data     | 6      | Hardware Revision          | H2        | 0x0       | 0xffff    | 0x0           | —                   |
| Configuration | 56          | Manufacturer Data     | 8      | Cell Revision              | H2        | 0x0       | 0xffff    | 0x0           | —                   |
| Configuration | 56          | Manufacturer Data     | 10     | DF Config Version          | H2        | 0x0       | 0xffff    | 0x0           | —                   |
| Configuration | 57          | Integrity Data        | 6      | Static Chem DF Checksum    | H2        | 0x0       | 0x7fff    | 0x0           | —                   |
| System Data   | 58          | Manufacturer Info     | 0–31   | Block A [0–31]             | H1        | 0x0       | ff        | 0             | —                   |
| System Data   | 58          | Manufacturer Info     | 32–63  | Block B [0–31]             | H1        | 0x0       | ff        | 0             | —                   |
| Configuration | 59          | Lifetime Data         | 0      | Lifetime Max Temp          | I2        | 0         | 1400      | 300           | 0.1°C               |
| Configuration | 59          | Lifetime Data         | 2      | Lifetime Min Temp          | I2        | -600      | 1400      | 200           | 0.1°C               |
| Configuration | 59          | Lifetime Data         | 4      | Lifetime Max Pack Voltage  | I2        | 0         | 32767     | 3200          | mV                  |
| Configuration | 59          | Lifetime Data         | 6      | Lifetime Min Pack Voltage  | I2        | 0         | 32767     | 3500          | mV                  |
| Configuration | 59          | Lifetime Data         | 8      | Lifetime Max Chg Current   | I2        | -32767    | 32767     | 0             | mA                  |
| Configuration | 59          | Lifetime Data         | 10     | Lifetime Max Dsg Current   | I2        | -32767    | 32767     | 0             | mA                  |
| Configuration | 60          | Lifetime Temp Samples | 0      | LT Flash Cnt               | U2        | 0         | 65535     | 0             | —                   |
| Configuration | 64          | Registers             | 0      | Pack Configuration         | H2        | 0x0       | 0xffff    | 0x0177        | —                   |
| Configuration | 64          | Registers             | 2      | Pack Configuration B       | H1        | 0x0       | 0xff      | 0x1f          | —                   |
| Configuration | 64          | Registers             | 3      | Pack Configuration C       | H1        | 0x0       | 0xff      | 0x0           | —                   |
| Configuration | 66          | Lifetime Resolution   | 0      | LT Temp Res                | U1        | 0         | 255       | 10            | Num                 |
| Configuration | 66          | Lifetime Resolution   | 1      | LT V Res                   | U1        | 0         | 255       | 25            | Num                 |
| Configuration | 66          | Lifetime Resolution   | 2      | LT Cur Res                 | U1        | 0         | 255       | 100           | Num                 |
| Configuration | 66          | Lifetime Resolution   | 3      | LT Update Time             | U2        | 0         | 65535     | 60            | Num                 |
| Configuration | 68          | Power                 | 0      | Flash Update OK Voltage    | I2        | 0         | 4200      | 2800          | mV                  |
| Configuration | 68          | Power                 | 2      | Sleep Current              | I2        | 0         | 100       | 10            | mA                  |
| Configuration | 68          | Power                 | 11     | Hibernate I                | U2        | 0         | 700       | 8             | mA                  |
| Configuration | 68          | Power                 | 13     | Hibernate V                | U2        | 2400      | 3000      | 2550          | mV                  |
| Configuration | 68          | Power                 | 15     | FS Wait                    | U1        | 0         | 255       | 0             | s                   |
| Gas Gauging   | 80          | IT Cfg                | 0      | Load Select                | U1        | 0         | 255       | 1             | —                   |
| Gas Gauging   | 80          | IT Cfg                | 1      | Load Mode                  | U1        | 0         | 255       | 0             | —                   |
| Gas Gauging   | 80          | IT Cfg                | 21     | Max Res Factor             | U1        | 0         | 255       | 15            | num                 |
| Gas Gauging   | 80          | IT Cfg                | 22     | Min Res Factor             | U1        | 0         | 255       | 3             | num                 |
| Gas Gauging   | 80          | IT Cfg                | 25     | Ra Filter                  | U2        | 0         | 1000      | 500           | num                 |
| Gas Gauging   | 80          | IT Cfg                | 42     | Fast Qmax Start DOD %      | U1        | 0         | 255       | 92            | %                   |
| Gas Gauging   | 80          | IT Cfg                | 43     | Fast Qmax End DOD %        | U1        | 0         | 255       | 96            | %                   |
| Gas Gauging   | 80          | IT Cfg                | 44     | Fast Qmax Start Volt Delta | I2        | 0         | 4200      | 200           | mV                  |
| Gas Gauging   | 80          | IT Cfg                | 67     | Terminate Voltage          | I2        | 2800      | 3700      | 3000          | mV                  |
| Gas Gauging   | 80          | IT Cfg                | 69     | Term V Delta               | I2        | 0         | 4200      | 200           | mV                  |

**Table 20. Data Flash Summary (continued)**

| Class       | Subclass ID | Subclass           | Offset | Name                     | Data Type | Min Value | Max Value   | Default Value | Units (EVSW Units)* |
|-------------|-------------|--------------------|--------|--------------------------|-----------|-----------|-------------|---------------|---------------------|
| Gas Gauging | 80          | IT Cfg             | 72     | ResRelax Time            | U2        | 0         | 65534       | 200           | s                   |
| Gas Gauging | 80          | IT Cfg             | 76     | User Rate-mA             | I2        | 2000      | 9000        | 0             | mA                  |
| Gas Gauging | 80          | IT Cfg             | 78     | User Rate-Pwr            | I2        | 3000      | 14000       | 0             | mW/cW               |
| Gas Gauging | 80          | IT Cfg             | 80     | Reserve Cap-mAh          | I2        | 0         | 9000        | 0             | mA                  |
| Gas Gauging | 80          | IT Cfg             | 82     | Reserve Energy           | I2        | 0         | 14000       | 0             | mWh/cWh             |
| Gas Gauging | 80          | IT Cfg             | 86     | Max Scale Back Grid      | U1        | 0         | 15          | 4             | —                   |
| Gas Gauging | 80          | IT Cfg             | 87     | Max DeltaV               | U2        | 0         | 65535       | 200           | mV                  |
| Gas Gauging | 80          | IT Cfg             | 89     | Min DeltaV               | U2        | 0         | 65535       | 0             | mV                  |
| Gas Gauging | 80          | IT Cfg             | 91     | Max Sim Rate             | U1        | 0         | 255         | 2             | C/rate              |
| Gas Gauging | 80          | IT Cfg             | 92     | Min Sim Rate             | U1        | 0         | 255         | 20            | C/rate              |
| Gas Gauging | 80          | IT Cfg             | 93     | Ra Max Delta             | U2        | 0         | 65535       | 44            | mΩ                  |
| Gas Gauging | 80          | IT Cfg             | 95     | Qmax Max Delta %         | U1        | 0         | 100         | 5             | mAh                 |
| Gas Gauging | 80          | IT Cfg             | 96     | DeltaV Max Delta         | U2        | 0         | 65535       | 10            | mV                  |
| Gas Gauging | 80          | IT Cfg             | 102    | Fast Scale Start SOC     | U1        | 0         | 100         | 10            | %                   |
| Gas Gauging | 80          | IT Cfg             | 103    | Charge Hys Voltage Shift | I2        | 0         | 2000        | 40            | mV                  |
| Gas Gauging | 81          | Current Thresholds | 0      | Dsg Current Threshold    | I2        | 0         | 2000        | 60            | mA                  |
| Gas Gauging | 81          | Current Thresholds | 2      | Chg Current Threshold    | I2        | 0         | 2000        | 75            | mA                  |
| Gas Gauging | 81          | Current Thresholds | 4      | Quit Current             | I2        | 0         | 1000        | 40            | mA                  |
| Gas Gauging | 81          | Current Thresholds | 6      | Dsg Relax Time           | U2        | 0         | 8191        | 60            | s                   |
| Gas Gauging | 81          | Current Thresholds | 8      | Chg Relax Time           | U1        | 0         | 255         | 60            | s                   |
| Gas Gauging | 81          | Current Thresholds | 9      | Quit Relax Time          | U1        | 0         | 63          | 1             | s                   |
| Gas Gauging | 81          | Current Thresholds | 10     | Max IR Correct           | U2        | 0         | 1000        | 400           | mV                  |
| Gas Gauging | 82          | State              | 0      | Qmax Cell 0              | I2        | 0         | 32767       | 1000          | mAh                 |
| Gas Gauging | 82          | State              | 2      | Cycle Count              | U2        | 0         | 65535       | 0             | num                 |
| Gas Gauging | 82          | State              | 4      | Update Status            | H1        | 0x0       | 0x6         | 0x0           | —                   |
| Gas Gauging | 82          | State              | 5      | V at Chg Term            | I2        | 0         | 5000        | 4200          | mV                  |
| Gas Gauging | 82          | State              | 7      | Avg I Last Run           | I2        | -32768    | 32767       | -299          | mA                  |
| Gas Gauging | 82          | State              | 9      | Avg P Last Run           | I2        | -32768    | 32767       | -1131         | mA                  |
| Gas Gauging | 82          | State              | 11     | Delta Voltage            | I2        | -32768    | 32767       | 2             | mV                  |
| Gas Gauging | 82          | State              | 15     | T Rise                   | I2        | 0         | 32767       | 0             | Num                 |
| Gas Gauging | 82          | State              | 17     | T Time Constant          | I2        | 0         | 32767       | 32767         | Num                 |
| OCV Table   | 83          | OCVa Table         | 0      | Chem ID                  | H2        | 0x0       | 0xffff      | 0x0107        | —                   |
| Ra Table    | 88          | R_a0               | 0      | Cell0 R_a flag           | H2        | 0x0       | 0x0         | 0xff55        | —                   |
| Ra Table    | 88          | R_a0               | 2-30   | Cell0 R_a 0-14           | I2        | 183       | 183         | 105           | 2 <sup>-10</sup> Ω  |
| Ra Table    | 89          | R_a0x              | 0      | xCell0 R_a flag          | H2        | 0xffff    | 0xffff      | 0xffff        | —                   |
| Ra Table    | 89          | R_a0x              | 2-30   | xCell0 R_a 0-14          | I2        | 183       | 183         | 105           | 2 <sup>-10</sup> Ω  |
| Calibration | 104         | Data               | 0      | CC Gain                  | F4        | 1.0e-1    | 4.0e+1      | 0.4768        | num                 |
| Calibration | 104         | Data               | 4      | CC Delta                 | F4        | 2.9826e+4 | 1.193046e+6 | 5677445.6     | num                 |
| Calibration | 104         | Data               | 8      | CC Offset                | I2        | -32768    | 32767       | -1200         | num                 |
| Calibration | 104         | Data               | 10     | Board Offset             | I1        | -128      | 127         | 0             | num                 |
| Calibration | 104         | Data               | 11     | Int Temp Offset          | I1        | -128      | 127         | 0             | num                 |
| Calibration | 104         | Data               | 12     | Ext Temp Offset          | I1        | -128      | 127         | 0             | num                 |
| Calibration | 104         | Data               | 13     | Pack V Offset            | I1        | -128      | 127         | 0             | mV                  |
| Calibration | 107         | Current            | 1      | Deadband                 | U1        | 0         | 255         | 5             | mA                  |
| Security    | 112         | Codes              | 0      | Sealed to Unsealed       | H4        | 0x0       | 0xffffffff  | 0x36720414    | —                   |
| Security    | 112         | Codes              | 4      | Unsealed to Full         | H4        | 0x0       | 0xffffffff  | 0xffffffff    | —                   |
| Security    | 112         | Codes              | 8      | Authen Key3              | H4        | 0x0       | 0xffffffff  | 0x01234567    | —                   |
| Security    | 112         | Codes              | 12     | Authen Key2              | H4        | 0x0       | 0xffffffff  | 0x89abcdef    | —                   |
| Security    | 112         | Codes              | 16     | Authen Key1              | H4        | 0x0       | 0xffffffff  | 0xfedcba98    | —                   |
| Security    | 112         | Codes              | 20     | Authen Key0              | H4        | 0x0       | 0xffffffff  | 0x76543210    | —                   |

## CHARGING AND CHARGE TERMINATION INDICATION

### Detection Charge Termination

For proper bq28z560 operation, the cell charging voltage must be specified by the user. The default value for this variable is in the data flash **Charging Voltage**.

The bq28z560 detects charge termination when:

The battery current drops below the **Taper Current** for two consecutive **Current Taper Window** time periods during charging AND battery voltage is equal to or higher than the **Charging Voltage – Taper Voltage**. Full Charge is set when the taper condition is met.

### Charge Inhibit

The bq28z560 can indicate when battery temperature has fallen below or risen above predefined thresholds **Charge Inhibit Temp Low** or **Charge Inhibit Temp High**. In this mode, the CHG\_FET bit is set in the Control register to indicate this condition, and is returned to its low state, once battery temperature returns to the range [**Charge Inhibit Temp Low + Temp Hys**, **Charge Inhibit Temp High – Temp Hys**]. This is implemented to indicate that an action is required by the battery charger.

The charging should not start when the temperature is below the **Charge Inhibit Temp Low** or above the **Charge Inhibit Temp High**.

The charge FET should not turn off when Temp > Chg Inhibit Temp during charging .

The gas gauge will enter charge inhibit mode only if it is in discharge mode or RELAX mode and Temp > Chg Inhibit Low. Then it will set the Charging Current and Charging Voltage values to 0.

### POWER MODES

The bq28z560 has four power modes: NORMAL, SLEEP, HIBERNATE, and SHUTDOWN. In NORMAL mode, the bq28z560 is fully powered and can execute any allowable task. In SLEEP mode, the gas gauge exists in a reduced-power state, periodically taking measurements and performing calculations. In HIBERNATE mode, the gas gauge is in a low power state, but can be awoken by communication or certain I/O activity. The device enters SHUTDOWN mode if there is an BATLOW condition detected or power down of the system.

[Figure 7](#) shows the relationship between these modes. The sections that follow describe the details.

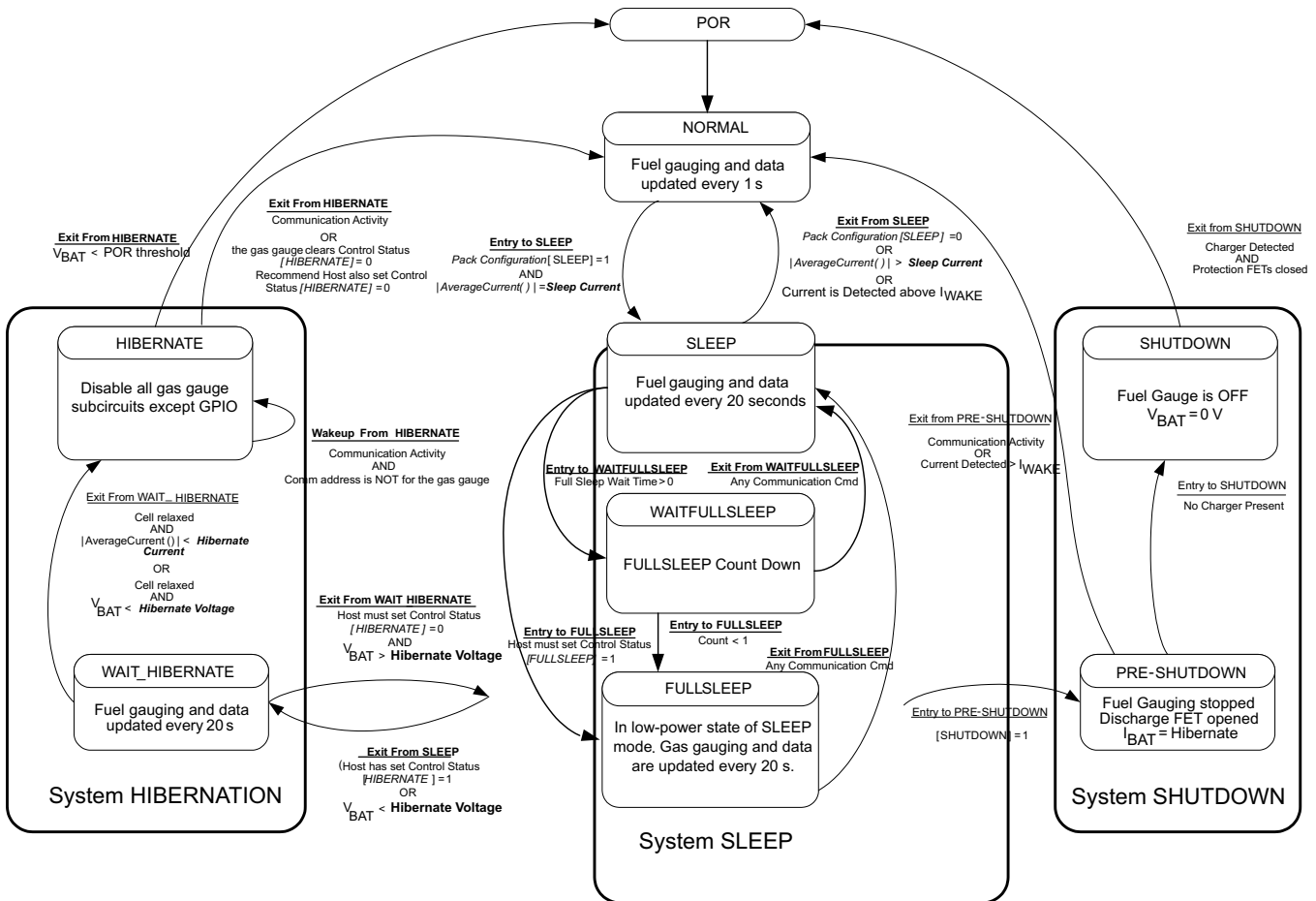


Figure 7. Power Mode Diagram

## NORMAL MODE

The gas gauge is in NORMAL mode when not in any other power mode. During this mode, *AverageCurrent()*, *Voltage()*, and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

Because the gauge consumes the most power in NORMAL mode, the algorithm minimizes the time the gas gauge remains in this mode.

### NOTE

When the battery is connected for the first time, discharging may not be enabled. For this case, one of the following procedures is required:

Short the VM pin to the VSS pin or connect the charger such that the IC returns to normal status.

## SLEEP MODE

SLEEP mode is entered automatically if the feature is enabled (**Pack Configuration [SLEEP]** = 1) and *AverageCurrent()* is below the programmable level **Sleep Current**. Once entry into SLEEP mode has been qualified, but prior to entering it, the bq28z560 performs an ADC auto-calibration to minimize offset.

While in SLEEP mode, the gas gauge can suspend serial communications as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, since the gas gauge processor is mostly halted in SLEEP mode.

During the SLEEP mode, bq28z560 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition. The bq28z560 exits SLEEP if any entry condition is broken, specifically when (1) *AverageCurrent()* rises above **Sleep Current**, or (2) a current in excess of  $I_{WAKE}$  through RSENSE is detected.

## FULLSLEEP MODE

FULLSLEEP mode is entered automatically if the feature is enabled by setting the **Configuration [FULLSLEEP]** bit in the Control Status register when the bq28z560 is in SLEEP mode. The gauge exits the FULLSLEEP mode when there is any communication activity. Therefore, the execution of SET\_FULLSLEEP sets the **[FULLSLEEP]** bit, but EVSW might still display the bit clear. The FULLSLEEP mode can be verified by measuring the current consumption of the gauge. In this mode, the high frequency oscillator is turned off. The power consumption is further reduced in this mode compared to the SLEEP mode.

FULLSLEEP mode can also be entered by setting the **Full Sleep Wait Time** to be a number larger than 0. FULLSLEEP will be entered when the timer counts down to 0. This feature is disabled when the data flash is set as 0.

During FULLSLEEP mode, the bq28z560 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The bq28z560 exits SLEEP if any entry condition is broken, specifically when (1) *AverageCurrent()* rises above **Sleep Current**, or (2) a current in excess of  $I_{WAKE}$  through RSENSE is detected.

While in FULLSLEEP mode, the gas gauge can suspend serial communications as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, since the gas gauge processor is mostly halted in SLEEP mode.

### Clearing FULLSLEEP Mode

FULLSLEEP mode will stay on permanently if **Full Sleep Wait Time** is not set to 0.

Clearing FULLSLEEP mode:

- If **Full Sleep Wait Time** is set to 0, the CLEAR condition clears the flag. If it is not set to 0, the CLEAR condition resets the timer.
- The CLEAR condition determines that there is I<sup>2</sup>C communication while FULLSLEEP is active. I<sup>2</sup>C communication while not in FULLSLEEP will NOT clear the flag. This means if there is current flowing when the FULLSLEEP command is sent, there is no way to clear it until after the device enters SLEEP mode.

## HIBERNATE MODE

HIBERNATE mode should be used when the host system needs to enter a low-power state, and minimal gauge power consumption is required. This mode is ideal when the host is set to its own HIBERNATE, SHUTDOWN, or OFF modes. The gas gauge can enter HIBERNATE due to either low cell voltage or low load current.

- HIBERNATE due to the load current—If the gas gauge enters the HIBERNATE mode due to the load current, the [HIBERNATE] bit of the CONTROL\_STATUS register must be set. The gauge waits to enter HIBERNATE mode until it has taken a valid OCV measurement and the magnitude of the average cell current has fallen below Hibernate Current.
- HIBERNATE due to the cell voltage—When the cell voltage drops below the Hibernate Voltage and a valid OCV measurement has been taken, the gas gauge enters HIBERNATE mode. The [HIBERNATE] bit of the CONTROL register has no impact for the gas gauge to enter the HIBERNATE mode. If the [SHUTDOWN] bit of CONTROL\_STATUS is also set.

The gauge will remain in HIBERNATE mode until communication activity appears on the communication lines. Upon exiting HIBERNATE mode, the **[HIBERNATE]** bit of CONTROL\_STATUS is cleared.

Because the gas gauge is dormant in HIBERNATE mode, the battery should not be charged or discharged in this mode, because any changes in battery charge status will not be measured. If necessary, the host equipment can draw a small current (generally infrequent and less than 1 mA, for purposes of low-level monitoring and updating); however, the corresponding charge drawn from the battery will not be logged by the gauge. Once the gauge exits to NORMAL mode, the algorithm re-establishes the correct battery capacity.

If a charger is attached, the host should immediately take the gas gauge out of HIBERNATE mode before beginning to charge the battery.

#### **CAUTION**

Charging the battery in HIBERNATE mode results in a notable gauging error that will take several hours to correct. In the HDQ bus communication interface, the bus line when in Hibernate mode must always be pulled high with external resistor, and not allowed to go low in this mode. If the bus line is pulled low the system may have to go through a full reset by the battery pack being removed and re-inserted. This may be an issue for systems with embedded battery packs. Alternatively, disable HIBERNATE mode by setting CLEAR\_HIBERNATE bit to 0. Another option is to set Hibernate I,V settings to 0 in DF commands.

### **SHUTDOWN MODE**

The device enters SHUTDOWN mode if there is a BATLOW condition detected or power down of the system. The device can also disable SHUTDOWN by using the CLEAR\_SHUTDOWN (0x0014) option.

#### **NOTE**

- A SHUTDOWN command should NOT be invoked if charger voltage is present.
- Sending a SHUTDOWN command while charger voltage is present causes a 1–2 s time of DSG FET off, and may or may not cause a watchdog reset. (If current is  $\leq 0$  after the DSG FET is opened, it will attempt to shutdown and start a watchdog; otherwise, it will only clear the shutdown flag without a reset).
- The recommendation is to NOT send a SHUTDOWN command if charger voltage is present

[Figure 8](#) shows an overview of the hardware controlled SHUTDOWN operation.

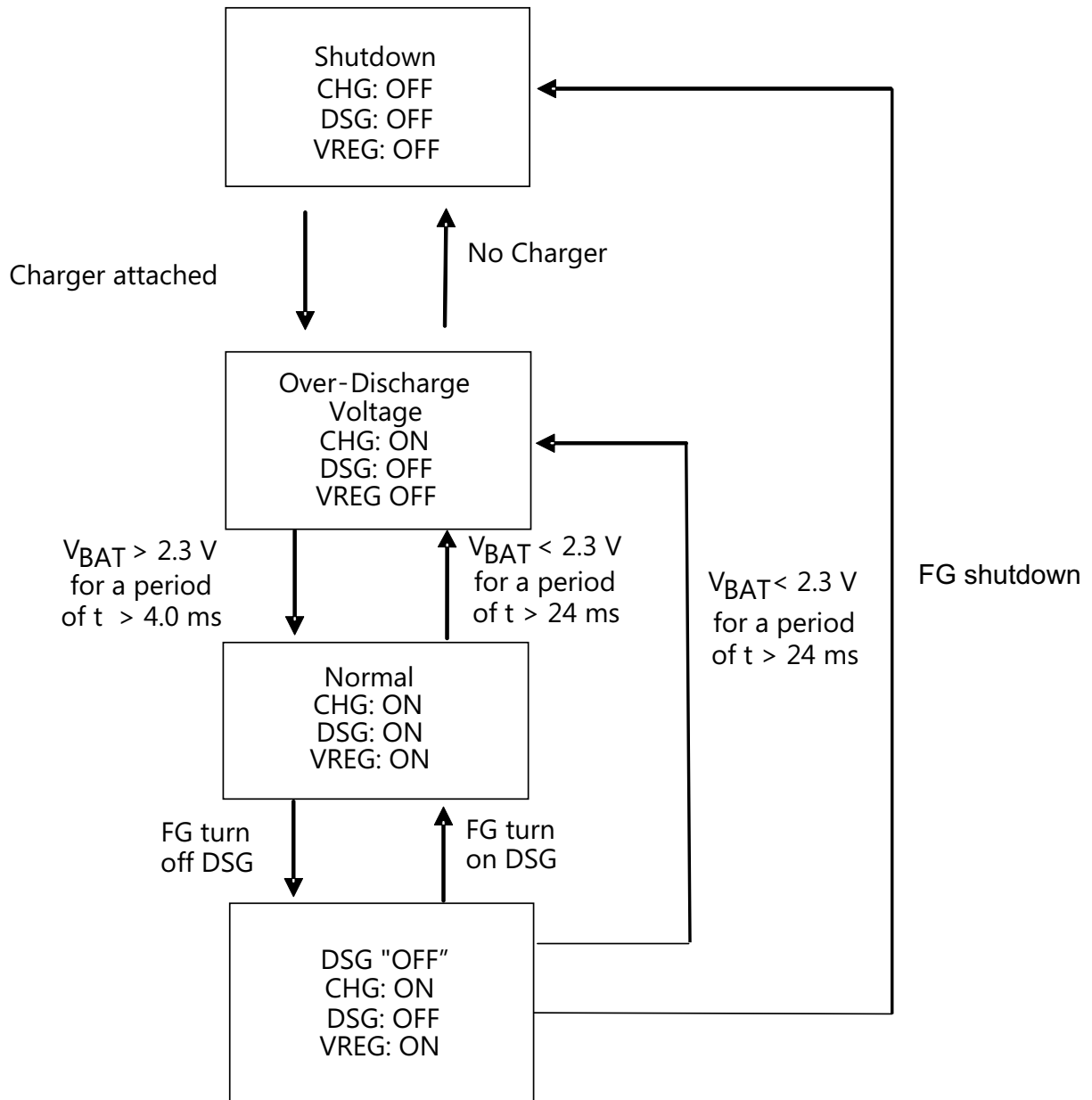


Figure 8. Shutdown Operation



## OPERATIONAL MODES

### POWER CONTROL

#### Reset Functions

When the bq28z560 detects a software reset ([RESET] bit of *Control()* initiated), it determines the type of reset and increments the corresponding counter. This information is accessible by issuing the command *Control()* function with the RESET\_DATA subcommand.

#### Wake-Up Comparator

The wake up comparator is used to indicate a change in cell current while the bq28z560 is in SLEEP modes. *Pack Configuration* uses bits [RSNS1–RSNS0] to set the sense resistor selection. **Pack Configuration** also uses the [IWAKE] bit to select one of two possible voltage threshold ranges for the given sense resistor selection. An internal interrupt is generated when the threshold is breached in either charge or discharge directions. Setting both [RSNS1] and [RSN0] to 0 disables this feature.

**Table 21. IWAKE Threshold Settings(1)**

| RSNS1 | RSNS0 | IWAKE | Vth (SRP–SRN)      |
|-------|-------|-------|--------------------|
| 0     | 0     | 0     | Disabled           |
| 0     | 0     | 1     | Disabled           |
| 0     | 1     | 0     | +1.0 mV or –1.0 mV |
| 0     | 1     | 1     | +2.2 mV or –2.2 mV |
| 1     | 0     | 0     | +2.2 mV or –2.2 mV |
| 1     | 0     | 1     | +4.6 mV or –4.6 mV |
| 1     | 1     | 0     | +4.6 mV or –4.6 mV |
| 1     | 1     | 1     | +9.8 mV or –9.8 mV |

(1) The actual resistance value vs the setting of the sense resistor is not important just the actual voltage threshold when calculating the Configuration. The voltage thresholds are typical values under room temperature.

#### Flash Updates

Data flash can only be updated if *Voltage()* > Flash Update OK Voltage. Flash programming current can cause an increase in the LDO dropout.

The mode of going from one state to another is as follows, NORMAL → SLEEP → FULLSLEEP. Then from FULLSLEEP either HIBERNATE or SHUTDOWN.

| Mode      | Enter Mode  | Exit Mode  | Comment  |
|-----------|---|--|--|
| NORMAL    | If ALL conditions are satisfied like Average Current, Cell Voltage, and Temperature   | Go into other modes like SLEEP, FULLSLEEP, HIBERNATE, or SHUTDOWN mode if conditions are satisfied.                                  | In this mode power consumption is the highest. Measurements are taken and updated every 1 s. |
| SLEEP     | SLEEP bit set = 1 in Control register AND AverageCurrent measured is equal to Sleep current value.  | Change SLEEP bit = 0 OR AverageCurrent measurement > Sleep current value OR Current detected is above the I <sub>WAKE</sub> setting. | The data is measured every 20 s to reduce current consumption.                               |
| FULLSLEEP | From SLEEP mode if the WAIT_FULLSLEEP wait is programmed, this is the time the system must be in SLEEP mode before it can go to FULLSLEEP mode. | The system exits the FULLSLEEP mode if there are any communication commands set on the bus to the device.                            | The wait time to enter FULLSLEEP from SLEEP is 1 s to 240 s with the default at 15 s.        |

| Mode        | Enter Mode  | Exit Mode  | Comment  |
|-------------|---|--|--|
| HIBERNATION | From FULL SLEEP mode, the system will go into HIBERNATE mode if the load current decreases to programmed value, OR if the cell voltage falls below programmed value, OR the host sets the command in MAC. | The system exits this mode if the $V_{BAT} >$ programmed threshold, OR load current is $>$ programmed threshold, OR communication activity on bus line, OR host sets the command in MAC. | Enters hibernation if $V_{BAT}$ range is 2.4 V to 3 V with default at 2.55 V. The load current threshold range is 0 to 0.7 A with a default value of 8 mA. |
| SHUTDOWN    | From SLEEP mode, the system will enter this mode if the $V_{BAT} < 2.4$ V for a period longer than 24 ms and the charger is not attached. The system can also be put in SHUTDOWN mode through MAC.        | Exit from this mode if there is bus activity, OR the load current detected is $> I_{WAKE}$ , OR charger is connected to the system.  | In this mode, the VREG and DSG FET are turned OFF and the system will only wake up if the charger is attached on the Pack+, Pack- terminals.               |

## AUTOCALIBRATION

The bq28z560 provides an auto calibration feature that measures the voltage offset error across SRP and SRN from time-to-time as operating conditions change. It subtracts the resulting offset error from the normal sense resistor voltage, VSR, for maximum measurement accuracy.

Auto calibration of the ADC begins on entry to SLEEP mode, except if *Temperature()* is  $\leq 5^{\circ}\text{C}$  or *Temperature()*  $\geq 45^{\circ}\text{C}$ .

The gas gauge also performs a single offset when (1) the condition of *AverageCurrent()*  $\leq 100$  mA and (2) {cell voltage change since last offset calibration  $\geq 256$  mV} or {temperature change since last offset calibration is greater than  $80^{\circ}\text{C}$  for  $\geq 60$  s}.

Capacity and current measurements continue at the last measured rate during the offset calibration when these measurements cannot be performed. If the battery voltage drops more than 32 mV during the offset calibration, the load current has likely increased considerably and the offset calibration will be aborted.

## COMMUNICATIONS

### AUTHENTICATION

The bq28z560 can act as a SHA-1/HMAC authentication slave by using its internal engine. Refer to the *Using SHA-1 in bq20zxx Family of Gas Gauges* application note ([SLUA359](#)) for SHA-1/HMAC for information.

By sending a 160-bit SHA-1 challenge message to the bq28z560, it causes the gauge to return a 160-bit digest, based upon the challenge message and a hidden, 128-bit plain-text authentication key. If this digest matches an identical one generated by a host or dedicated authentication master, and when operating on the same challenge message and using the same plain text keys, the authentication process is successful.

### KEY PROGRAMMING (DATA FLASH KEY)

By default, the bq28z560 contains a default plain-text authentication key of 0x0123456789ABCDEFEDCBA9876543210. This default key is intended for development purposes. It should be changed to a secret key and the part immediately sealed, before putting a pack into operation. Once written, a new plain-text key cannot be read again from the gas gauge while in SEALED mode.

Once the bq28z560 is UNSEALED, the authentication key can be changed from its default value by writing to the *Authenticate()* Extended Data Command locations. A 0x00 is written to *BlockDataControl()* to enable the authentication data commands. The *DataFlashClass()* is issued 112 (0x70) to set the Security class. Up to 32 bytes of data can be read directly from the *BlockData()* (0x40...0x5f) and the authentication key is located at 0x48 (0x40 + 0x08 offset) to 0x57 (0x40 + 0x17 offset). The new authentication key can be written to the corresponding locations (0x48 to 0x57) using the *BlockData()* command. The data is transferred to the data flash when the correct checksum for the whole block (0x40 to 0x5f) is written to *BlockDataChecksum()* (0x60). The checksum is (255- x) where x is the 8-bit summation of the *BlockData()* (0x40 to 0x5F) on a byte-by-byte basis. Once the authentication key is written, the gauge can then be SEALED again.

### KEY PROGRAMMING (THE SECURE MEMORY KEY)

As the name suggests, the bq28z560 secure-memory authentication key is stored in the secure memory of the bq28z560. If a secure-memory key has been established and the Data Flash Key is 0x00000000000000000000000000000000, only this key can be used for authentication challenges (the programmable data flash key is not available). The selected key can only be established/programmed by special arrangements with TI, using TI's *Secure B-to-B Protocol*. The secure-memory key can never be changed or read from the bq28z560.

### EXECUTING AN AUTHENTICATION QUERY

To execute an authentication query in UNSEALED mode, a host must first write 0x01 to the *BlockDataControl()* command, to enable the authentication data commands. If in SEALED mode, 0x00 must be written to *DataFlashBlock()*, instead.

Next, the host writes a 20-byte authentication challenge to the *Authenticate()* address locations (0x40 through 0x53). After a valid checksum for the challenge is written to *AuthenticateChecksum()*, the bq28z560 uses the challenge to perform the SHA-1/HMAC computation, in conjunction with the programmed key. The resulting digest is written to *AuthenticateData()*, overwriting the pre-existing challenge. The host may then read this response and compare it against the result created by its own parallel computation.

### HDQ SINGLE-PIN SERIAL INTERFACE

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the bq28z560. With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first. Note that the DATA signal on pin 12 is open-drain and requires an external pull-up resistor. The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (MSB bit 7). The R/W field directs the bq28z560 to do either of the following two actions:

- Store the next 8 or 16 bits of data to a specified register or,
- Output 8 bits of data from the specified register.

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

HDQ serial communication is normally initiated by the host processor sending a break command to the bq28z560. A break is detected when the DATA pin is driven to a logic-low state for a time  $t_{(B)}$  or greater. The DATA pin should then be returned to its normal ready high logic state for a time  $t_{(BR)}$ . The bq28z560 is now ready to receive information from the host processor.

The bq28z560 is shipped in the I<sup>2</sup>C mode. TI provides tools to enable the HDQ peripheral.

**HDQ HOST INTERRUPTION FEATURE**

The default bq28z560 behaves as an HDQ slave only device. If the HDQ interrupt function is enabled, the bq28z560 is capable of mastering and also communicating to a HDQ device. There is no mechanism for negotiating who is to function as the HDQ master and care must be taken to avoid message collisions. The interrupt is signaled to the host processor with the bq28z560 mastering an HDQ "message." This message is a fixed message that will be used to signal the interrupt condition. The message itself is 0x80 (slave write to register 0x00) with no data byte being sent as the command is not intended to convey any status of the interrupt condition. The HDQ interrupt function is not public and needs to be enabled by command.

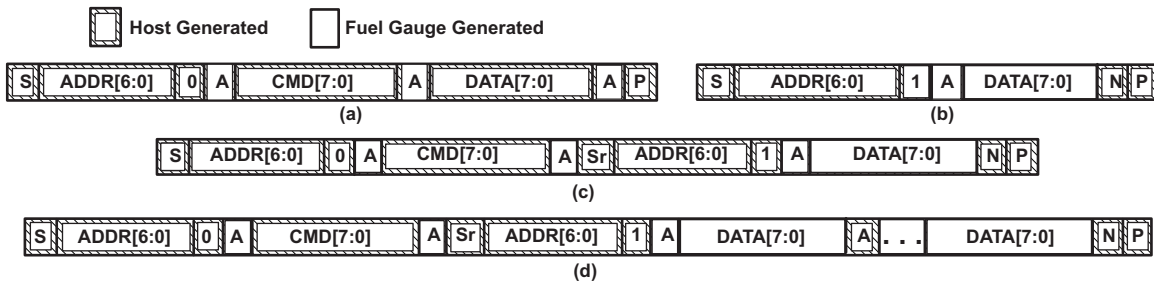
When the SET\_HDQINTEN subcommand is received, the bq28z560 will detect any of the interrupt conditions and assert the interrupt at one second intervals until the CLEAR\_HDQINTEN command is received or the count of HDQHostIntrTries has lapsed.

The number of tries for interrupting the host will be determined the data flash parameter named **Configuration.Register.HDQHostIntrTries**.

The HDQ host interrupt is triggered by the settings in the bat alert feature. The HDQ host interrupt signal will be asserted when the *Flags()[ALRT]* bit is triggered based on the settings in the *BatAlertConfig()* register.

**I<sup>2</sup>C INTERFACE**

The gas gauge supports the standard I<sup>2</sup>C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively.



**Figure 9. Supported I<sup>2</sup>C formats: (a) 1-byte write, (b) quick read, © 1 byte-read, and (d) incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).**

The "quick read" returns data at the address indicated by the address pointer. The address pointer, a register internal to the I<sup>2</sup>C communication engine, increments whenever data is acknowledged by the bq28z560 or the I<sup>2</sup>C master. "Quick writes" function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

Attempt to write a read-only address (NACK after data sent by master):



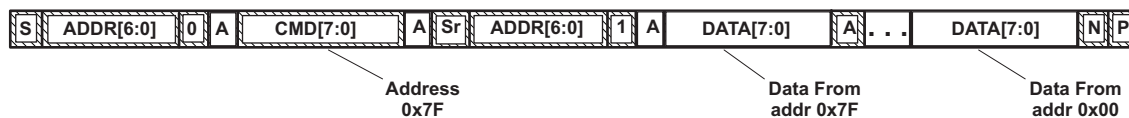
Attempt to read an address above 0x7F (NACK command):



Attempt at incremental writes (NACK all extra data bytes sent):



Incremental read at the maximum allowed read address:



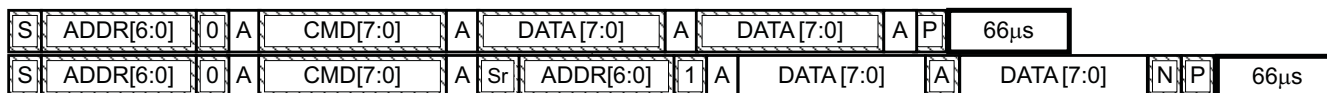
The I<sup>2</sup>C engine releases both SDA and SCL if the I<sup>2</sup>C bus is held low for  $t_{(BUSERR)}$ . If the gas gauge was holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I<sup>2</sup>C engine enters the low-power sleep mode.

**I<sup>2</sup>C Time Out**

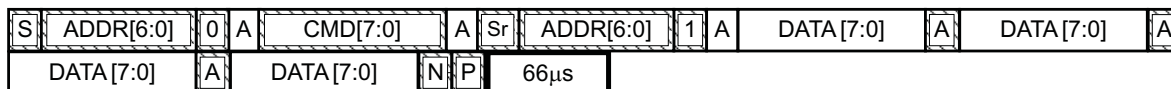
The I<sup>2</sup>C engine will release both SDA and SCL if the I<sup>2</sup>C bus is held low for about 2 s. If the bq28z560 was holding the lines, releasing them will free for the master to drive the lines.

**I<sup>2</sup>C Command Waiting Time**

To ensure getting the correct results of a command with the 400 KHz I<sup>2</sup>C operation, a proper waiting time should be added between issuing command and reading results. For subcommands, the following diagram shows the waiting time required between issuing the control command and reading the status with the exception of the checksum command. A 100-ms waiting time is required between the checksum command and reading result. For read-write standard commands, a minimum of 2 s is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host should not issue all standard commands more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



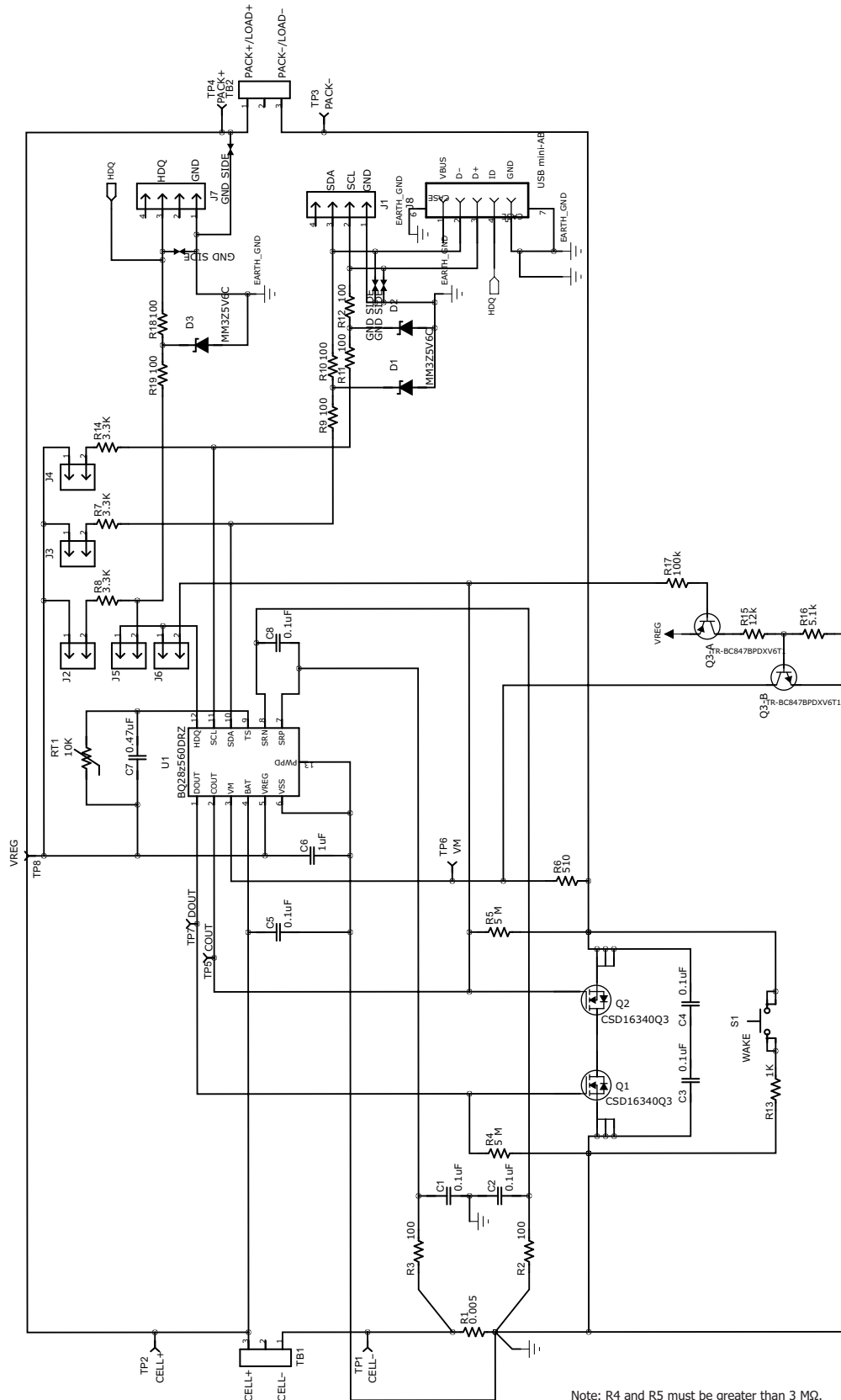
Waiting time between control subcommand and reading results



Waiting time between continuous reading results

The I<sup>2</sup>C clock stretch could happen in a typical application. A maximum 80-ms clock stretch could be observed during the flash updates. There is up to 270-ms clock stretch after the OCV command is issued.

### REFERENCE SCHEMATIC



Note: R4 and R5 must be greater than 3 MΩ.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|---------|
| BQ28Z560DRZR     | PREVIEW       | SON          | DRZ                | 12   |                | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | BQ28<br>Z560             |         |
| BQ28Z560DRZT     | PREVIEW       | SON          | DRZ                | 12   |                | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | BQ28<br>Z560             |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

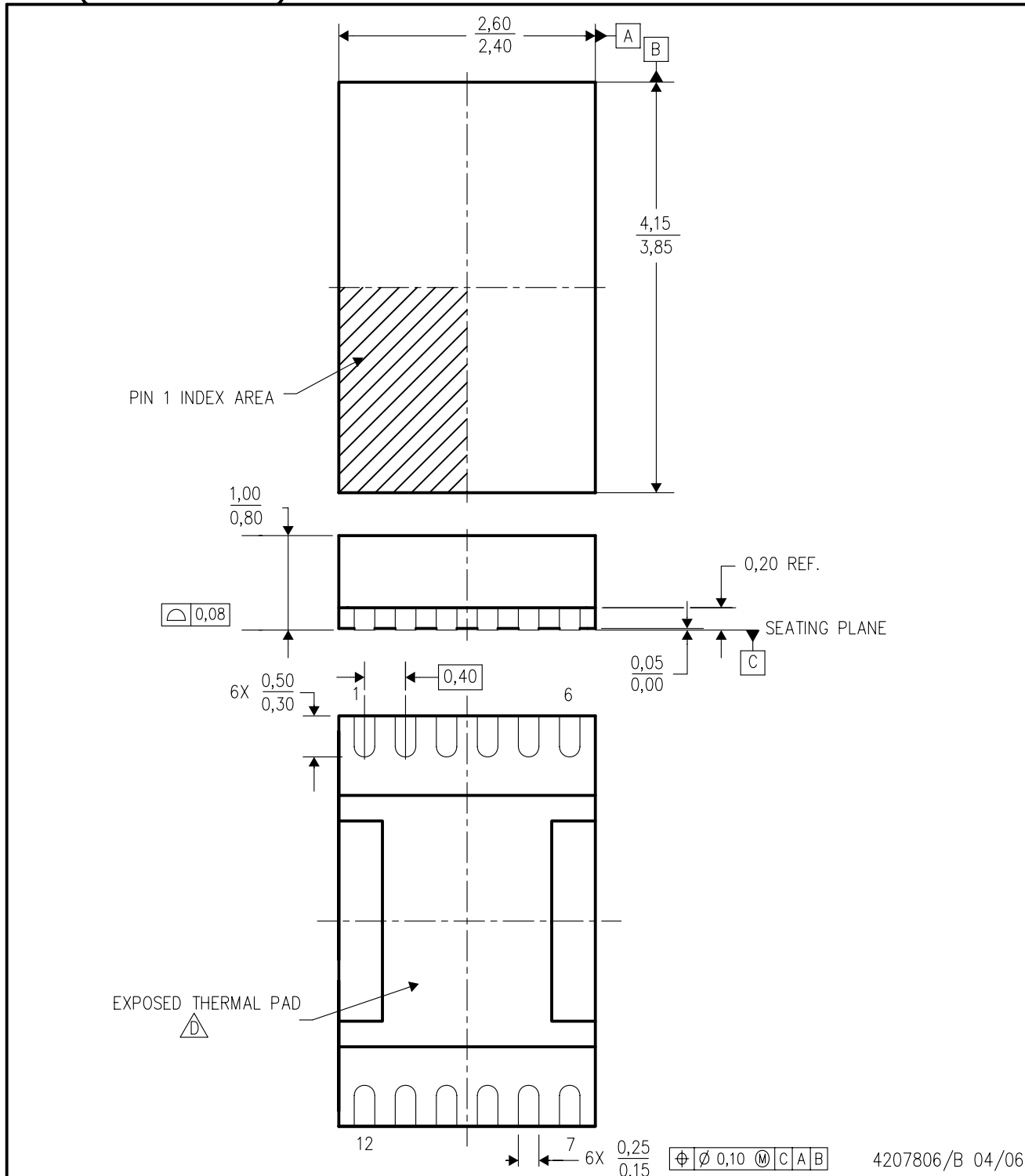
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



DRZ (S-PDSO-N12)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. This package is lead-free.

## THERMAL PAD MECHANICAL DATA

DRZ (R-PDSO-N12)

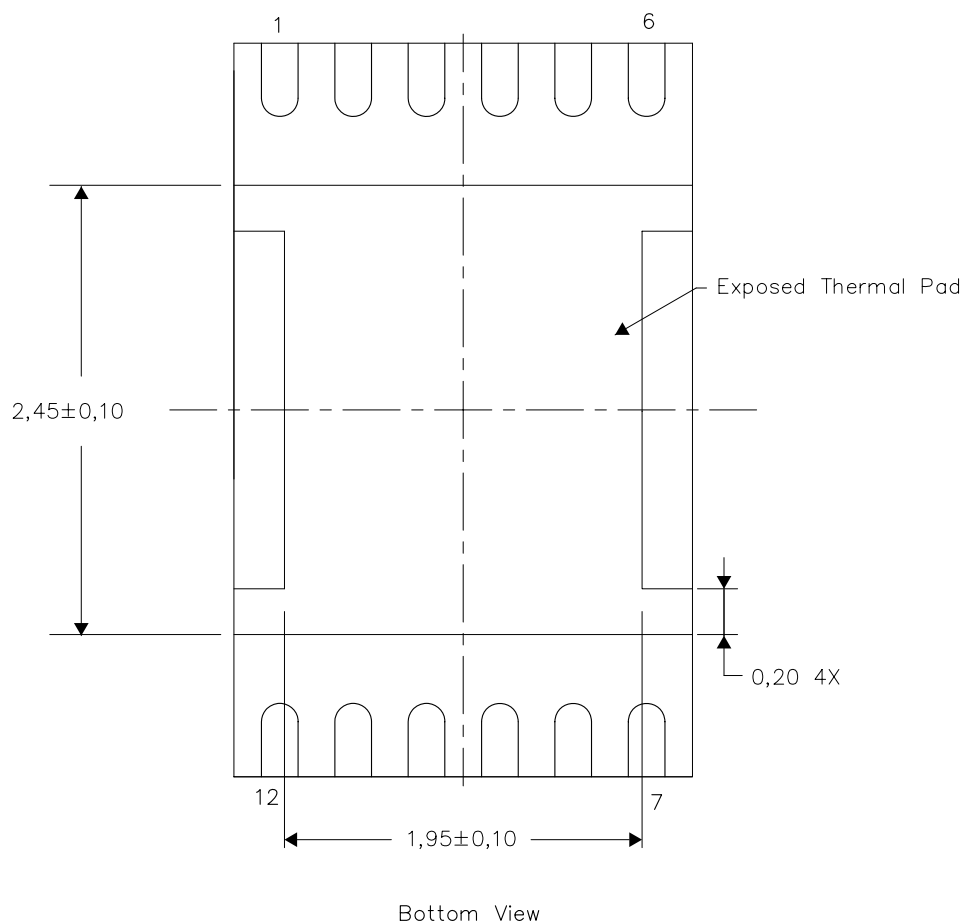
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



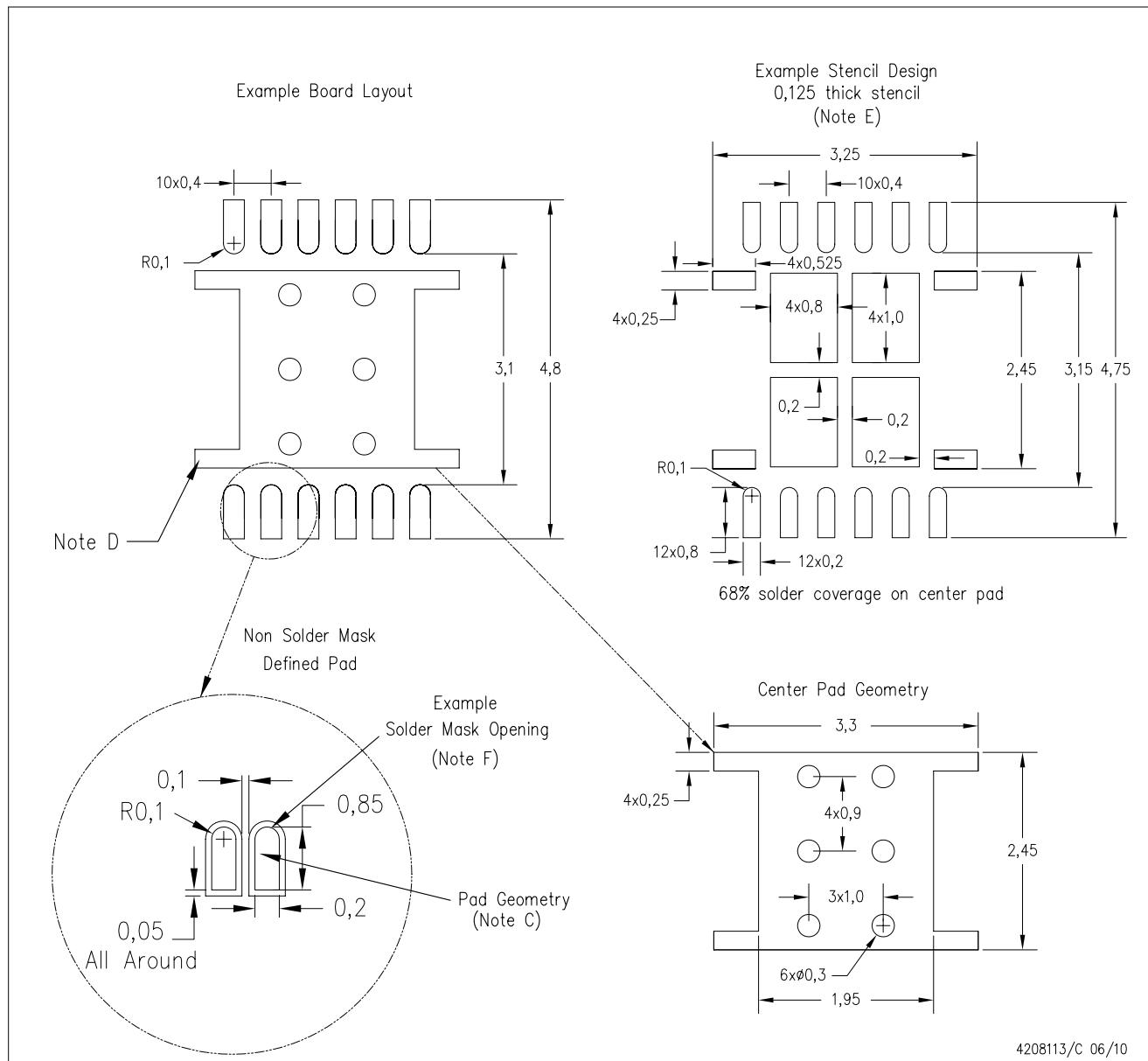
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4208114/E 06/10

DRZ (S-PDSO-N12)

PLASTIC SMALL OUTLINE NO-LEAD



4208113/C 06/10

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)