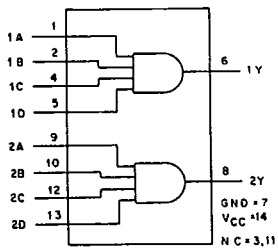


**CD54/74HC21**  
**CD54/74HCT21**

File Number 1782

**High-Speed CMOS Logic**

HARRIS SEMICONDUCTOR 27E D ■ 4302271 0017491 3 ■ HAS



**Dual 4-Input AND Gate**

- Type Features:**
- Buffered inputs
  - Typical propagation delay = 9ns
- @ V<sub>CC</sub> = 5V, C<sub>L</sub> = 15 pF, T<sub>A</sub> = 25°C (HC types)

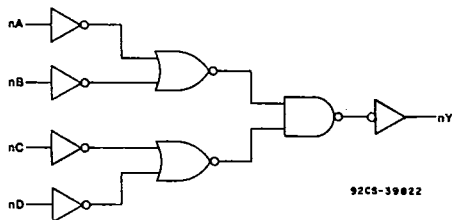
FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

The RCA-CD54/74HC21 and CD54/74HCT21 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC21 and CD54HCT21 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC21 and CD74HCT21 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

**Family Features:**

- Fanout (Over Temperature Range):  
Standard Outputs - 10 LSTTL Loads  
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:  
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:  
2 to 6 V Operation  
High Noise Immunity:  
N<sub>IL</sub> = 30%, N<sub>IH</sub> = 30% of V<sub>CC</sub>; @ V<sub>CC</sub> = 5V
- CD54HCT/CD74HCT Types:  
4.5 to 5.5 V Operation  
Direct LSTTL Input Logic Compatibility  
V<sub>IL</sub> = 0.8 V max., V<sub>IH</sub> = 2 V Min.  
CMOS Input Compatibility  
I<sub>i</sub> ≤ 1 μA @ V<sub>OL</sub>, V<sub>OH</sub>



LOGIC DIAGRAM

TRUTH TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X = Don't Care  
L = Low Level Voltage  
H = High Level Voltage

**CD54/74HC21**  
**CD54/74HCT21**

T-43-21

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE, ( $V_{CC}$ ):  
(Voltages referenced to ground) ..... -0.5 to + 7 V

DC INPUT DIODE CURRENT,  $I_{IK}$  (FOR  $V_i < -0.5$  V OR  $V_i > V_{CC} + 0.5$ V) .....  $\pm 20$ mA

DC OUTPUT DIODE CURRENT,  $I_{OK}$  (FOR  $V_o < -0.5$  V OR  $V_o > V_{CC} + 0.5$ V) .....  $\pm 20$ mA

DC DRAIN CURRENT, PER OUTPUT ( $I_o$ ) (FOR  $-0.5$  V  $< V_o < V_{CC} + 0.5$ V) .....  $\pm 25$ mA

DC  $V_{CC}$  OR GROUND CURRENT ( $I_{CC}$ ) .....  $\pm 50$ mA

POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -40$  to  $+60^\circ$ C (PACKAGE TYPE E) ..... 500 mW

For  $T_A = +60$  to  $+85^\circ$ C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For  $T_A = -55$  to  $+100^\circ$ C (PACKAGE TYPE F, H) ..... 500 mW

For  $T_A = +100$  to  $+125^\circ$ C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For  $T_A = -40$  to  $+70^\circ$ C (PACKAGE TYPE M) ..... 400 mW

For  $T_A = +70$  to  $+125^\circ$ C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/ $^\circ$ C to 70 mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F, H .....  $-55$  to  $+125^\circ$ C

PACKAGE TYPE E, M .....  $-40$  to  $+85^\circ$ C

STORAGE TEMPERATURE ( $T_{STG}$ ) .....  $-65$  to  $+150^\circ$ C

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$  mm) from case for 10 s max. ....  $+265^\circ$ C

Unit inserted into a PC Board (min. thickness  $1/16$  in., 1.59 mm) with solder contacting lead tips only .....  $+300^\circ$ C

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) $V_{CC}$ .* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature $T_A$ : CD74 Types CD54 Types	-40 -55	+85 +125	$^\circ$ C
Input Rise and Fall Times $t_r, t_f$ at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

\*Unless otherwise specified, all voltages are referenced to Ground.

**CD54/74HC21**  
**CD54/74HCT21**

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC21/CD54HC21										CD74HCT21/CD54HCT21										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE			
	V <sub>i</sub> V	I <sub>o</sub> mA	V <sub>cc</sub> V	+25°C			-40/ +85°C		-55/ +125°C		V <sub>i</sub> V	V <sub>cc</sub> V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V <sub>ih</sub>			2	1.5	—	—	1.5	—	1.5	—	—	4.5								V	
			4.5	3.15	—	—	3.15	—	3.15	—	to	2	—	—	2	—	2	—			
			6	4.2	—	—	4.2	—	4.2	—	5.5										
Low-Level Input Voltage V <sub>il</sub>			2	—	—	0.5	—	0.5	—	0.5	—	4.5								V	
			4.5	—	—	1.35	—	1.35	—	1.35	to	—	—	0.8	—	0.8	—	0.8	—		
			6	—	—	1.8	—	1.8	—	1.8	5.5										
High-Level Output Voltage V <sub>oh</sub>	V <sub>ih</sub>	-0.02	2	1.9	—	—	1.9	—	1.9	—	V <sub>ih</sub>	4.5	4.4	—	—	4.4	—	4.4	—	V	
or			4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—		
CMOS Loads	V <sub>ih</sub>		6	5.9	—	—	5.9	—	5.9	—	V <sub>ih</sub>										
TTL Loads	V <sub>ih</sub>									V <sub>ih</sub>	V <sub>ih</sub>	4.5	3.98	—	—	3.84	—	3.7	—	V	
or		-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—		
V <sub>ih</sub>		-5.2	6	5.48	—	—	5.34	—	5.2	—	V <sub>ih</sub>										
Low-Level Output Voltage V <sub>ol</sub>	V <sub>ih</sub>	0.02	2	—	—	0.1	—	0.1	—	0.1	V <sub>ih</sub>	4.5	—	—	0.1	—	0.1	—	0.1	V	
or			4.5	—	—	0.1	—	0.1	—	0.1	—	or	4.5	—	—	0.1	—	0.1	—		
CMOS Loads	V <sub>ih</sub>		6	—	—	0.1	—	0.1	—	0.1	—	V <sub>ih</sub>									
TTL Loads	V <sub>ih</sub>									V <sub>ih</sub>	V <sub>ih</sub>	4.5	—	—	0.26	—	0.33	—	0.4	V	
or		4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4		
V <sub>ih</sub>		5.2	6	—	—	0.26	—	0.33	—	0.4	V <sub>ih</sub>										
Input Leakage Current I <sub>i</sub>	V <sub>cc</sub> or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V <sub>cc</sub> & Grid	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I <sub>cc</sub>	V <sub>cc</sub> or Gnd	0	6	—	—	2	—	20	—	40	V <sub>cc</sub> or Gnd	5.5	—	—	2	—	20	—	40	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI <sub>cc</sub> *											V <sub>cc</sub> -2.1	4.5	—	—	100	360	—	450	—	490	μA
											5.5	to	—	—	—	—	—	—	—		

\*For dual-supply systems theoretical worst case (V<sub>i</sub> = 2.4 V, V<sub>cc</sub> = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
ALL	1

\*Unit load is ΔI<sub>cc</sub> limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HARRIS SEMICONDUCTOR SECTOR 27E D 4302271 0017493 7 HAS

**CD54/74HC21**  
**CD54/74HCT21**

T-43-21

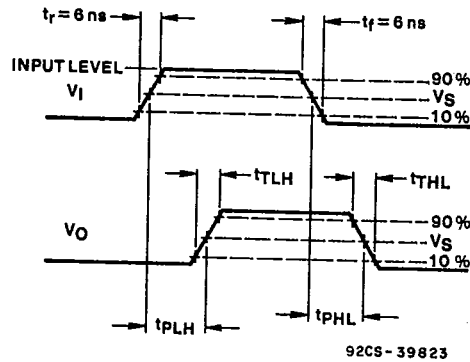
SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Input  $t_r$ ,  $t_f = 6\text{ ns}$ )

CHARACTERISTIC	CL (pF)	TYPICAL		UNITS
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1)	$t_{PHL}$ , $t_{PLH}$	9	11	ns
Power Dissipation Capacitance*	$C_{PD}$	36	42	pF

\* $C_{PD}$  is used to determine the dynamic power consumption, per gate.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where:  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage

SWITCHING CHARACTERISTICS ( $C_L = 50\text{ pF}$ , Input  $t_r$ ,  $t_f = 6\text{ ns}$ )

CHARACTERISTIC	$V_{CC}$	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	$t_{PLH}$	—	110	—	—	—	140	—	—	—	165	—	—	ns
	$t_{PHL}$	4.5	22	—	27	—	28	—	34	—	33	—	41	
		6	19	—	—	—	24	—	—	—	28	—	—	
Transition Times (Fig. 1)	$t_{TLH}$	2	75	—	—	—	95	—	—	—	110	—	—	ns
	$t_{THL}$	4.5	15	—	15	—	19	—	19	—	22	—	22	
		6	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	$C_i$	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	$V_{CC}$	3V
Switching Voltage, $V_s$	50% $V_{CC}$	1.3 V

Fig. 1 — Transition times and propagation delay times.