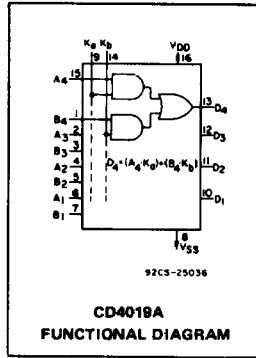


CD4019A Types

CMOS Quad AND/OR Select Gate

The RCA-CD4019A types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B . In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical $A + B$ function.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, Absolute-Maximum Values:

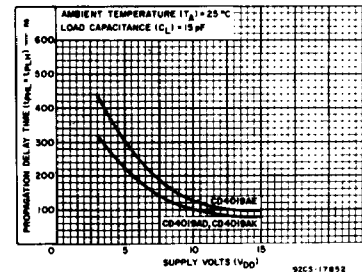
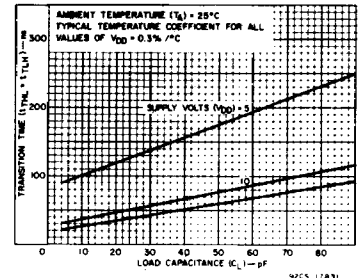
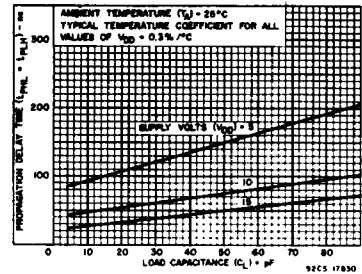
- STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to +150°C
- OPERATING-TEMPERATURE RANGE (T_A):
 - PACKAGE TYPES D, F, K, H -55 to +125°C
 - PACKAGE TYPE E -40 to +85°C
- DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 - (Voltages referenced to V_{SS} Terminal) -0.5 to +15 V
- POWER DISSIPATION PER PACKAGE (P_D)
 - FOR $T_A = -40$ to +60°C (PACKAGE TYPE E) 500 mW
 - FOR $T_A = +60$ to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 - FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K) 500 mW
 - FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 - FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) 100 mW
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V
- LEAD TEMPERATURE (DURING SOLDERING):
 - At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max +265°C

Features:

- Medium-speed operation
 - . . . $t_{PHL} = t_{PLH} = 50$ ns (typ.) at $C_L = 15$ pF, $V_{DD} = 10$ V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	12	3	12	

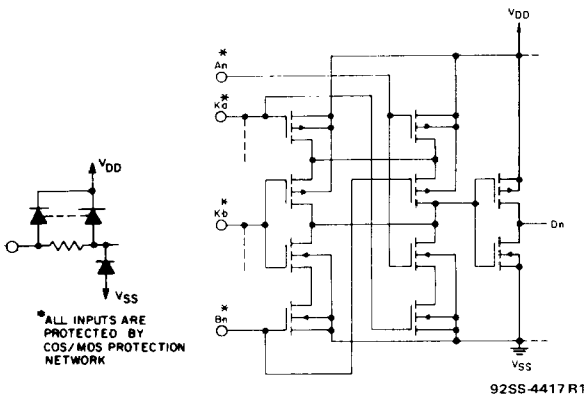
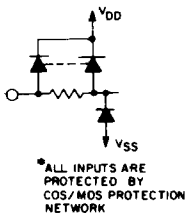


Fig. 1 – Schematic diagram for 1 of 4 identical stages.



CD4019A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
Quiescent Device Current, I _L Max.	-	-	5	5	0.03	5	300	50	0.1	50	700	μA
	-	-	10	10	0.05	10	600	100	0.2	100	1400	
	-	-	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V _{OL}	-	5	5	0 Typ.; 0.05 Max.								V
	-	10	10	0 Typ.; 0.05 Max.								
	High Level V _{OH}	-	0	5	4.95 Min.; 5 Typ.							
Noise Immunity: Inputs Low, V _{NL}	3.6	-	5	1.5 Min.; 2.25 Typ.								V
	7.2	-	10	3 Min.; 4.5 Typ.								
Inputs High V _{NH}	1.4	-	5	1.5 Min.; 2.25 Typ.								V
	2.8	-	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V _{NML}	4.5	-	5	1 Min.								V
	9	-	10	1 Min.								
	Inputs High, V _{NMH}	0.5	-	5	1 Min.							
Output Drive Current: n-Channel (Sink) I _{DN} Min.	0.5	-	5	0.6	0.9	0.45	0.3	0.37	1	0.3	0.23	mA
	0.5	-	10	0.9	1.5	0.75	0.55	0.8	1.5	0.65	0.5	
p-Channel (Source): I _{DP} Min.	4.5	-	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	mA
	9.5	-	10	-0.95	-1.5	-0.7	-0.5	-0.6	-1.5	-0.5	-0.4	
Input Leakage Current, I _{IL} , I _{IH}	Any Input			±10 ⁻⁵ Typ., ±1 Max.								μA

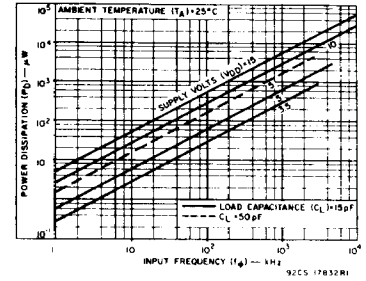


Fig. 5 - Typical dissipation characteristics. (per output).

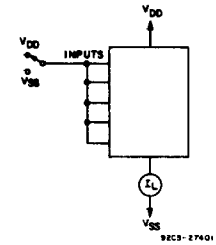


Fig. 6 - Quiescent-device-current test circuit.

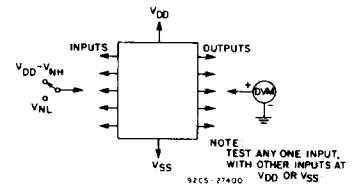


Fig. 7 - Noise-immunity test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS	
		D, F, K, H Packages			E Package				
		V _{DD} (V)	Min.	Typ.	Max.	Min.	Typ.		Max.
Propagation Delay Time; t _{PLH} , t _{PHL}		5	-	100	225	-	100	300	ns
		10	-	50	100	-	50	125	
Transition Time; t _{THL} , t _{TLH}		5	-	100	200	-	100	275	ns
		10	-	40	65	-	40	80	
Average Input Capacitance, C _I	All A and B Inputs	-	5	-	-	5	-	pF	
	K _a and K _b Inputs	-	12	-	-	12	-	pF	

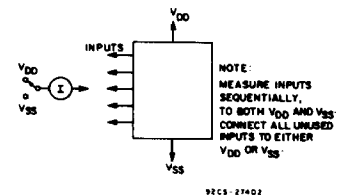


Fig. 8 - Input-leakage-current test circuit.