

PHD108NQ03LT

N-channel TrenchMOS logic level FET

Rev. 04 — 5 June 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

1.4 Quick reference data

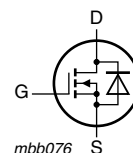
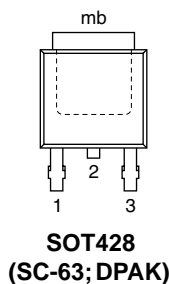
Table 1. Quick reference

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 25 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ see Figure 1 ; see Figure 3 | - | - | 75 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | - | 187 | W |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C};$ $I_D = 43\text{ A}; V_{sup} \leq 25\text{ V};$ unclamped; $t_p = 0.25\text{ ms};$ $R_{GS} = 50\text{ }\Omega$ | - | - | 180 | mJ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 12\text{ V}; T_j = 25\text{ °C};$ see Figure 12 ; see Figure 13 | - | 5.6 | - | nC |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 10 ; see Figure 11 | - | 5.3 | 6 | m Ω |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--------------------|----------------|
| 1 | G | gate | | |
| 2 | D | drain [1] | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |



[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|--------------|-------------|---|---------|
| | Name | Description | |
| PHD108NQ03LT | SC-63; DPAK | plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) | SOT428 |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

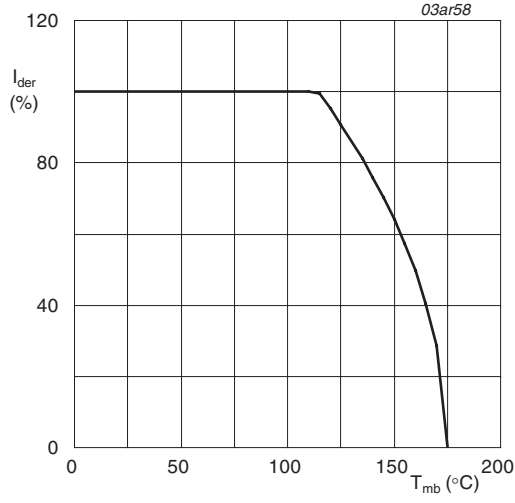
| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | 25 | V |
| V_{DGR} | drain-gate voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 25 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3 | - | 75 | A |
| | | $V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1 | - | 75 | A |
| I_{DM} | peak drain current | $t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3 | - | 240 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; see Figure 2 | - | 187 | W |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |

Source-drain diode

| | | | | | |
|----------|---------------------|--|---|-----|---|
| I_S | source current | $T_{mb} = 25\text{ °C}$ | - | 75 | A |
| I_{SM} | peak source current | $t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$ | - | 240 | A |

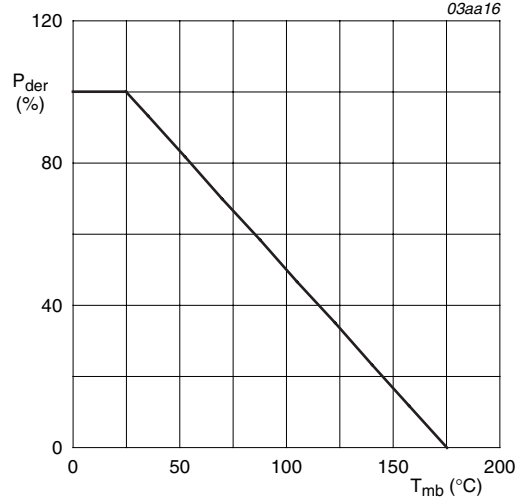
Avalanche ruggedness

| | | | | | |
|---------------|--|---|---|-----|----|
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 43\text{ A}$; $V_{sup} \leq 25\text{ V}$; unclamped; $t_p = 0.25\text{ ms}$; $R_{GS} = 50\text{ }\Omega$ | - | 180 | mJ |
|---------------|--|---|---|-----|----|



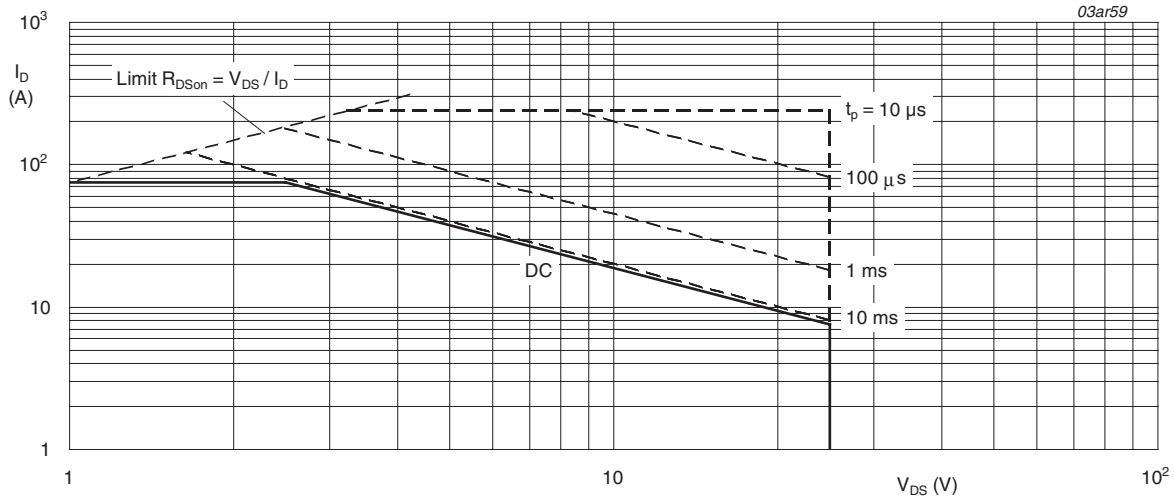
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25^\circ\text{C}; I_{DM} \text{ is single pulse}; V_{GS} = 5\text{V}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 0.8 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint; mounted on a printed-circuit board; vertical in still air | - | 75 | - | K/W |
| | | mounted on a printed-circuit board; vertical in still air; SOT404 minimum footprint | - | 50 | - | K/W |

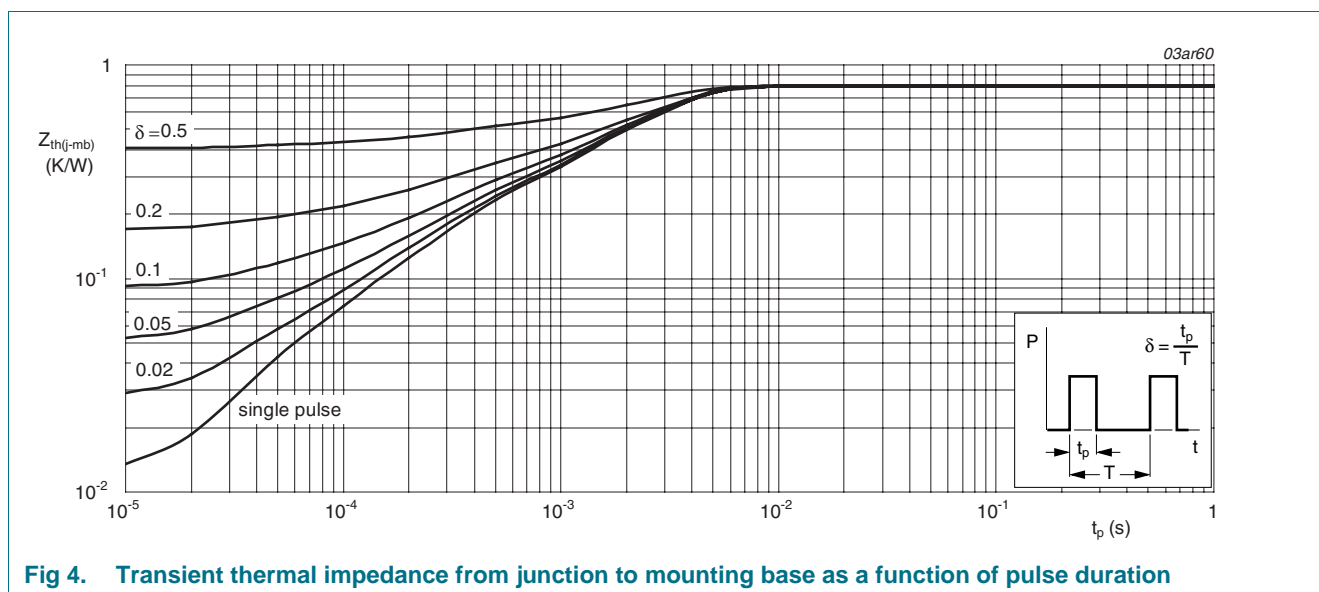


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

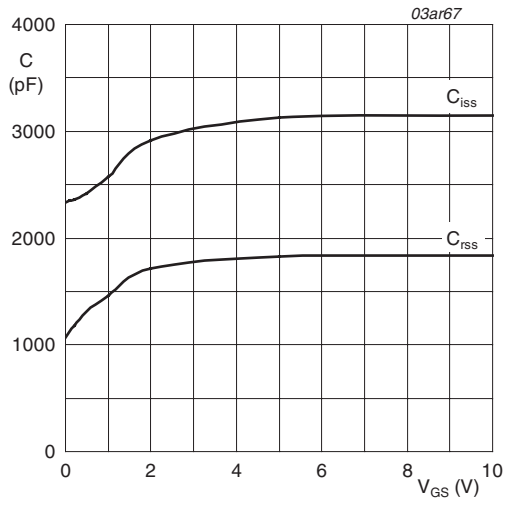
6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------|---|-----|------|-----|---------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 25 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 22 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 8 ; see Figure 9 | 1 | 1.5 | 2 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 8 ; see Figure 9 | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 8 ; see Figure 9 | - | - | 2.2 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | 1 | μA |
| | | $V_{DS} = 25 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 100 | nA |
| | | $V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 100 | nA |

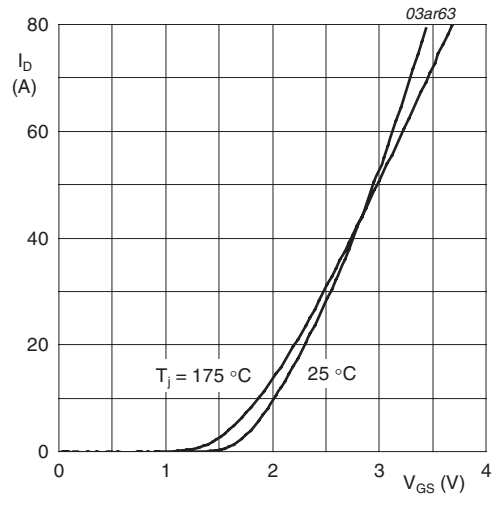
Table 6. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|---|-----|------|------|------|
| R _{DSon} | drain-source on-state resistance | V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 10 ; see Figure 11 | - | 6.7 | 7.5 | mΩ |
| | | V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 10 ; see Figure 11 | - | 12.1 | 13.5 | mΩ |
| | | V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 10 ; see Figure 11 | - | 5.3 | 6 | mΩ |
| R _G | internal gate resistance (AC) | f = 1 MHz; T _j = 25 °C | - | 1.2 | - | Ω |
| Dynamic characteristics | | | | | | |
| Q _{G(tot)} | total gate charge | I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; T _j = 25 °C; see Figure 12 ; see Figure 13 | - | 16.3 | - | nC |
| | | I _D = 0 A; V _{DS} = 0 V; V _{GS} = 4.5 V; T _j = 25 °C | - | 12.5 | - | nC |
| Q _{GS} | gate-source charge | I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; T _j = 25 °C; see Figure 12 ; see Figure 13 | - | 4 | - | nC |
| Q _{GS1} | pre-threshold gate-source charge | | - | 2.5 | - | nC |
| Q _{GS2} | post-threshold gate-source charge | | - | 1.5 | - | nC |
| Q _{GD} | gate-drain charge | | - | 5.6 | - | nC |
| V _{GS(pl)} | gate-source plateau voltage | I _D = 25 A; V _{DS} = 12 V; T _j = 25 °C; see Figure 12 ; see Figure 13 | - | 2.4 | - | V |
| C _{iss} | input capacitance | V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 14 | - | 1375 | - | pF |
| | | V _{DS} = 0 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 14 | - | 2120 | - | pF |
| C _{oss} | output capacitance | V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 14 | - | 640 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 250 | - | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 12 V; R _L = 0.5 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5.6 Ω; T _j = 25 °C | - | 15 | - | ns |
| t _r | rise time | | - | 38 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 32 | - | ns |
| t _f | fall time | | - | 25 | - | ns |
| Source-drain diode | | | | | | |
| V _{SD} | source-drain voltage | I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 15 | - | 0.86 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C | - | 34 | - | ns |
| Q _r | recovered charge | | - | 21 | - | nC |



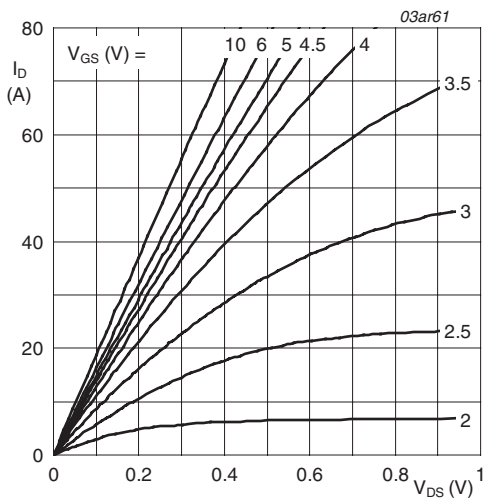
$V_{DS} = 0V$

Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



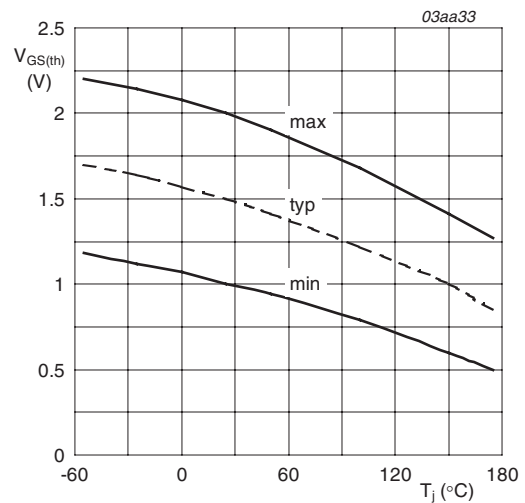
$T_j = 25^\circ C$ and $175^\circ C; V_{DS} > I_D \times R_{Dson}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



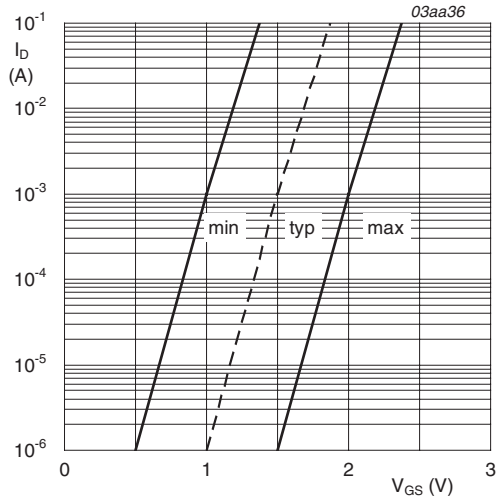
$T_j = 25^\circ C$

Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values



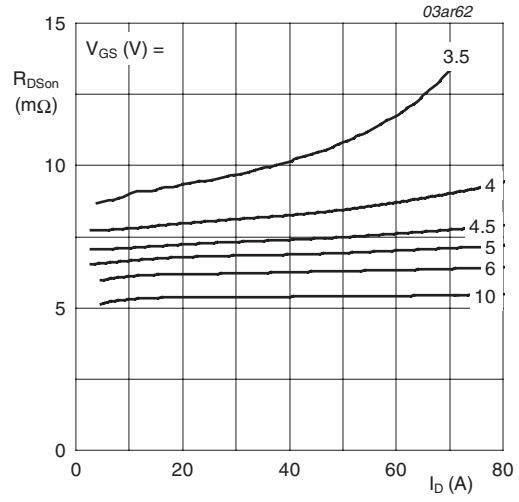
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



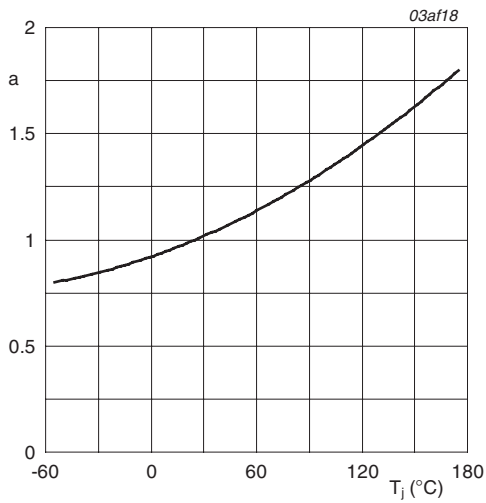
$$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



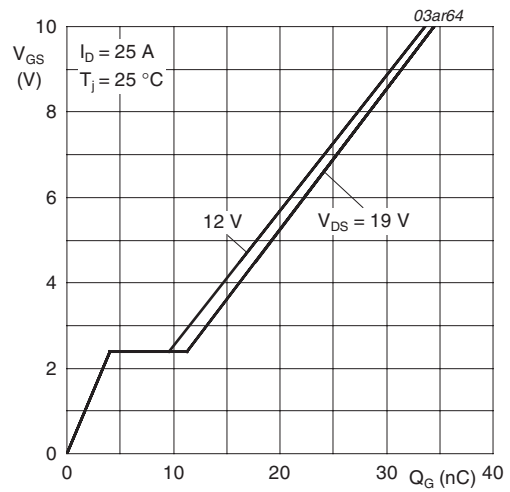
$$T_j = 25^\circ\text{C}$$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$$I_D = 25\text{A}; V_{DS} = 12\text{V and } 19\text{V}$$

Fig 12. Gate-source voltage as a function of gate charge; typical values

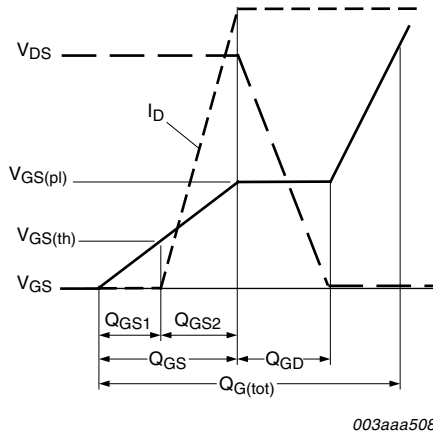
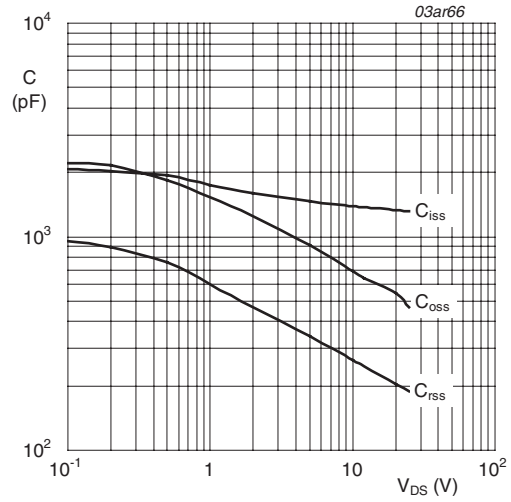
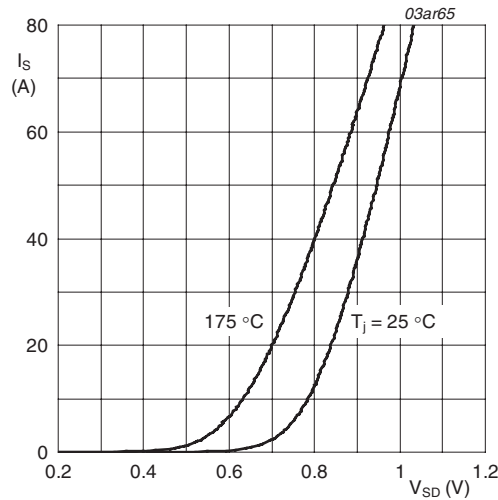


Fig 13. Gate charge waveform definitions



$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ C \text{ and } 175^\circ C; V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

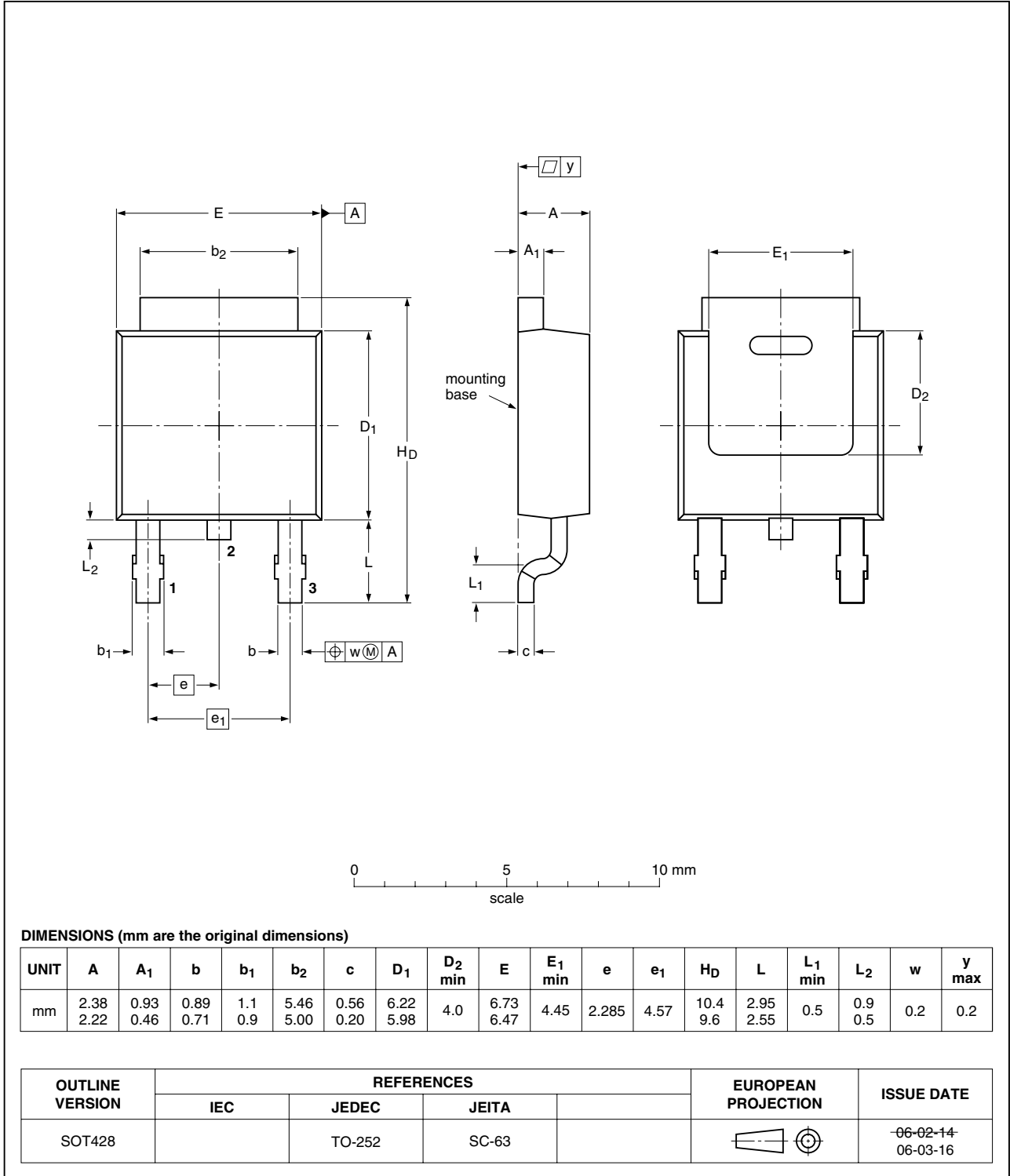


Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|--------------|---|---------------|-------------------------|
| PHD108NQ03LT_4 | 20090605 | Product data sheet | - | PHB_PHD_PHU108NQ03LT_3 |
| Modifications: | | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Type number PHD108NQ03LT separated from data sheet PHB_PHD_PHU108NQ03LT_3. | | |
| PHB_PHD_PHU108NQ03LT_3 (9397 750 14707) | 20050418 | Product data sheet | 2004070095 | PHP_PHB_PHD108NQ03LT-02 |
| PHP_PHB_PHD108NQ03LT-02 (9397 750 10159) | 20020911 | Product data | - | PHP_PHB_PHD108NQ03LT-01 |
| PHP_PHB_PHD108NQ03LT-01 (9397 750 09065) | 20011218 | Product data | - | - |

9. Legal information

9.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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