

IRFD310, IRFD311, IRFD312, IRFD313

0.3A and 0.4A, 350V and 400V, 3.6 and 5.0 Ohm,
N-Channel Power MOSFETs

January 1998

Features

- 0.3A and 0.4A, 350V and 400V
- $r_{DS(ON)} = 3.6\Omega$ and 5.0Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFD310	HEXDIP	IRFD310
IRFD311	HEXDIP	IRFD311
IRFD312	HEXDIP	IRFD312
IRFD313	HEXDIP	IRFD313

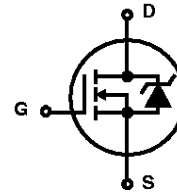
NOTE: When ordering, use the entire part number.

Description

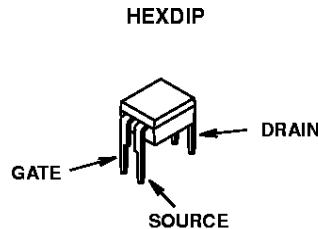
These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17444.

Symbol



Packaging



IRFD310, IRFD311, IRFD312, IRFD313

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFD310	IRFD311	IRFD312	IRFD313	UNITS
Drain to Source Voltage (Note 1) V_{DS}	400	350	400	350	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1) V_{DGR}	400	350	400	350	V
Continuous Drain Current I_D	0.4	0.4	0.3	0.3	A
Pulsed Drain Current (Note 3) I_{DM}	1.6	1.6	1.2	1.2	A
Gate to Source Voltage V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor	0.008	0.008	0.008	0.008	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4) E_{AS}	45	45	45	45	mJ
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s T_L	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 T_{pk}	260	260	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

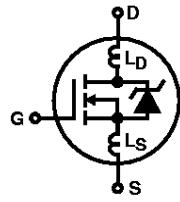
- $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

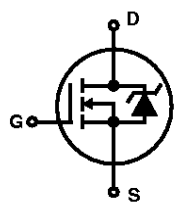
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS		
Drain to Source Breakdown Voltage IRFD310, IRFD312	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$, (Figure 9)	400	-	-	V		
			IRFD311, IRFD313	350	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA		
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	250	μA		
On-State Drain Current (Note 2) IRFD310, IRFD311	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$	0.4	-	-	A		
			IRFD312, IRFD313	0.3	-	-	A	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA		
Drain to Source On Resistance (Note 2) IRFD310, IRFD311	$r_{DS(ON)}$	$I_D = 0.2\text{A}, V_{GS} = 10\text{V}$, (Figures 7, 8)	-	3.3	3.6	Ω		
			IRFD312, IRFD313	-	3.6	5.0	Ω	
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, I_D = 0.2\text{A}$	0.5	1.2	-	S		
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 \times \text{Rated } BV_{DSS}, I_D \approx 0.4\text{A}, R_G = 9.1\Omega, V_{GS} = 10\text{V}$ (Figures 16, 17) $R_L = 495\Omega$ for $V_{DSS} = 200\text{V}$ $R_L = 433\Omega$ for $V_{DSS} = 175\text{V}$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	3.0	10	ns		
Rise Time	t_r		-	10	20	ns		
Turn-Off Delay Time	$t_{d(OFF)}$		-	5.0	10	ns		
Fall Time	t_f		-	8.0	15	ns		
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_g(\text{TOT})$	$V_{GS} = 10\text{V}, I_D = 0.4\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{G(\text{REF})} = 1.5\text{mA}$, (Figures 13, 18, 19) Gate Charge is Essentially Independent of Operating Temperature	-	6.0	7.5	nC		
			Gate to Source Charge	Q_{gs}	-	3.0	-	nC
			Gate to Drain "Miller" Charge	Q_{gd}	-	3.0	-	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$, (Figure 10)	-	135	-	pF		
Output Capacitance	C_{OSS}		-	35	-	pF		
Reverse Transfer Capacitance	C_{RSS}		-	8.0	-	pF		

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Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	L_D	Measured From Drain Lead, 2.0mm (0.08in) From Package to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 2.0mm (0.08in) from Package to Source Bonding Pad		-	6.0	-	nH
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	120	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 		-	-	0.4	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	1.6	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 1.6\text{A}$, $V_{GS} = 0\text{V}$, (Figure 12)		-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = 150^\circ\text{C}$, $I_{SD} = 1.6\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	380	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^\circ\text{C}$, $I_{SD} = 1.6\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	2.7	-	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by maximum junction temperature.
- $V_{DD} = 40\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 44.89\text{mH}$, $R_G = 50\Omega$, peak $I_{AS} = 1.4\text{A}$. (Figures 14, 15).

Typical Performance Curves Unless Otherwise Specified

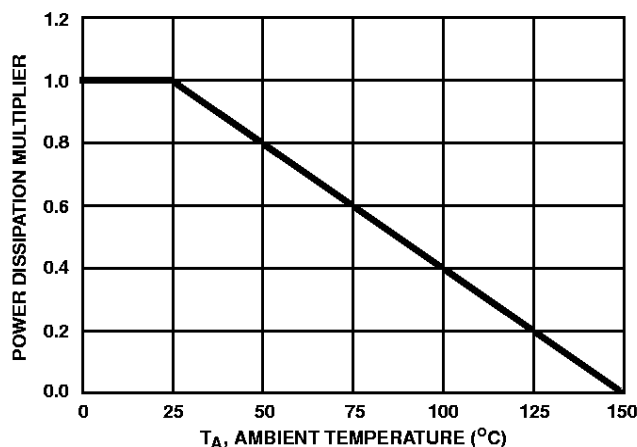


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

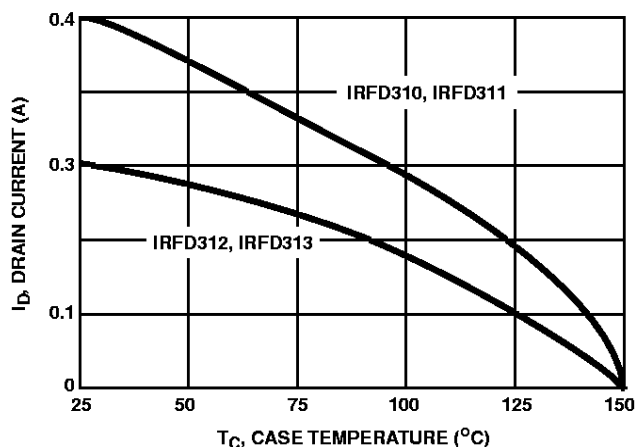


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

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Typical Performance Curves Unless Otherwise Specified (Continued)

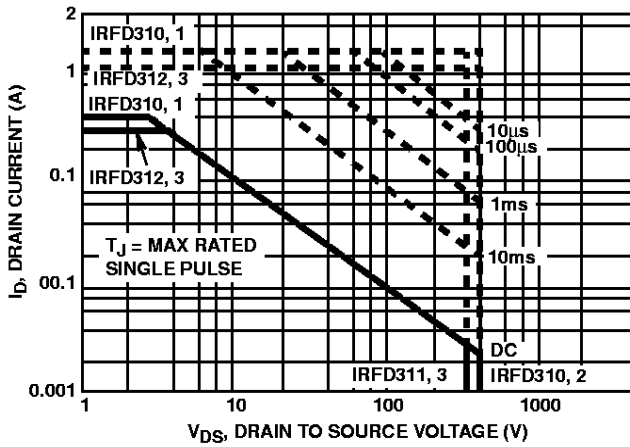


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

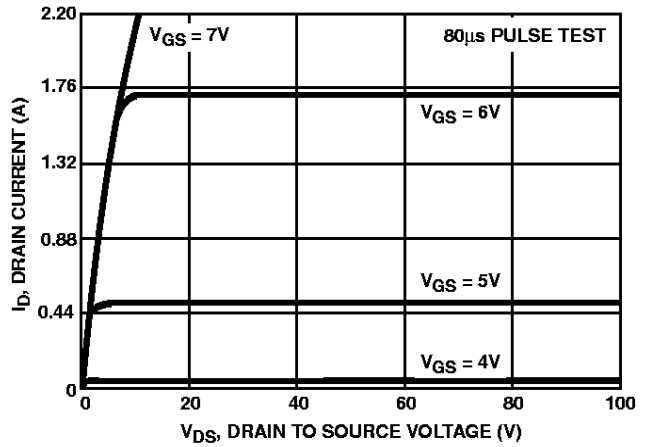


FIGURE 4. OUTPUT CHARACTERISTICS

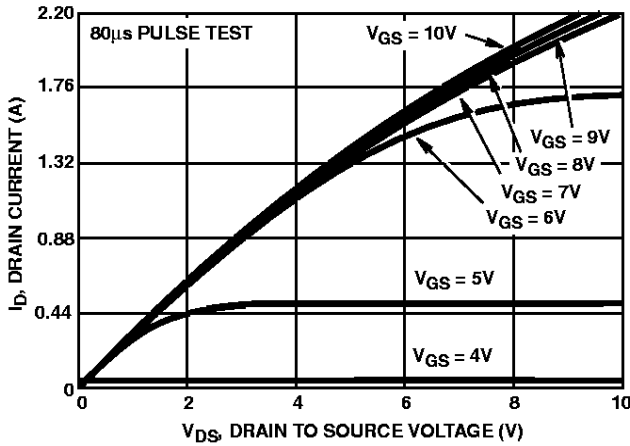


FIGURE 5. SATURATION CHARACTERISTICS

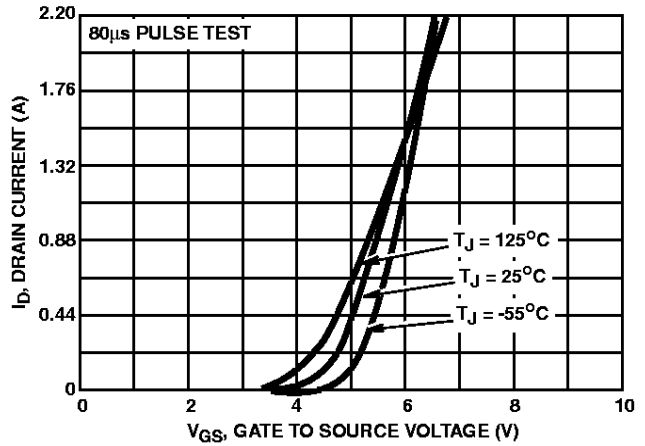


FIGURE 6. TRANSFER CHARACTERISTICS

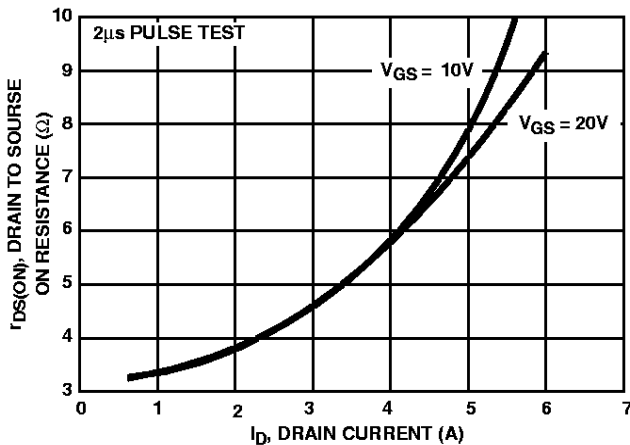


FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

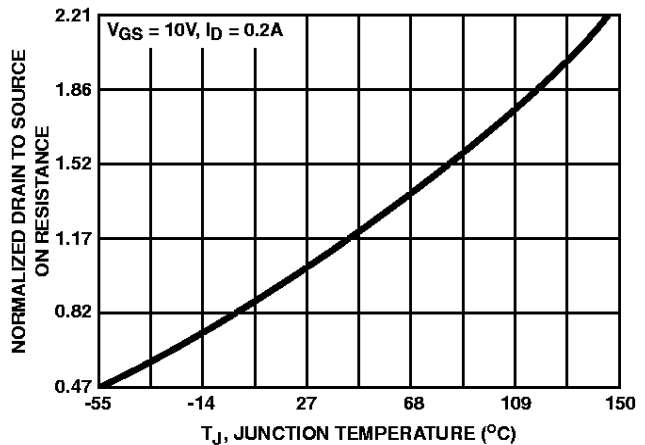


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

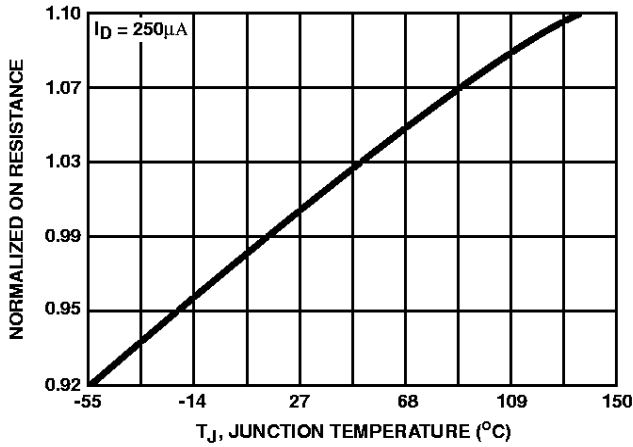


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

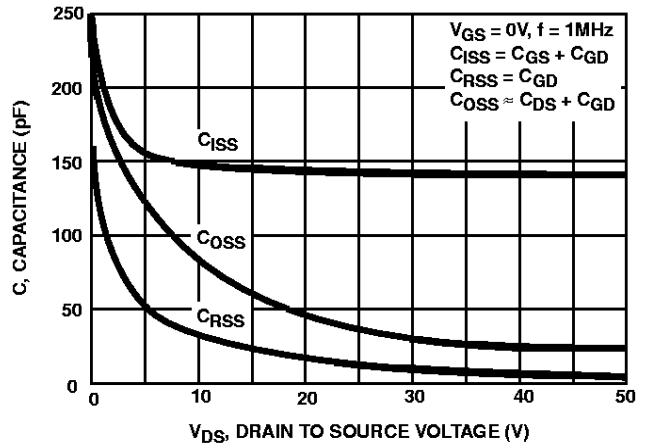


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

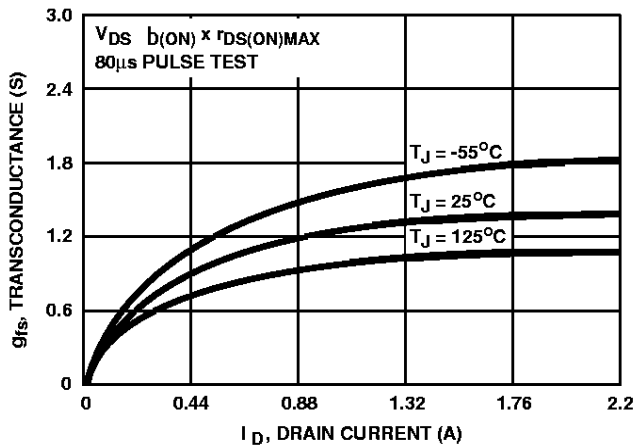


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

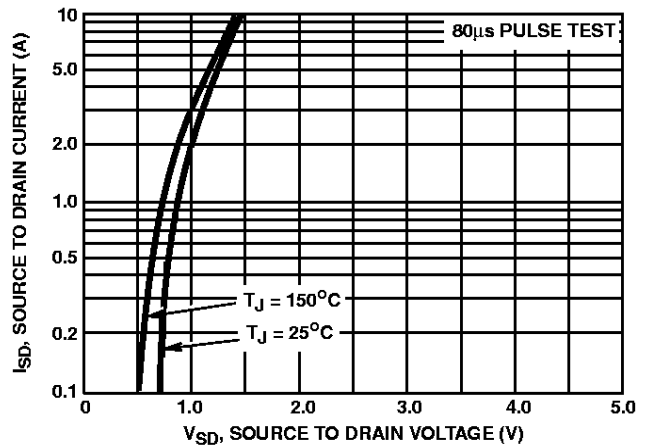


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

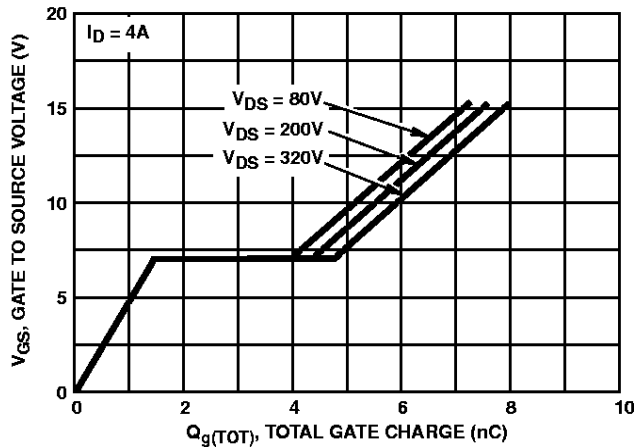


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

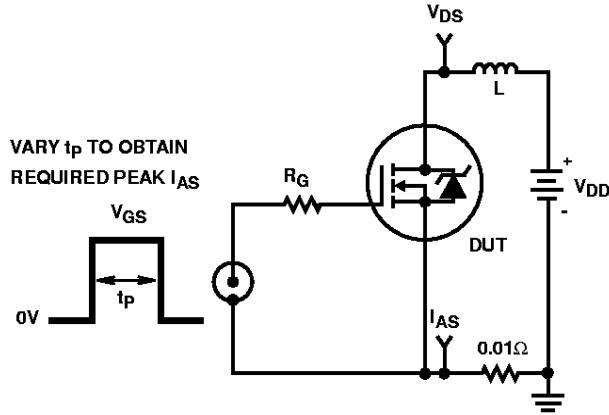


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

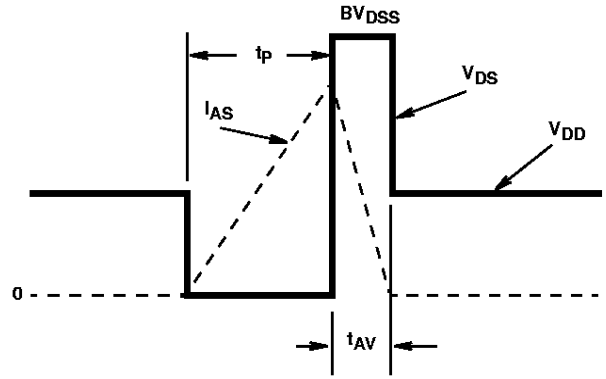


FIGURE 15. UNCLAMPED ENERGY WAVEFORM

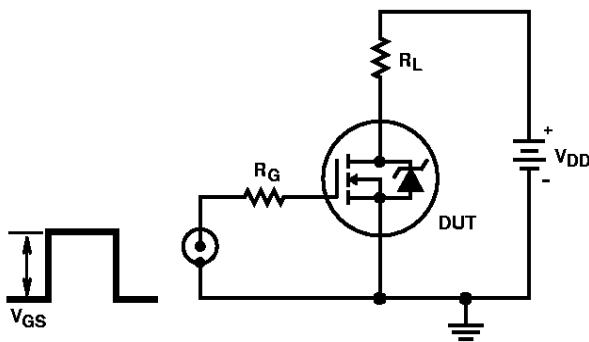


FIGURE 16. SWITCHING TIME TEST CIRCUIT

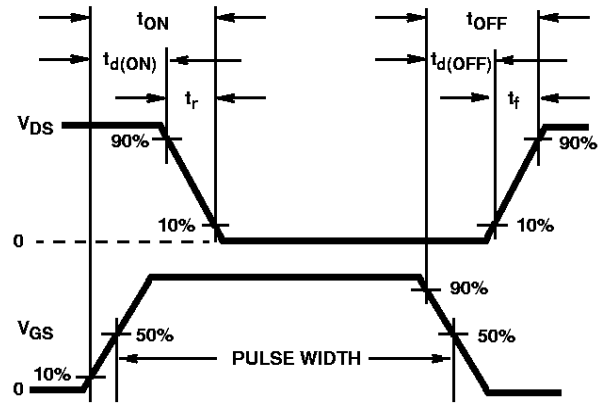


FIGURE 17. GATE CHARGE TEST CIRCUIT

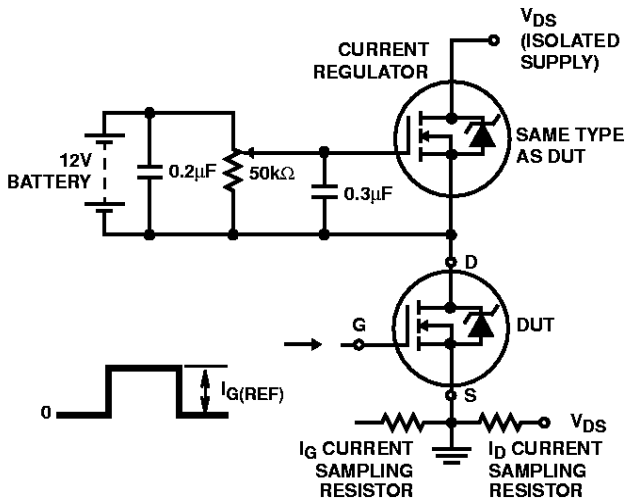


FIGURE 18. GATE CHARGE TEST CIRCUIT

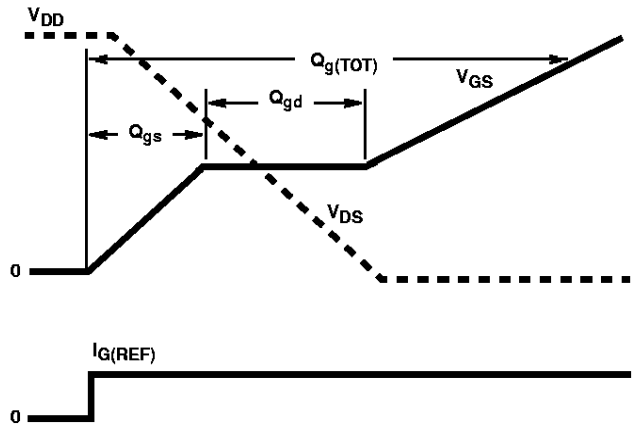


FIGURE 19. GATE CHARGE WAVEFORMS