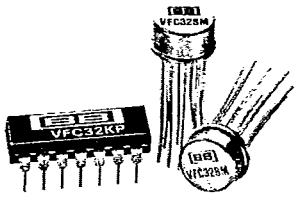
T-73-13-03

BURR-BROWN®



VFC32

MILITARY & DIE VERSIONS AVAILABLE

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- RELIABLE MONOLITHIC CONSTRUCTION
- HIGH LINEARITY:
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F or F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- VOLTAGE OR CURRENT INPUT
- OUTPUT TTL/CMOS COMPATIBLE

APPLICATIONS

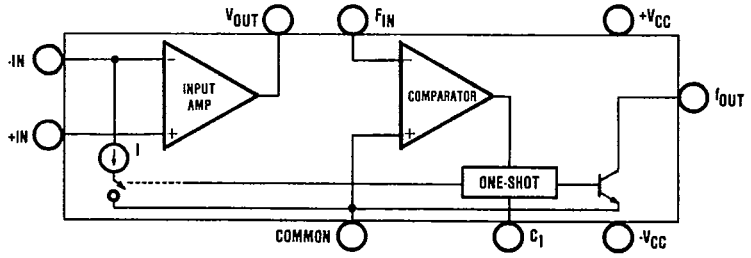
- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. Full scale frequency and input voltage are determined by one resistor (in series with —IN) and two capacitors (one-shot timing and input amplifier integration). High linearity is achieved with relatively few external components, e.g., ±0.01% at 10kHz. The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$).

The VFC32 is available in three models and two package configurations. The TO-100 versions are hermetically sealed, and specified for the −25°C to +85°C and −55°C to +125°C ranges. The plastic DIP and SOIC are specified from 0°C to +70°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-372E

T-73-13-03

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC32KP, KU MIN	VFC32KP, KU TYP	VFC32KP, KU MAX	VFC32BM MIN	VFC32BM TYP	VFC32BM MAX	VFC32SM MIN	VFC32SM TYP	VFC32SM MAX	UNITS
INPUT (V/F CONVERTER)	$F_{OUT} = V_{IN} / 7.5\ R_1C_1$, Figure 6										
Voltage Range[1]											
Positive Input		>0		+0.25mA x R_1	•		•	•		•	V
Negative Input		>0		-10	•		•	•		•	V
Current Range[1]		>0		+0.25	•		•	•		•	mA
Bias Current											
Inverting Input			20	100		•	•		•	•	nA
Noninverting Input			100	250		•	•		•	•	nA
Offset Voltage[2]			1	4		•	•		•	•	mV
Differential Impedance		300 || 10	650 ||10		•	•		•		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		•	•		•		MΩ || pF
INPUT (F/V CONVERTER)	$V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9										
Impedance		50 || 10	150 || 10		•	•		•	•		kΩ || pF
Logic "1"			+1.0		•		•	•		•	V
Logic "0"			−0.05		•		•	•		•	V
Pulse-width Range		0.1		150k/F_{MAX}	•		•	•		•	µsec
ACCURACY											
Linearity Error[3]	0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010[4]		•	•		•	•	% of FSR[5]
	0.1Hz ≤ oper freq ≤ 100kHz		±0.025	±0.05		•	•		•	•	% of FSR
	0.5Hz ≤ oper freq ≤ 500kHz		±0.05			•			•		% of FSR
Offset Error Input											
Offset Voltage[2]			1	4		•	•		•	•	mV
Offset Drift[6]			±3			•			•		ppm of FSR/°C
Gain Error[2]			5			•	•		•	•	% of FSR
Gain Drift[6]	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift offset drift & gain drift [6][7]	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			•			•	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	•	•	•	•	•	•	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		•	•		•	•	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4			V_{PU}			•			•	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			•	•		•	•	sec
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			•			•	nsec
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	I_O ≤ 7mA	0 to +10			•			•			V
Current	V_O ≤ 7VDC	+10			•			•			mA
Impedance	Closed loop			1			•			•	Ω
Capacitive Load	Without oscillation			100			•			•	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500[8]	•			•			kHz
Dynamic Range		6			•			•			decades
Settling Time	V/F to specified linearity for a full scale input step		[9]			•			•		
Overload Recovery	< 50% overload		[9]			•			•		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					•		V
Quiescent Current			±5.5	±6.0		•	•		•		mA
TEMPERATURE RANGE											
Specification		0		+70	-25		+85	-55		+125	°C
Operating		-25		+85	-55		+125	-55		+125	°C
Storage		-25		+85	-65		+150	-65		+150	°C

*Specification the same as VFC32KP

T-73-13-03

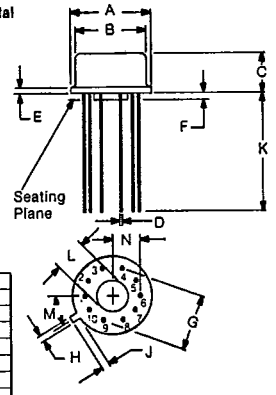
NOTES:
1. A 25% duty cycle ·0.25mA input current· is recommended where possible to achieve best linearity.
2. Adjustable to zero. See Offset and Gain Adjustment section.
3. Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C.
4. ±0.015% of FSR for negative inputs shown in Figure 7. Positive inputs are shown in Figure 6.
5. FSR = Full Scale Range ·corresponds to full scale frequency and full scale input voltage .
6. Exclusive of external components' drift.
7. Positive drift is defined to be increasing frequency with increasing temperature.
8. For operation above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections.
9. One pulse of new frequency plus 1µsec.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, -Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range:	
VFC32BM, SM	-65°C to +150°C
VFC32KP, KU	-25°C to +85°C

MECHANICAL

VFC8M, VFC32SM-TO-100 Metal

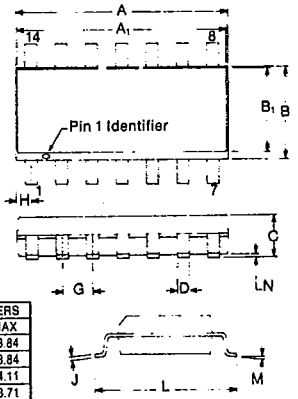


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

VFC32KU - Plastic SOIC

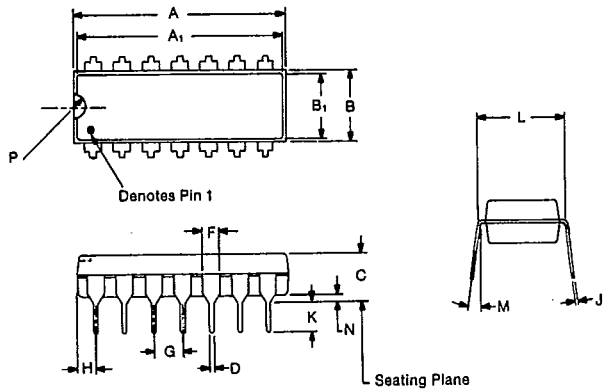


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.332	.348	8.44	8.84
A_1	.325	.348	8.26	8.84
B	.146	.162	3.71	4.11
B_1	.128	.146	3.25	3.71
C	.052	.068	1.32	1.73
D	.014	.019	0.36	0.48
G	.050 BASIC		1.27 BASIC	
H	.016	.024	0.41	0.61
J	.008	.012	0.20	0.30
L	.226	.246	5.74	6.25
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

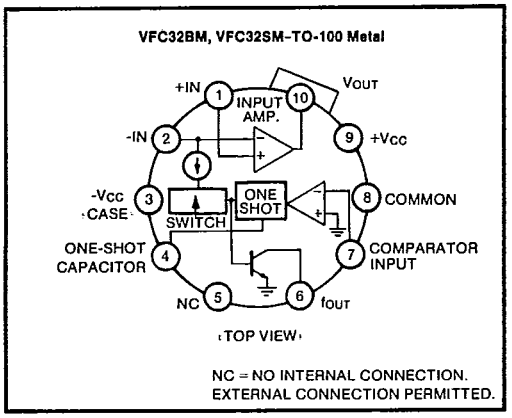
VFC32KP-Plastic DIP

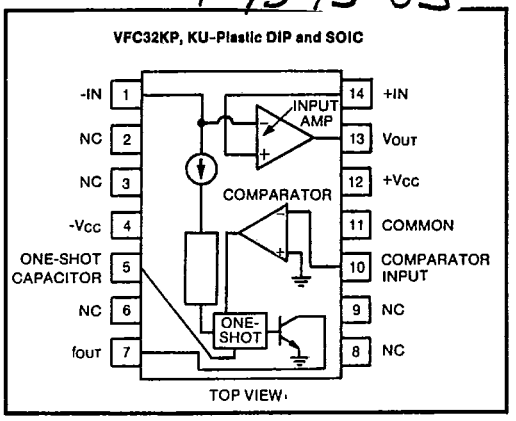
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.700	.800	17.78	20.32
A_1	.685	.785	17.40	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.050	.100	1.27	2.54
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

PIN CONFIGURATIONS





DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (90% of full scale input or frequency and 0.1% of full scale called zero). Linearity is the true measure of voltage-to-frequency converter's performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. For a given full scale frequency, the linearity error decreases with decreasing operating frequency as shown in Figure 2. Also, best linearity is achieved at lower gains ($\Delta F_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC32 makes the device an excellent choice for use as the front end of A/D converters with 8- to 12-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire serial data transmission).

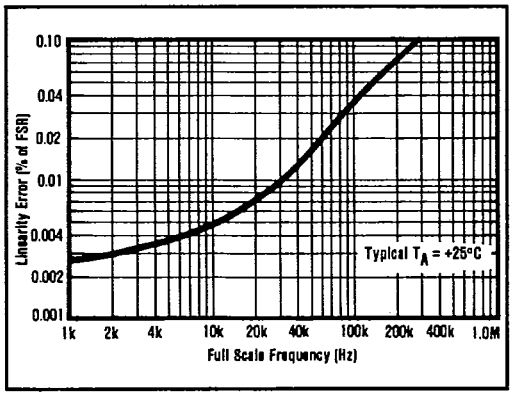


FIGURE 1. Linearity Error vs Full Scale Frequency. (25% Duty Cycle)

FREQUENCY STABILITY vs TEMPERATURE

The full scale frequency drift of the VFC32 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 100kHz, and this should be taken into account for

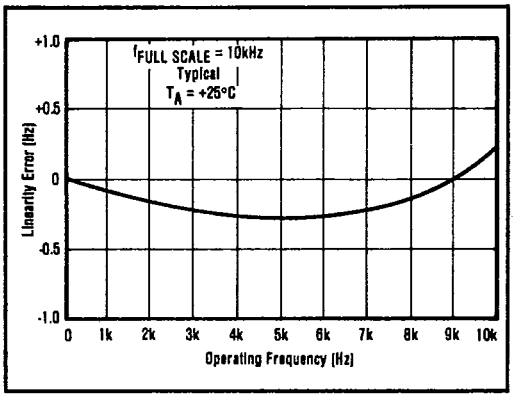


FIGURE 2. Linearity Error vs Operating Frequency. (25% Duty Cycle)

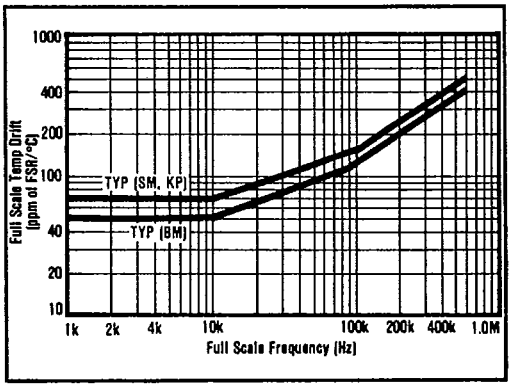


FIGURE 3. Full Scale Drift vs Full Scale Frequency. (25% Duty Cycle)

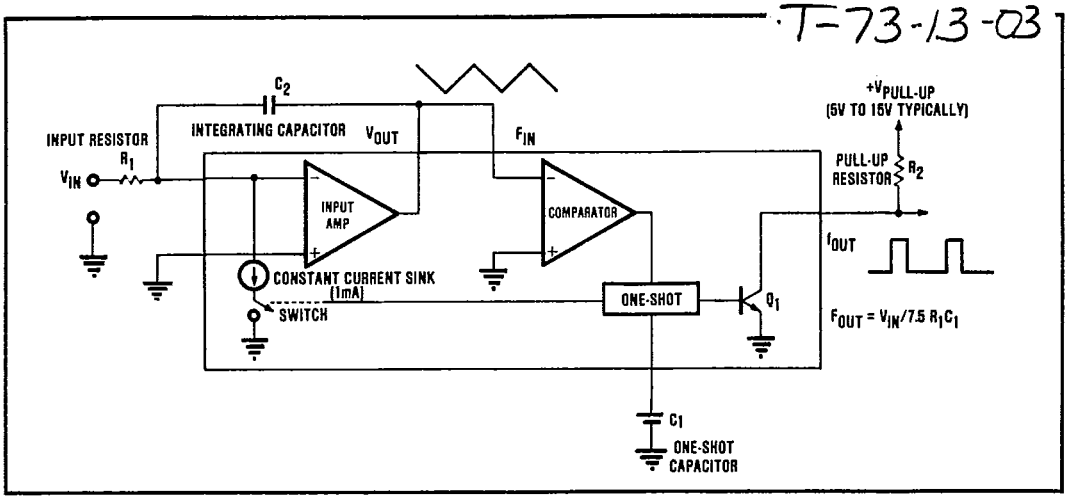


FIGURE 4. Functional Block Diagram of the VFC32.

specific applications. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC32. Above 200kHz, it is recommended all grades be operated below +85°C. Higher duty cycle (up to 50%) and higher output transistor collector current (up to 15mA) will be required. Linearity will, however, be degraded.

RESPONSE

Response of the VFC32 to changes in input signal level is specified for a full scale step, and is 1 microsecond plus 1 pulse of the new frequency. For a 10 volt input signal step with the VFC32 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 11 microseconds.

THEORY OF OPERATION

The VFC32 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage in Figure 4.

Essentially, the input amplifier acts as an integrator that produces a 2-part ramp. The first part is a function of the input voltage, and the second part dependent on the current sink. When a positive input voltage is applied at V_{IN}, a constant current will flow through the input resistor, causing the voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time, the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and integrating components. When the ramp reaches a voltage close to zero, the comparator will cause the one-shot to fire. The one-shot period is determined by an internal 7.5V reference and C_1. The f_{OUT} signal will then change logic states, going from a "0" to a "1", and the switch will close, enabling the constant current sink. The ramp voltage will then change direction and begin to ramp up. Since V_{IN} R_1 is always set up to be less than 1mA, the current in the integrating capacitor will flow toward the summing junction, and the ramp voltage rate of change will be;

$$\frac{dV}{dt} = \frac{\frac{V_{IN}}{R_1} - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot will reset, disabling the current sink, changing the output state back to logic "0", and restarting the cycle. Since the integrating capacitor C_2 affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to V_{IN}/R_1, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

To operate the VFC32 as a highly linear frequency-to-voltage converter, open the connection between V_{OUT} and f_{IN}, and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}, and a positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. For details see Installation and Operating Instructions.

The total VFC period is determined by the following equations, which is shown graphically in Figure 5.

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2 \text{ and } i = c\,dv/dt$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1) - 1mA}$$

T-73-13-03

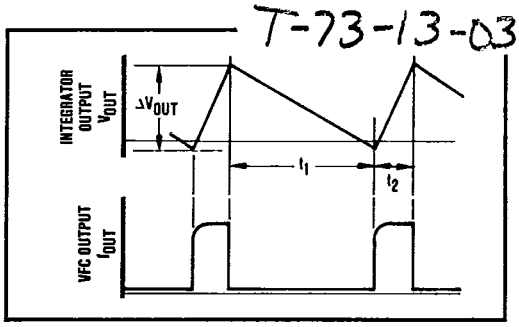


FIGURE 5. Integrator and VFC Output Timing.

and:

$$-\Delta V_{OUT} t_1 = +\Delta V_{OUT} t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5(R_1)\,C_1}$$

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which gives the full scale output frequency, F_{FS}.

$$D = \frac{t_2}{t_1 + t_2} = PW \times F_{FS}$$

$$PW = \frac{D}{F_{FS}}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\ max/(R_1)}{1mA} = \frac{I_{IN}\ max}{1mA}$$

A 25% duty cycle or less is recommended to achieve the best linearity. This corresponds to a maximum input current of 0.25mA. However, for frequencies above 200kHz a higher duty cycle (up to 50%) will provide more stable high temperature operation at a sacrifice in linearity.

In general, designs with the VFC32 include: (1) Choosing F_{MAX}, (2) Choosing the duty cycle (D = 0.25 typically), (3) Determining the one-shot PW, and (4) Calculating C_1, C_2, R_1, R_2, and R_3.

INSTALLATION AND OPERATING INSTRUCTIONS

The VFC32 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

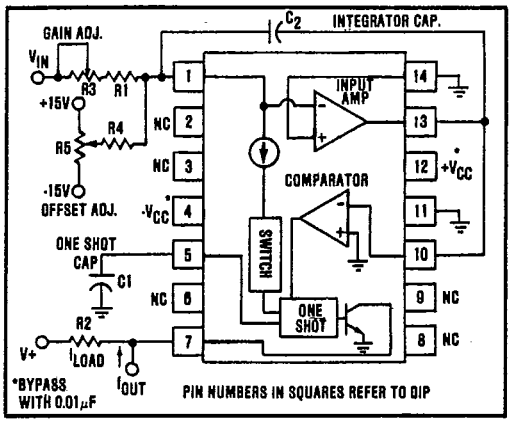


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

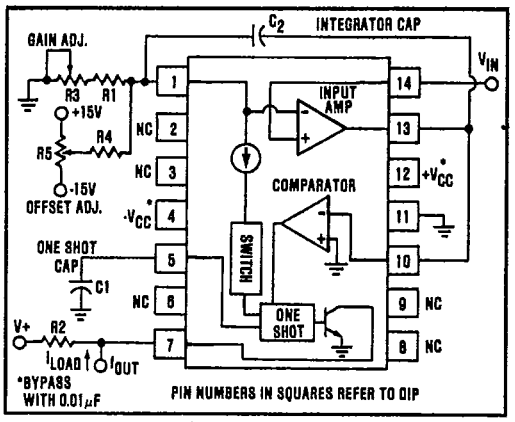


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

Differential inputs are also possible (in Figure 7 lift ground on R_3 and drive R_3 and pin 14 differentially). Note, no CMR will be present.

The full scale frequency and full scale input voltage (current) are established by the selection of values for R1, C2, and C1. Most applications will require a gain adjustment pot (R3), but the offset adjust network (R4, R5) can be omitted if input offset voltages of 1mV to 4mV can be tolerated. R2 is an output pull up resistor and its value depends on the pull up voltage and output drive requirements.

EXTERNAL COMPONENT SELECTION CRITERIA

One-shot Capacitor, C1. This capacitor determines the duration of the output pulse, and is a function of the full scale frequency, according to this equation:

$$C1(pF) = 33 \times 10^6 / f_{MAX} - 30$$

Above 425kHz use 47pF

Select the closest standard value to the capacitance given by the equation. The initial tolerance of this capacitor is

T-73-13-03

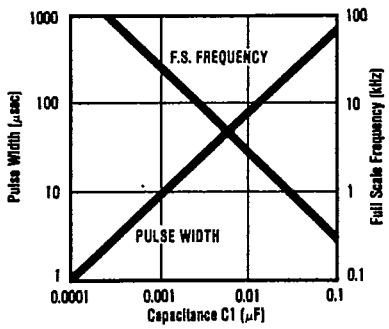


FIGURE 8. Output Pulse Width (D = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

not critical since R3 will be adjusted to remove initial gain errors. The temperature drift is critical, since it will add directly to the errors in the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize the parasitic capacitance at this connection to the VFC32 and C1 should be mounted as close as possible. Figure 8 shows pulse width and FS frequency for various values of C1.

Input Resistor R1 and R3. R1 and R3 determine the magnitude of the current which charges the integrator capacitor. It is a function of the full scale input voltage, according to this equation for 25% duty cycle.

$$R1\ (k\Omega)\ [90\% - \%\ \text{tolerance C1}]\ \times V_{IN}\ \text{max}/0.25mA$$

R1 is scaled down by [1-(initial C1 tolerance + 0.1)] to allow the addition of a series gain adjusting pot, R3.

$$R_3\ (k\Omega) = V_{IN}\ \text{max}/0.25mA - R_1$$

R1 should have a very low temperature coefficient since this drift adds directly to the errors in the transfer function. If the input signal is a current rather than a voltage, R1 and R3 should be replaced with a short circuit, and the full scale input current should be 0.25mA (25% duty cycle). Removal of gain error then requires adjustment of C1.

Integrating Capacitor C2. C2 is a function of the full scale frequency, according to this equation:

$$C_2(\mu F) = 10^2/f_{MAX}\ \text{below 100kHz}$$
$$0.001\mu F\ \text{min above 100kHz}$$

Select the closest standard value to the capacitance given by the equation. The initial tolerance and temperature stability are not critical since these errors do no affect the transfer function. Since the leakage current of the capacitor introduces a gain error, select a capacitor with leakage that is small compared to the full scale input current e.g., 0.25mA. A mylar type is recommended.

Output Pull Up Resistor R2. The open collector output can sink up to 8mA and still be TTL-compatible. Select R2 according to this equation:

$$R_2\ \text{min}\ (\Omega) = V_{PULLUP}/(8mA - i_{LOAD})$$

A 10% carbon composition resistor is suitable for use as R2.

Operation above 200kHz up to 500kHz requires higher duty cycles up to 50% (I_{IN} = 0.5mA) and a pull-up resistor that permits 15mA to flow in the output transistor. At this speed, capacitive loading should be minimized to 100pF or less to allow the output voltage time to rise to logic one. Due to the large collector current, the logic zero may rise above +0.4V. This may require an interface circuit such as diode clamp or voltage comparator for coupling to TTL inputs. Note, that linearity will degrade. Also, it is recommended to stay below +85°C at high frequencies.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC32 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses -0.6V. Choose C3 for appropriate value of t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the -0.6V threshold. Errors are nulled following the procedure given on this page, using 0.001X full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC32 is 0.015% of FSR/% max. To maintain ±0.015% conversion,

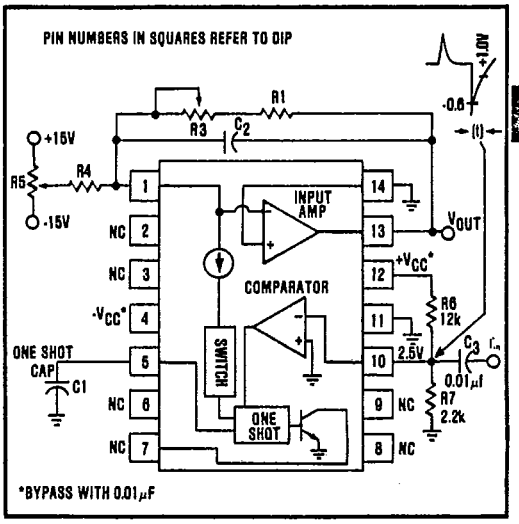


FIGURE 9. Connection Diagram for F/V Conversion.

T-73-13-03

power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Current in the f_{OUT} pin (logic sink current) flows in the common connection (pin 11 of DIP package). It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by logic current flowing through any ground return impedance.

Trimming Components R3, R4, R5.

R5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm °C. R4 can be a 20% carbon composition resistor with a value of 10MΩ.

R3 nulls the gain errors of the converter and compensates for initial tolerances of R1 and C1. Its total resistance should be at least 20% of R1, if R1 is selected 10% low (see R1 equation). Its temperature coefficient should be no greater than five times that of R1, to maintain a low drift of the R3 - R1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1

$C_1 = 33 \times 10^6 / f_{MAX} - 30$
$= 33 \times 10^6 / 100kHz - 30$
$= 300pF$

Choose a 300pF NPO ceramic capacitor with ±1% tolerance.

Selecting R_1 and R_3 (for D = 0.25; for D = 0.5 use 0.5mA)

$R_1 = [90\% - \%$ tolerance of $C_1] \times V_{IN}$ max / 0.25mA
$= [0.9 - 0.1] \times 10V/0.25mA$
$= 32k\Omega$

Choose a 32.4kΩ metal film resistor with ±1% tolerance.

$R_3 = 10V/0.25mA - R_1$
$= 8k\Omega$

Choose a 10kΩ cermet potentiometer

Selecting C_2

$C_2 = 10^2 / F_{MAX}$
$= 10^2 / 100kHz$
$= 0.001\mu F$

Choose a 0.001μF mylar capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP} / (8mA - i_{LOAD})$
$= 5V / (8mA - 1.6mA)$, one TTL-load = 1.6mA
$= 781\Omega$

Choose a 750Ω 1/4-watt carbon composition resistor with ±5% tolerance.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC32 ideal for a variety of VFC applications. High accuracy allows the VFC32 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 12-bits.

Figures 10 - 14 show typical applications of the VFC32.

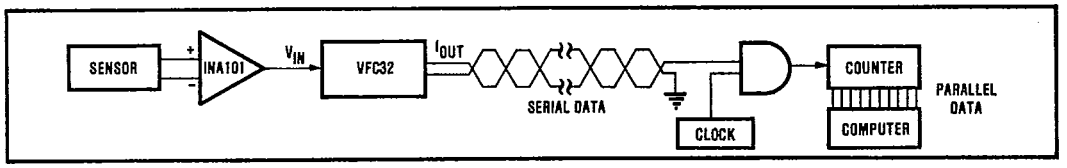


FIGURE 10. Inexpensive A/D with Serial Transmission of Digital Data.

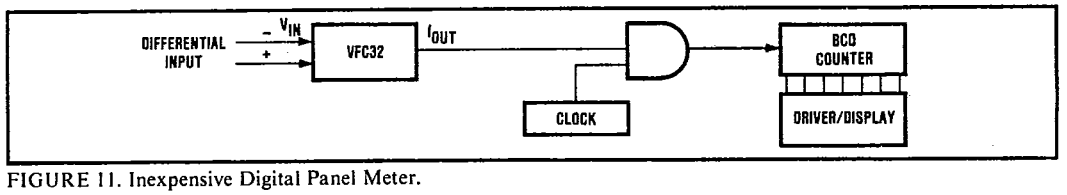


FIGURE 11. Inexpensive Digital Panel Meter.

T-73-13-03

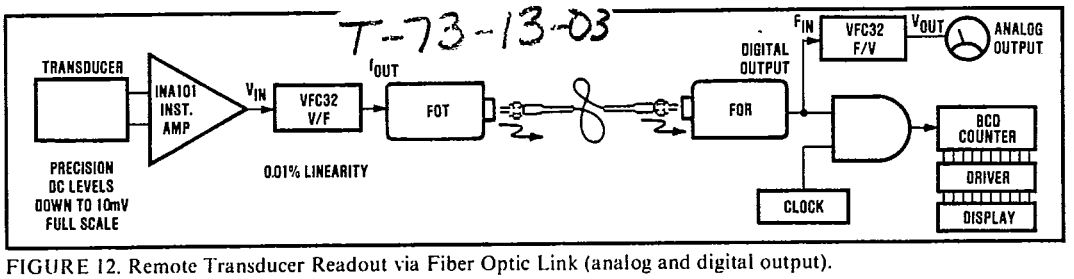


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

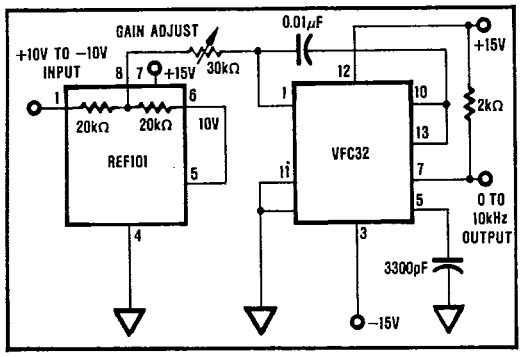


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

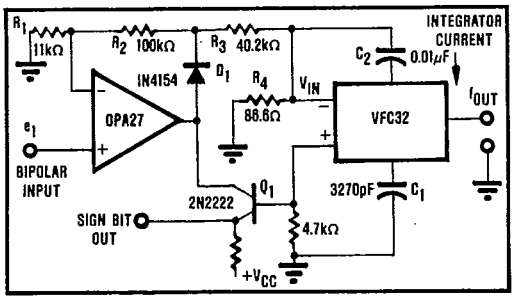


FIGURE 14. Absolute value circuit with the VFC32. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.