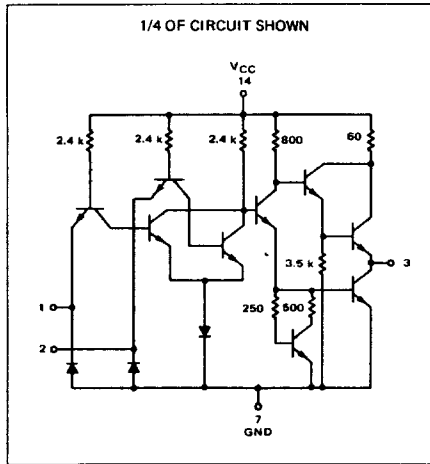


QUAD 2-INPUT "OR" GATE

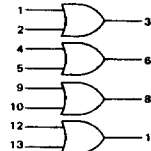
MTTL III MC3100/3000 series

MC3103F • MC3003F
MC3103L • MC3003L_P

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

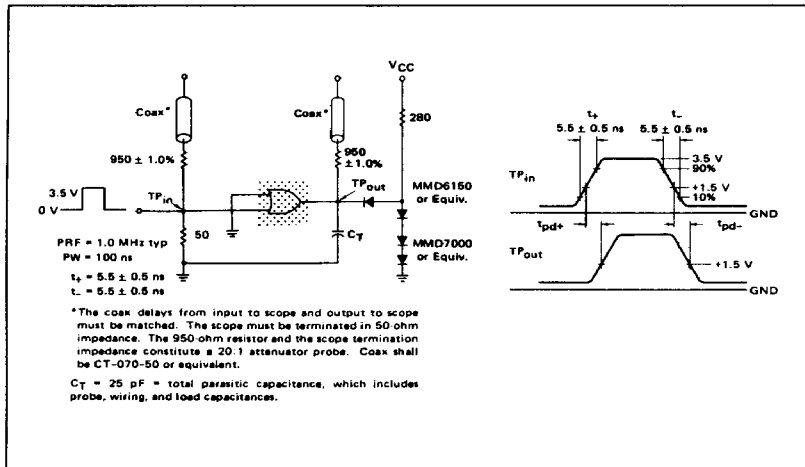


Positive Logic: $3 = 1 + 2$
Negative Logic: $3 = 1 - 2$

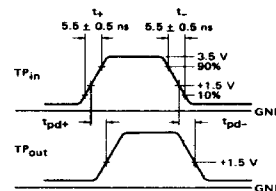
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



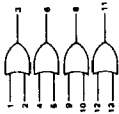
VOLTAGE WAVEFORMS AND DEFINITIONS



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



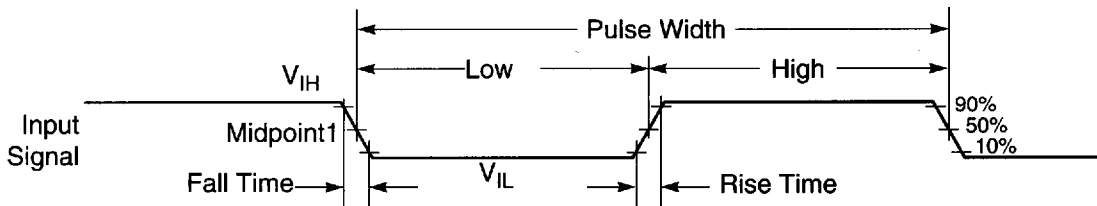
Characteristic	Symbol	MC3103 Test Limits			MC3003 Test Limits			TEST CURRENT/VOLTAGE VALUES																		
		-55°C		+25°C	+125°C	0°C		+25°C	+75°C	mA		Volts												Gnd		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	I_{CC}	I_{OH}	I_{OL}	I_{in}	I_{b}	V_{in}	V_{b}	V_{F}	V_{M}	V_{OH}	V_{OL}	V_{CC}		V_{ECN}	
Input																										
Forward Current	I_F	1	-2.0	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Leakage Current	I_L	1	50	50	-	50	-	50	-	50	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Breakdown Voltage	V_{B1}	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Clamp Voltage	V_D	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Output																										
Output Voltage	V_{OH}	3	0.4	0.4	-	0.4	-	0.4	-	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	V_{OL}	3	2.4	2.4	-	2.4	-	2.5	-	2.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	V_{OC}	3	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100	-4.0	-100
Short-Circuit Current	I_{SC}	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Power Requirements																										
Maximum (Total Device)	I_{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Maximum Supply Current	I_{FDD}	14	-	32	-	32	-	32	-	32	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Power Supply Drain	I_{PDL}	14	-	55	-	55	-	55	-	55	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Switching Parameters																										
Turn-On Delay	t_{pd}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Turn-Off Delay	t_{pd}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Notes: 1. In non-driving gate, power drain is minimized by tying the inputs to GND not under test to V_{CC} .

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AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference