Si3441DV

FAIRCHILD

P-Channel 2.5V Specified PowerTrench[®] MOSFET

General Description

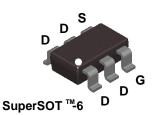
This P-Channel 2.5V specified MOSFET uses Fairchild's low voltage PowerTrench process. It has been optimized for battery power management applications.

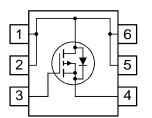
Applications

- Battery management
- · Load switch
- Battery protection

Features

- -3.5 A, -20 V. $R_{DS(ON)} = 80 \ m\Omega \ @ V_{GS} = -4.5 \ V$ $R_{DS(ON)} = 110 \ m\Omega \ @ V_{GS} = -2.5 \ V$
- Low gate charge
- High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$





Absolute Maximum Ratings T_{A=25°C} unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±8	V
I _D	Drain Current – Continuous	(Note 1a)	-3.5	A
	– Pulsed		-20	
P _D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

ReJA Thermal Resistance, Junction-to-Ambient (Note 1a) 78 °C/W ReJC Thermal Resistance, Junction-to-Case (Note 1) 30 °C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.441	Si3441DV	7"	8mm	3000 units

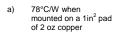
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Si3441DV

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = -250 \mu\text{A}$	-20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$, Referenced to 25°C		-12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -8 V$ $V_{DS} = 0 V$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	-0.4	-0.8	-1.5	V
$rac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$, Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{l} V_{GS}=-4.5 \ V, I_{D}=-3.5 \ A \\ V_{GS}=-2.5 \ V, I_{D}=-3.1 \ A \\ V_{GS}=-4.5 \ V, \ I_{D}=-3.5 A, T_{J}{=}125^{\circ}C \end{array} $		60 82 77	80 110 112	mΩ
I _{D(on)}	On–State Drain Current	$V_{\text{GS}} = -4.5 \text{ V}, \qquad V_{\text{DS}} = -5 \text{ V}$	-10			А
g fs	Forward Transconductance	$V_{\text{DS}} = -5 \text{ V}, \qquad I_{\text{D}} = -3.5 \text{ A}$		11		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = -10 V$, $V_{GS} = 0 V$,		779		pF
Coss	Output Capacitance	f = 1.0 MHz		121		pF
C _{rss}	Reverse Transfer Capacitance			56		pF
Switchir	g Characteristics (Note 2)					
t _{d(on)}	Turn–On Delay Time	$V_{DD} = -10 V$, $I_D = -1 A$,		10	20	ns
t _r	Turn–On Rise Time	$V_{GS} = -4.5 \text{ V}, \qquad R_{GEN} = 6 \Omega$		9	19	ns
t _{d(off)}	Turn–Off Delay Time			27	43	ns
t _f	Turn–Off Fall Time			11	20	ns
Q _g	Total Gate Charge	$V_{DS} = -10 V$, $I_D = -3.5 A$,		7.2	10	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 V$		1.7		nC
Q _{gd}	Gate-Drain Charge			1.5		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings			•	
l _s	Maximum Continuous Drain–Source Diode Forward Current –1.3 A			А		
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V$, $I_S = -1.3 A$ (Note 2)		-0.8	-1.2	V

1. $R_{\theta,JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta,JC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.





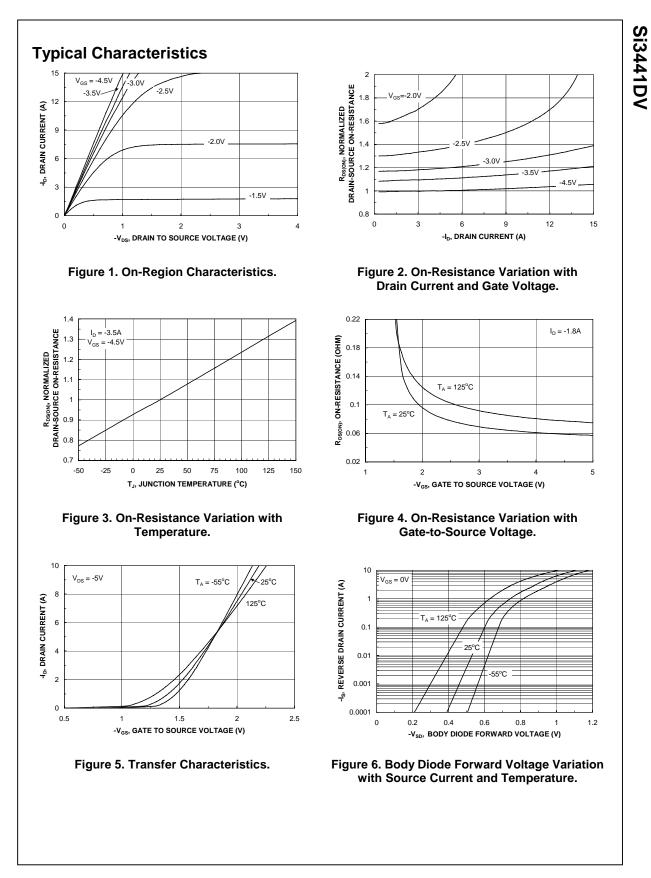


b) 156°C/W when mounted on a minimum pad of 2 oz copper

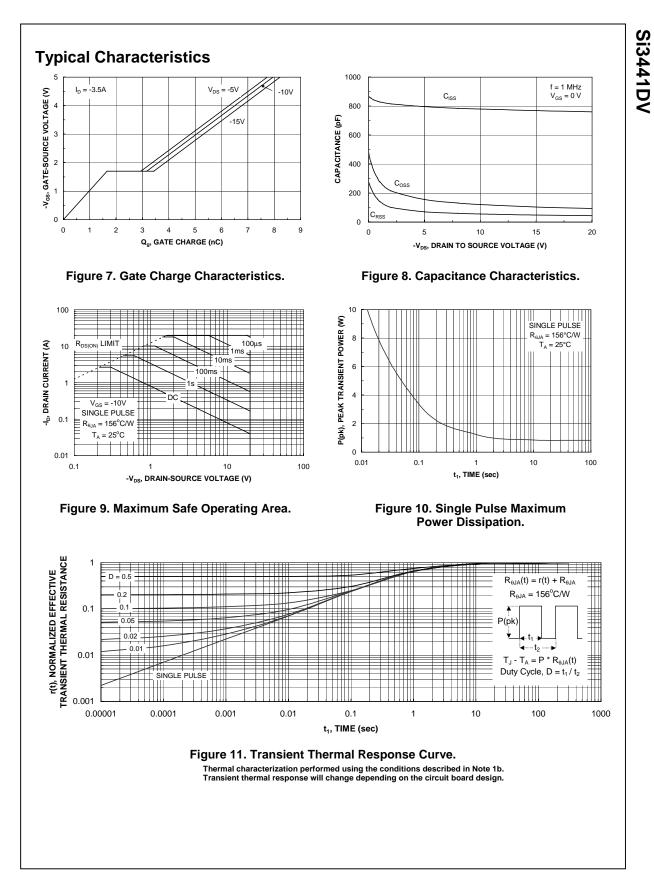
Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%

Si3441DV Rev A (W)



Si3441DV Rev A (W)



Si3441DV Rev A (W)

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