TEXAS INSTRUMENTS

GC1011A DIGITAL RECEIVER

1.0 FUNCTIONAL DESCRIPTION

Fabricated in 1 micron CMOS technology, the GC1011A chip is an all digital receiver which can extract narrow band signals from wide band digitized sources. At full rate operation (70 MHz input rate), the input bandwidth can be up to 35 MHz wide. Any signal within the input bandwidth can be down-converted to zero frequency, low pass filtered, and output at a reduced sample rate. The narrow band output can be formatted as either a complex data stream, or a real data stream. In the complex output mode the output sample rate ranges from $(1/64)^{th}$ to $(1/65{,}536)^{th}$ of the input rate in steps of (1/4N) where N is an integer ranging from 16 to 16,384. The output sample rate is doubled in the real output mode.

The user may select a standard output filter which has a passband covering 80% of the output bandwidth and has more than 70 dB of out-of-band rejection, or a wider, 90% passband filter which has 50 dB of out-of-band rejection.

The 28 bit accumulator in the chip's digital oscillator circuit provides a tuning accuracy equal to the input clock rate divided by 2^{28}. With a 60 MHz clock rate the tuning resolution is 0.2 Hz giving a tuning accuracy of +/- 0.1 Hz. The phase noise in the oscillator is low enough to provide a spur free dynamic range of over 75 dB. All arithmetic following the oscillator is performed to sufficient accuracy to provide over 90 dB of noise free dynamic range. This allows the chip to generate and preserve up to 20 dB of narrow band processing gain. The gain of the output signal can be adjusted in 6 dB steps.

The chip's output circuit allows the user to select a real or complex data output format, to select spectral inversion, or to offset the output spectrum by half of the output sample rate. The filtered signal is output in a bit-serial format. The user has control over the bit-serial format including its rate, its bit-strobe format and its frame-strobe format.

On chip diagnostics are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 4 bit address port, a read/$\overline{\text{write}}$ bit, and a control select strobe.

The GC1011A chip replaces the GC1011 chip. The new features include improved real output formatting and a symmetric rounding algorithm which removes unwanted DC rounding bias from the output.

1.1 KEY FEATURES

- 70 million samples per second input rate
- 0.1 Hz tuning resolution
- >70 dB dynamic range
- Programmable output bandwidth
- 12 bit inputs, 16 bit outputs
- Real or complex output formats
- Built in strobe/sync generator
- Microprocessor interface for control, output, and diagnostics
- Power down mode
- Built in diagnostics
- 750 mW power at 50 MHz, 5 volts
- 200 mW at 30 MHz, 3.3 volts
- Small, 44 pin Leaded chip carrier package

1.2 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

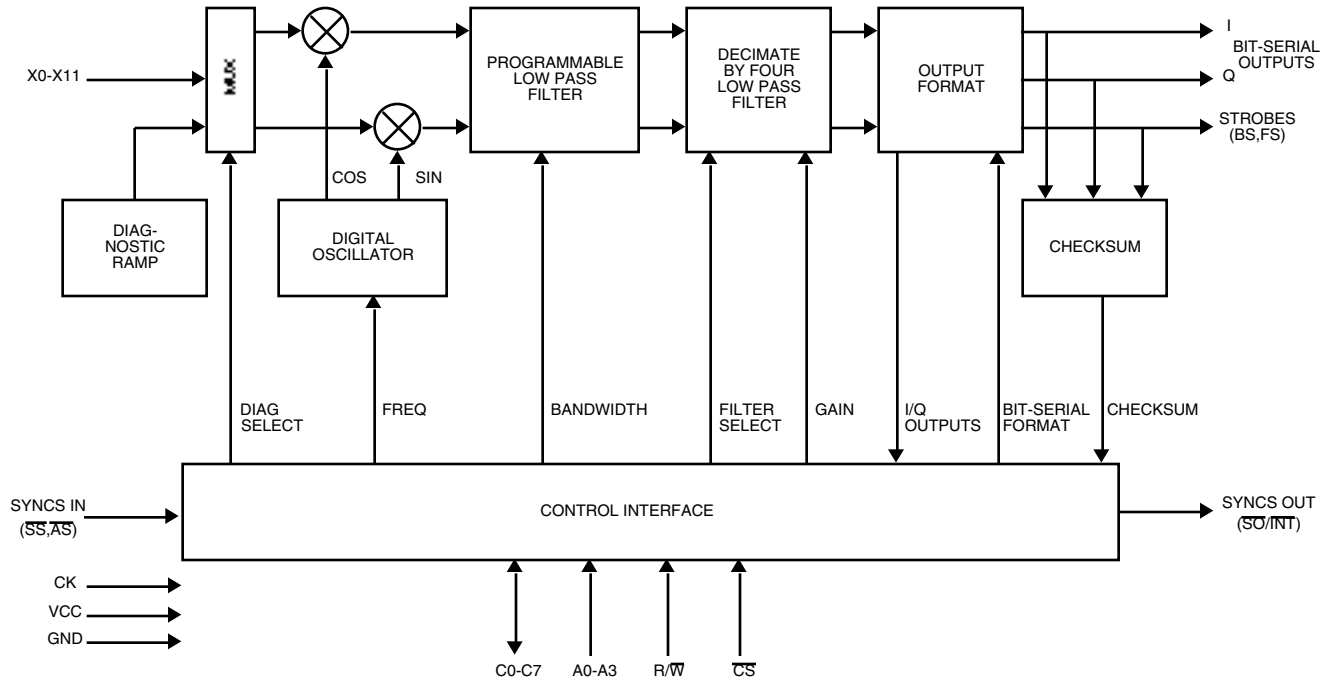


Figure 1. GC1011A BLOCK DIAGRAM

Each of these functions are described below.

1.3 CONTROL INTERFACE

The control interface performs four major functions: It allows an external processor to configure the chip, it allows an external processor to capture and read output samples from the chip, it allows an external processor to perform diagnostics, and it generates internal synchronization strobes.

The chip is configured by writing control information into 8 bit control registers within the chip. The contents of these control registers and how to use them are described in Section 3. The registers are written to or read from using the **C[0:7]**, **A[0:3]**, **R/$\overline{W}$**, and **$\overline{CS}$** pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:3]** to the desired register address, setting the **R/$\overline{W}$** pin low, setting **D[0:7]** to the desired value and then pulsing **$\overline{CS}$** low.

To read from a control register the processor must set **A[0:3]** to the desired address, set **R/$\overline{W}$** high, and then set **$\overline{CS}$** low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set **$\overline{CS}$** high. The **C[0:7]** pins are turned off (high impedance) whenever **$\overline{CS}$** is high or **R/$\overline{W}$** is low. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.

Control register addresses 12, 13, 14, and 15 are reserved to allow an external processor to read output samples from the chip. Addresses 12 and 13 are the I-registers which store the16 bit real part of the output sample. Addresses 14 and 15 are the Q-registers which store the imaginary part. In the real mode the I registers store the even-time output samples and the Q registers store the odd-time output samples. Output ready and missed flags are provided in control register 10 in order to synchronize the storing and reading of the output samples. An interrupt output pin is also provided on the chip which can be used to interrupt the external processor when a new sample is ready. See the description of control register 10 in Section 3.7 for more details. The setup, hold and pulse width requirements for control read or write operations are given in Section 4.4.

Checksums are read from the chip during diagnostics using address 11. More details on the diagnostic modes is given in Section 1.9.

The control interface also generates the chip's internal sync strobes. The user may select to synchronize the chip using an external sync strobe ($\overline{\textbf{SS}}$), or use the chip's internal sync counter. The internal sync counter can be synchronized to $\overline{\textbf{SS}}$, or left to free run (See **SS_OFF** in Section 3.2). The period of the internal sync counter can be either 256 clocks or 2^{20} clocks. The 256 clock period is intended to be used for chip test purposes only. The internal sync counter is used during diagnostics to clear the data paths and strobe the checksum generator. The internal sync counter can also be used to periodically re-synchronize all of the counters in the chip during normal operating modes if the chip's decimation ratio is set to a power of 2. Except for diagnostics the sync counter cannot be used for non-power of 2 decimation modes.

1.4 DIGITAL OSCILLATOR

The digital oscillator generates sine and cosine sequences which are used to mix the desired signal down to zero frequency. The digital oscillator contains a 28 bit frequency register, a 28 bit frequency accumulator, and a sine-cosine generator. The tuning frequency of the oscillator is set by loading a 28 bit frequency word from the control registers into the frequency register. If the frequency register is set to the word **FREQ**, then the tuning frequency will be: $\text{Frequency} = \frac{\text{Sample Rate}}{2^{28}}\textbf{FREQ}$.

The frequency word **FREQ** is stored into the control registers at control addresses 0,1,2 and 3. The 28 bit word is then transferred into the frequency register using one of the following methods:

(1) The frequency register is always loading (the frequency changes immediately as the frequency word is loaded into the control registers).

(2) The frequency register is loaded when the user sets a control register bit.

(3) The frequency register is synchronously loaded when the accumulator sync strobe ($\overline{\textbf{AS}}$) goes low.

(4) The frequency register is synchronously loaded when the system sync strobe ($\overline{\textbf{SS}}$) goes low.

See Section 3.2 for more details on the frequency load modes.

The 28 bit frequency word is accumulated in the 28 bit frequency accumulator. The frequency accumulator will normally free run, but can be synchronously cleared by either the system sync ($\overline{\textbf{SS}}$) or the

accumulator sync (**$\overline{\text{AS}}$**). The accumulator clear modes are controlled by bits in control register 4. See Section 3.2 for details.

The upper 13 frequency accumulator bits are used to generate the oscillator's sine and cosine outputs. These sines and cosines are generated to 12 bit accuracy. The spectral purity of the oscillator is illustrated in the following figures.

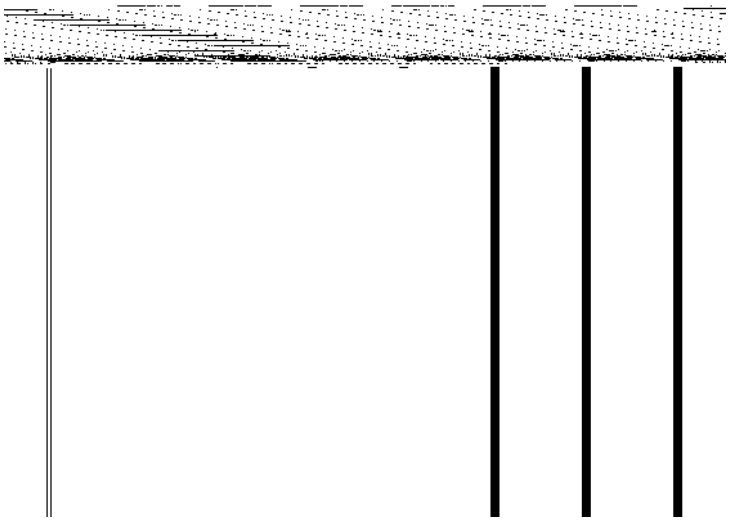


Figure 2. DLO SPECTRUM: FREQ = (HEX) 1234567

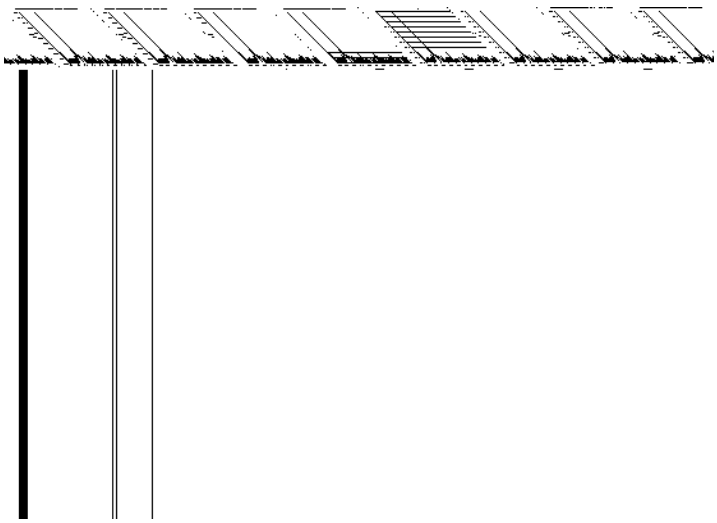


Figure 3. DLO SPECTRUM: FREQ = (HEX) 3456789

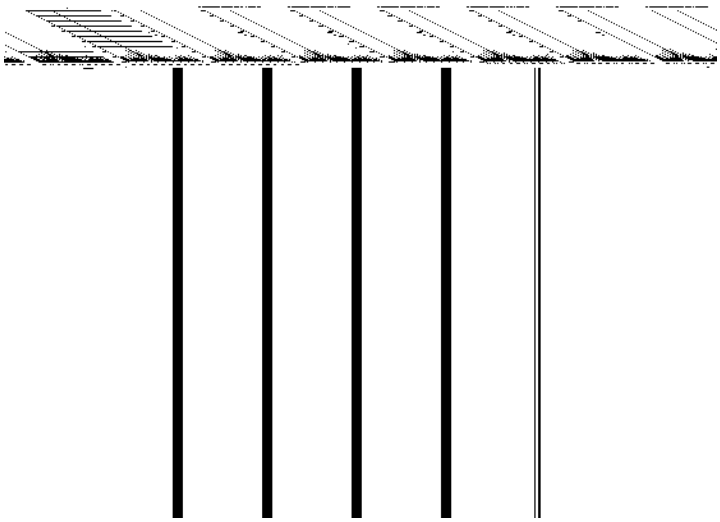


Figure 4. DLO SPECTRUM: FREQ = (HEX) 5678910

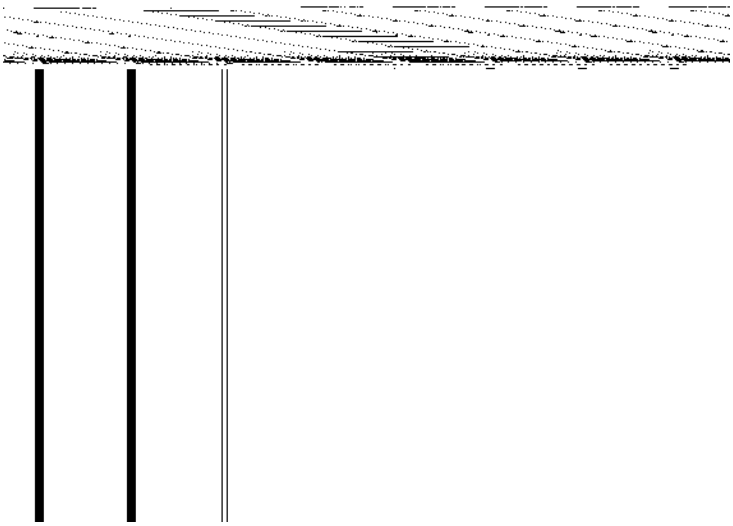


Figure 5. DLO SPECTRUM: FREQ = (HEX) c1234567

The oscillator's peak spur levels, as can be seen from these plots, are well below -75 dB.

1.5 MIXER

The mixer multiplies the 12 bit input samples by the 12 bit sine and cosine values coming from the digital oscillator. An input signal at the oscillator's tuning frequency will be centered at zero frequency after passing through the mixer.

1.6 PROGRAMMABLE LOW PASS FILTER

The mixer's output is filtered to isolate the desired signal using a programmable bandwidth low pass filter. The filter reduces the sample rate by a factor of **D**, where **D** is a user specified integer ranging from 16 to 16,384. The value of **D** is stored in control registers 8 and 9. The out-of-band rejection of the filter is over 72 dB.

1.7 DECIMATE BY FOUR FILTER

The programmable bandwidth filter is followed by a 64 tap filter which, in the complex mode, reduces the sample rate by an additional factor of 4, giving an overall bandwidth (and sample rate) reduction of 4**D**. In the real mode the final filter only reduces the sample rate by a factor of two. The user may select a choice of two spectral responses for this filter. The standard response has a 3 dB passband which covers 80% of the output Nyquist rate and has an out-of-band rejection of over 70 dB. The optional response has a 3 dB passband covering 90% of the Nyquist rate, but only 50 dB of out-of-band rejection. The spectral response of these filters is shown in the following figures.

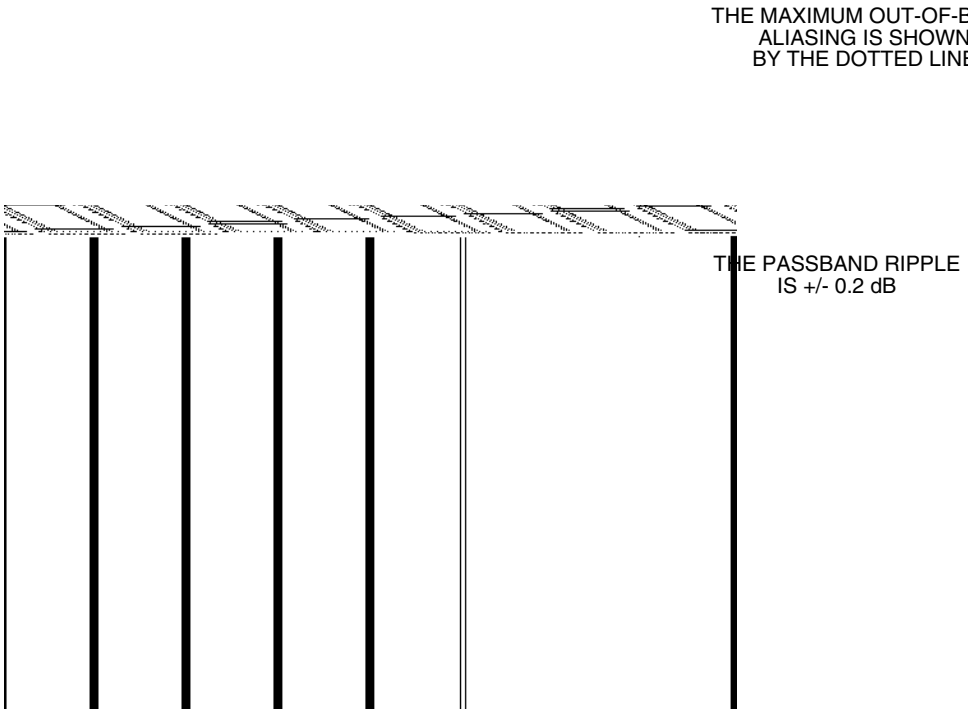


Figure 6. FILTER RESPONSE: 80% FILTER

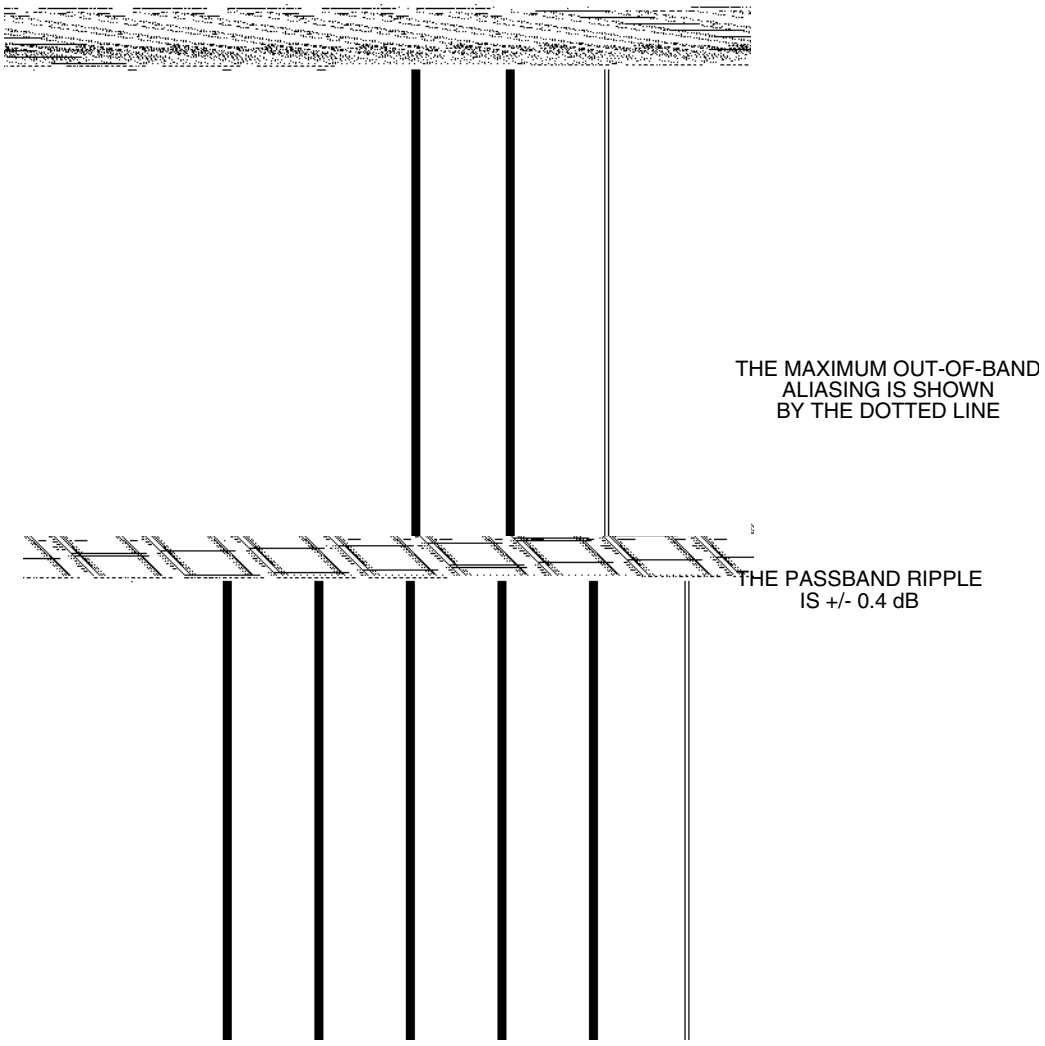


Figure 7. FILTER RESPONSE: 90% FILTER

1.8 OUTPUT FORMATTING

The output format circuit adjusts the gain of the filter output, optionally flips the output spectrum, optionally offsets the spectrum by one-fourth the Nyquist rate, optionally converts the complex output stream to a real one at twice the rate, and rounds the samples to 16 bits. The rounded outputs are passed to the control interface where they can be read by an external processor. They are also passed through a parallel to serial conversion circuit and output as bit-serial streams. Separate bit-serial outputs are provided for the **I** and **Q** halves of the complex output.

The bit-serial output has several programmable features. The user can select:

(1) The rate of the bit-serial stream. The bit rate is programmable to be a power of two division of the clock.

(2) MSB first or LSB first orientation. The 16 bit data is normally output LSB first, but can optionally be output MSB first.

(3) Multiplexed **I/Q** format. The user can have the **I** and **Q** outputs multiplexed together so that the bit streams contain the 16 bit **I** sample followed by the 16 bit **Q** sample. The **I** and **Q** outputs are identical in this mode.

(4) The format of the bit strobe. A bit strobe is provided as a clock for the bit-serial stream. The bit strobe can be selected to have a 50% duty cycle, or to have a pulse width equal to a system clock period. The user can also select the active high or active low polarity of the bit strobe. The clock pulse mode is suitable to be used as a clock enable signal. The bit strobe is a constant high or low level (depending upon the mode and polarity selected) when the bit rate is set to be equal to the clock rate.

(5) The format of the frame strobe. A frame strobe is provided at the start of each output frame. The strobe is either one bit-period wide synchronous with the first bit of the frame, or it is active during the clock cycle before the start of each frame. The active high or low polarity of the strobe is programmable. The frame rate is equal to the complex output rate.

The programmable bit rate allows the user to select the number of times that each 16 bit output sample repeats during a frame. If the frame period is 64 clocks (i.e., the chip is decimating by a factor of 64), then the same 16 bit output sample will be repeated 4 times when the bit rate is equal to the system clock rate. If the bit rate is set to one-half, then the sample will only repeat twice. If the bit rate is set to one-fourth, then there will be exactly one output sample per frame. The higher bit rates allow one to multiplex the outputs from multiple GC1011A chips into a single time division multiplexed (TDM) stream. If the bit rate is set so that each output sample is repeated four times in a frame, then the outputs from four chips can be multiplexed into a TDM stream by selecting the first chip's output for the first 16 bit-strobes of the frame, selecting the second chip's output for the next 16 strobes, selecting the third chip's output for the next 16 strobes, and then selecting the last chip's output for the final 16 strobes of the frame.

In the real output mode the frame rate is double the complex mode rate and the output signal is shifted in frequency so that it is centered from 0 to $F_O/2$, where F_O is the output sample rate. The I and Q output streams are identical in the real mode. For compatibility with system designs using the older GC1011 chip see the REAL_FS bit described in Section 3.7.

The output format circuitry is synchronized by the $\overline{\mathbf{SS}}$ input sync. This allows one to synchronize the output frame timing of multiple GC1011A chips.

1.9 DIAGNOSTICS

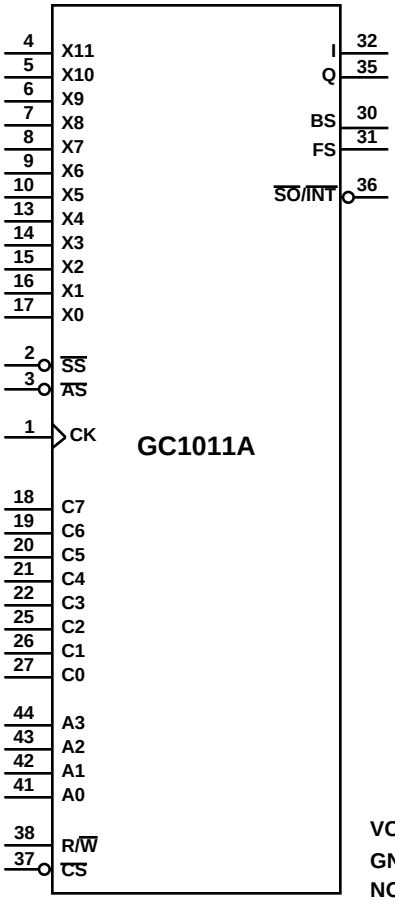
An input ramp generator, a sync period generator, and a checksum generator are provided on the chip in order to run diagnostic tests. Diagnostics are performed by turning on the ramp generator, enabling the diagnostic syncs, letting the chip operate for at least 4 sync periods, reading the checksum and comparing it to its predicted value. A new checksum is generated every sync period. The input ramp sequence is the same for every sync period and the chip is re-initialized at the beginning of each sync period so that each checksum should be the same once the chip's data path has been flushed. The chip requires at least 3 sync periods to flush, so the fourth and following checksums should be valid. The test is then repeated for several different tuning frequencies, decimation settings, and output modes.

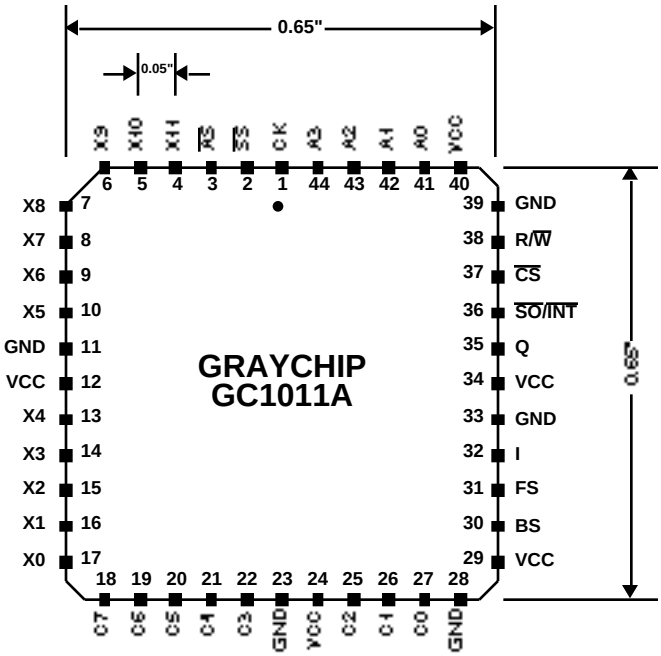
The sync period is 2^{20} clocks, or approximately 1 million clock cycles, so four sync periods will be about 4 million clocks. This represents a delay of less than 15 milliseconds for a clock rate of 60 MHz.

The following table lists the expected checksums for four test configurations. All values are in HEX.

CONTROL REGISTER	TEST 1	TEST 2	TEST 3	TEST 4
FREQ (REG 0,1,2,3)	0000101	0F0F0F0	55AA55A	AA55AA5
SYNC MODE (REG 4)	A9	A9	A9	A9
OUTPUT MODE (REG 5)	01	51	F2	0C
FILTER MODE (REG 6)	50	66	7D	4B
GAIN (REG 7)	0	1	2	3
DECIMATION (REG 8,9)	000F	0020	0F30	30C1
EXPECTED CHECKSUMS (GC1011A)				
(REG 11)	32	9E	22	52
EXPECTED CHECKSUMS (GC1011)				
(REG 11)	96	EB	9A	A6

2.0 PIN DESCRIPTIONS





44 PIN J-LEAD CHIP CARRIER

(CALL GRAYCHIP FOR ALTERNATE PACKAGE AVAILABILITY)

VCC PINS: 12, 24, 29, 34, 40

GND PINS: 11, 23, 28, 33, 39

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO PINS 11,12 AND PINS 33,34

SIGNAL	DESCRIPTION
X[0:11]	**INPUT DATA.** *Active high* The 12 bit two's complement input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
CK	**CLOCK INPUT.** *Active high* The clock input to the chip. The **X**, **$\overline{\text{SS}}$**, and **$\overline{\text{AS}}$** signals are clocked into the chip on the rising edge of this clock. The **I**, **Q**, **BS**, **FS**, and **$\overline{\text{SO}}$** signals are clocked out on the rising edge of this clock.
$\overline{\text{SS}}$	**SYSTEM SYNC**. *Active low* The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{\text{SS}}$**. Bits in control register 4 (see Section 3.2) determine the operation of **$\overline{\text{SS}}$**. This sync is clocked into the chip on the rising edge of the clock.

$\overline{\text{AS}}$ **ACCUMULATOR SYNC**. *Active low*
The accumulator sync is provided to synchronously change tuning frequencies. This sync can be used to load a new tuning frequency into the frequency register and/or to clear the frequency accumulator. This signal is clocked into the chip on the rising edge of the clock.

I **IN-PHASE OUTPUT STREAM**. *Active high*
The I part of each complex output sample is output as a bit serial stream on this pin. The bits are clocked out on the rising edge of the clock.

Q **QUADRATURE OUTPUT STREAM**. *Active high*
The Q part of each complex output sample is output as a bit serial stream on this pin. The bits are clocked out on the rising edge of the clock.

BS **BIT STROBE**. *Programmable active high or low level*
This strobe is output synchronous with the **I** and **Q** bit streams. The strobe occurs once per bit and is either one clock wide or has a 50% duty cycle. The high/low polarity of the strobe is programmable. See Section 3.3 for details.

FS **FRAME STROBE**. *Programmable active high or low level*
This strobe marks the beginning of an output frame. The strobe is either one clock cycle wide, or is the width of a data bit at the selected bit rate. The high/low polarity of this signal is programmable. See Section 3.3 for details.

$\overline{\text{SO}}$/$\overline{\text{INT}}$ **SYNC OUT OR INTERRUPT OUT**. *Active low*
This signal is either a sync output or is an interrupt output depending upon a bit in control register 10. As a sync output, the signal is a delayed version of the input system sync **$\overline{\text{SS}}$**, or is the internally generated sync which has a period of 2^{20} clocks, or is a one-shot sync strobe. As an interrupt output, the signal is the READY flag from control register 10. This flag goes active when a new output sample is ready in control registers 12, 13, 14, and 15.

C[0:7] **CONTROL DATA I/O BUS**. *Active high*
This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{\text{CS}}$** is low and **R/$\overline{\text{W}}$** is high.

A[0:3] **CONTROL ADDRESS BUS**. *Active high*
These pins are used to address the 16 control registers within the chip. Each of the 16 control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:3]** to the register's address.

R/$\overline{\text{W}}$ **READ/$\overline{\text{WRITE}}$ CONTROL**. *High for read, low for write*
This pin determines if the control bus cycle is a read or write operation. The pin is high for a read and is low for a write.

$\overline{\text{CS}}$ **CONTROL STROBE**. *Active low*
This control strobe enables the read or write operation. The contents of the register selected by **A[0:3]** will be output on **C[0:7]** when **R/$\overline{\text{W}}$** is high and **$\overline{\text{CS}}$** is low. If **R/$\overline{\text{W}}$** is low when **$\overline{\text{CS}}$** goes low, then the selected register will be loaded with the contents of **C[0:7].**

3.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 16 eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{CS}$**, **R/$\overline{W}$**, **A[0:3]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	FREQ byte 0	8	Decimation byte 0
1	FREQ byte 1	9	Decimation byte 1
2	FREQ byte 2	10	Output Status
3	FREQ byte 3	11	Checksum
4	Sync mode	12	I-output byte 0
5	Output mode	13	I-output byte 1
6	Filter mode	14	Q-output byte 0
7	Gain	15	Q-output byte 1

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

3.1 FREQUENCY WORD REGISTERS

Registers 0, 1, 2, and 3 contain the 28 bit frequency tuning word. Bit 0 is the LSB, bit 27 is the MSB.

ADDRESS 0: FREQUENCY BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[0:7]	Byte 0 (least significant) of frequency word

ADDRESS 1: FREQUENCY BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[8:15]	Byte 1 of frequency word

ADDRESS 2: FREQUENCY BYTE 2

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[16:23]	Byte 2 of frequency word

ADDRESS 3: FREQUENCY BYTE 3

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**FREQ**[24:27]	4 most significant bits of the frequency word
4-7	R/W	-	unused

If the desired tuning frequency is **F**, then the frequency word should be set to:

$$\mathbf{FREQ} = 2^{28}\mathbf{F}/(\text{clock rate})$$

3.2 SYNC MODE REGISTER

The sync mode register controls the action of the **$\overline{SS}$** and **$\overline{AS}$** sync strobes and how they affect the chip's internal timers, counters, and accumulators.

ADDRESS 4: Sync Mode Register

BIT	TYPE	NAME	DESCRIPTION
0 (LSB)	R/W	SS_OFF	This bit disables the **$\overline{SS}$** input.
1	R/W	AS_ON	Enables the accumulator sync **$\overline{AS}$**. Normally the frequency accumulator will free run. This bit causes the frequency accumulator to be initialized to the contents of the frequency register when **$\overline{AS}$** goes low. **$\overline{SS}$**, instead of **$\overline{AS}$**, will reset the accumulator if AS_MUX is set and **$\overline{SS}$** is not disabled by SS_OFF.
2	R/W	AS_MUX	Use **$\overline{SS}$** for the accumulator sync. The **$\overline{AS}$** input is ignored and the **$\overline{SS}$** strobe is used in its place when this bit is set and **$\overline{SS}$** is not disabled by SS_OFF. (See AS_ON and AS_FREQ).
3	R/W	LD_FREQ	Load the frequency register in the digital oscillator with the contents of the frequency word registers. If left on, this bit will cause the frequency register to load whenever a frequency word register is changed.
4	R/W	AS_FREQ	Enables the synchronous frequency load mode. When this bit is set and **$\overline{AS}$** goes low, the frequency register will be synchronously loaded with the contents of the frequency control registers. **$\overline{SS}$**, instead of **$\overline{AS}$**, will load the frequency register if AS_MUX is set and **$\overline{SS}$** is not disabled by SS_OFF.
5	R/W	SS_DIAG	Enables diagnostic syncs. This bit routes the internal sync to the checksum generator and to all accumulators and control counters within the chip. This forces the chip to re-initialize at the start of every sync period. The internal sync period will be 2^{20} clocks if SS_MUX is set, otherwise it will be determined by the period of an externally provided **$\overline{SS}$** strobe.
6	R/W	TEST	Shortens the internal sync counter period from 2^{20} clocks to 2^{8} clocks. This mode is used to test chips at the factory.
7 (MSB)	R/W	SS_MUX	Use the sync counter's terminal count strobe for the internal sync instead of the sync input **$\overline{SS}$**. The internal sync is output on the **$\overline{SO}$** pin.

The operation of these control bits are illustrated in Figure 8 on the next page.

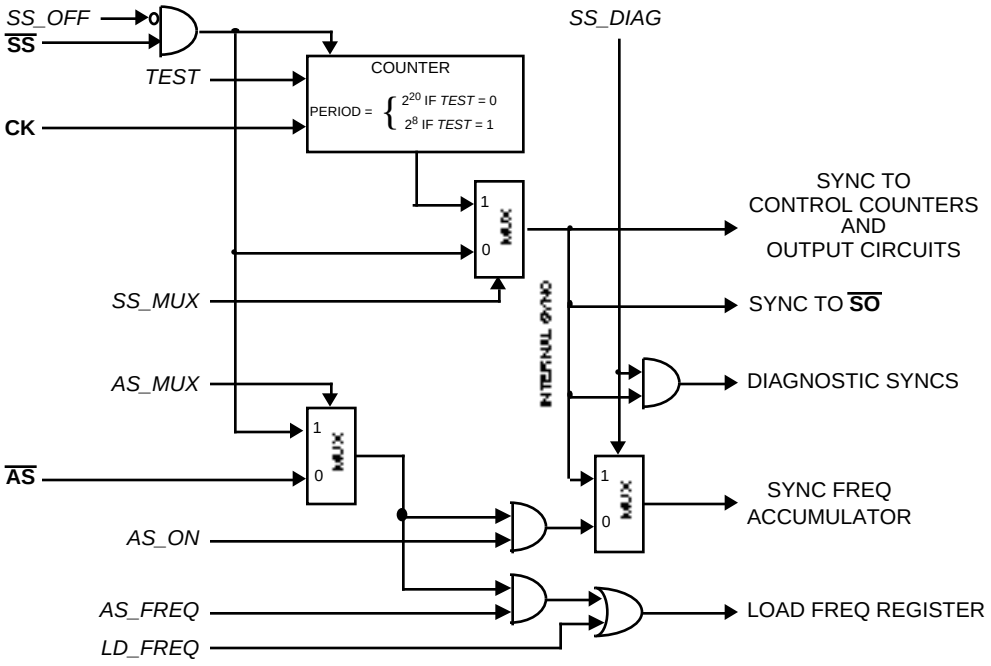


Figure 8. SYNC CONTROLS

3.3 OUTPUT MODE REGISTER

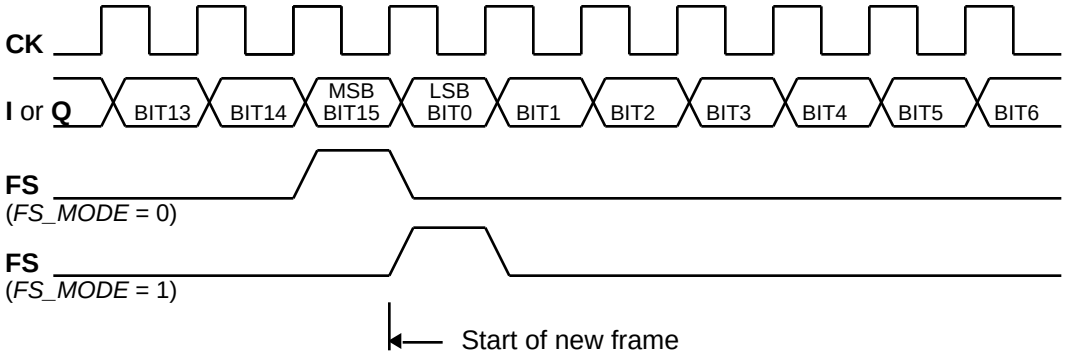
The output mode register contains the controls for the bit-serial outputs.

ADDRESS 5: Output mode register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**RATE**[0:3]	The bit rate select. The bit serial rate is: Bit rate = $2^{-\mathbf{RATE}}$ (clock rate)
4	R/W	BS_MODE	Changes the mode of **BS**. Normally **BS** pulses high during the clock cycle before a bit transition. This bit changes **BS** so that it is a 50% duty cycle clock with its rising edge in the middle of each bit period
5	R/W	BS_POL	Changes the polarity of **BS**.
6	R/W	FS_MODE	Changes the mode of **FS**. Normally **FS** pulses high during the clock cycle before the start of a new frame. This bit changes **FS** so that it will be high for the first bit period of each new frame.
7	R/W	FS_POL	Changes the polarity of **FS**.

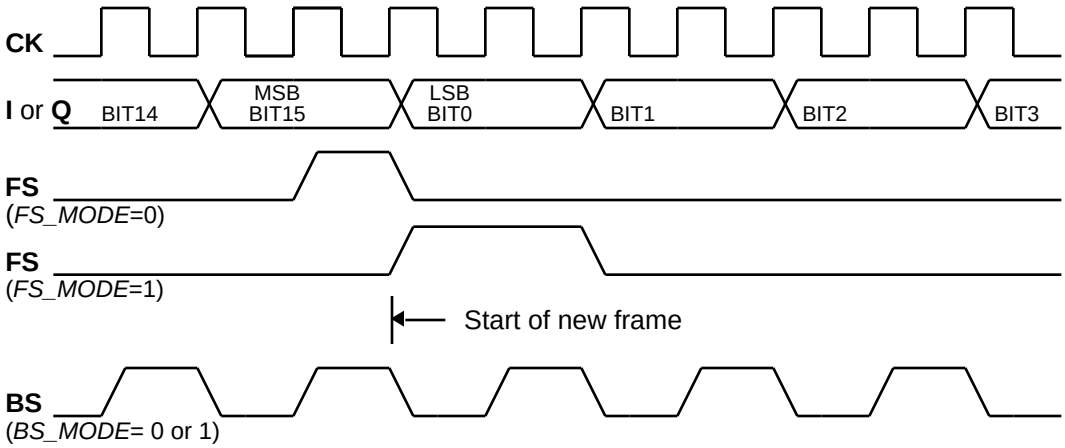
These controls are illustrated in the timing diagrams shown in Figure 9 on the next page. Note that the polarity shown for **BS** and **FS** can be changed using *BS_POL* and *FS_POL*.

FULL RATE: **RATE**=0



BS is a constant high if *BS_MODE* = 0, and is low if *BS_MODE* = 1

HALF RATE: **RATE**=1



QUARTER RATE: **RATE**=2

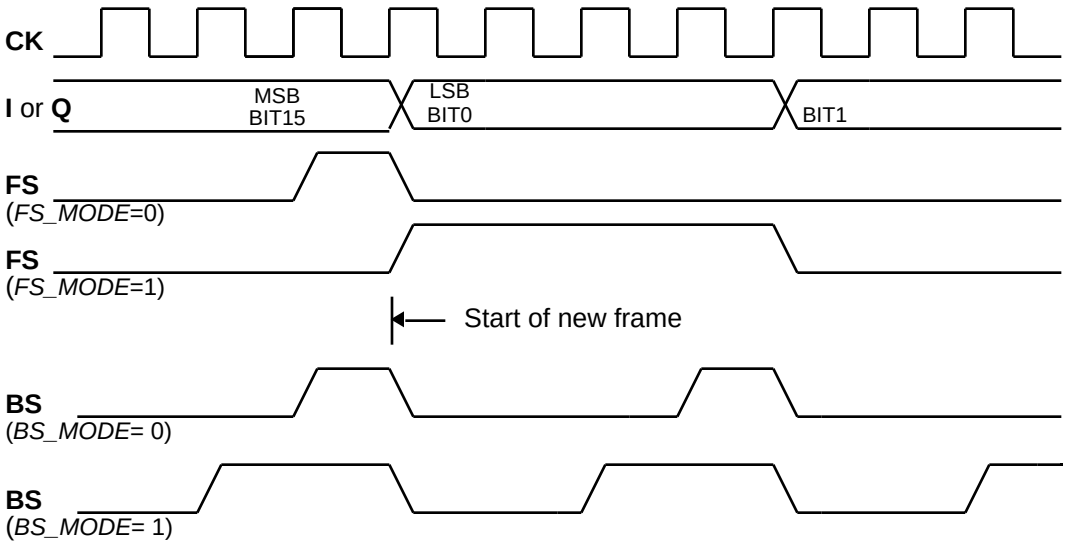


Figure 9. TIMING FOR BIT-SERIAL MODES

3.4 FILTER MODE REGISTER

This register controls filtering, output formatting and the diagnostic input mode.

ADDRESS 6: Filter Mode Register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	FSEL	Use the 90% filter instead of the 80% filter.
1	R/W	REAL	Use real output format instead of complex. The OFFSET and REAL_FS (see Section 3.7) control bits must also be high for the real mode to work. The output data rate is double the complex data rate in this mode.
2	R/W	OFFSET	Offset the output spectrum. In the complex output mode (REAL=0), this bit forces the output spectrum to be centered at $F_{CK}/2$, where F_{CK} is the output sample rate. This mode is useful for single-sideband AM signals because it moves the lower band edge up to zero frequency where it belongs. The upper half of the spectrum, in the complex mode, will appear as negative frequencies. This mode is mandatory in the real output mode.
3	R/W	FLIP	Flip the output spectrum. This bit inverts the output spectrum. In the complex mode the spectrum is flipped about zero. In the real mode the spectrum is flipped about $F_{CK}/4$, where F_{CK} is the real mode's output sample rate.
4	R/W	IQ_MUX	Multiplex the I and Q outputs together. In this mode the bit -serial output alternates between the 16 bit I sample and the 16 bit Q sample. The I sample is output first in each frame followed by the Q sample. The I and Q samples alternate, 16 bits each, until the end of the frame. The **I** and the **Q** pins output identical bit-streams in this mode.
5	R/W	MSB_MODE	Output MSB first instead of LSB first. Normally the 16 bit samples are output LSB first. The MSB is output first when this bit is set.
6	R/W	DIAG	Use the diagnostic ramp for the input to the chip instead of the **X** input. The ramp counts from -2048 to +2047 and then starts over again.
7	R/W	POWER_DOWN	Allows the $\overline{\textbf{AS}}$ input to gate the chip's internal clock. The clock is always enabled when this bit is low.

The effect on the output spectrum of the REAL, OFFSET and FLIP bits is illustrated in the following diagram. (F_O is the output sample rate))

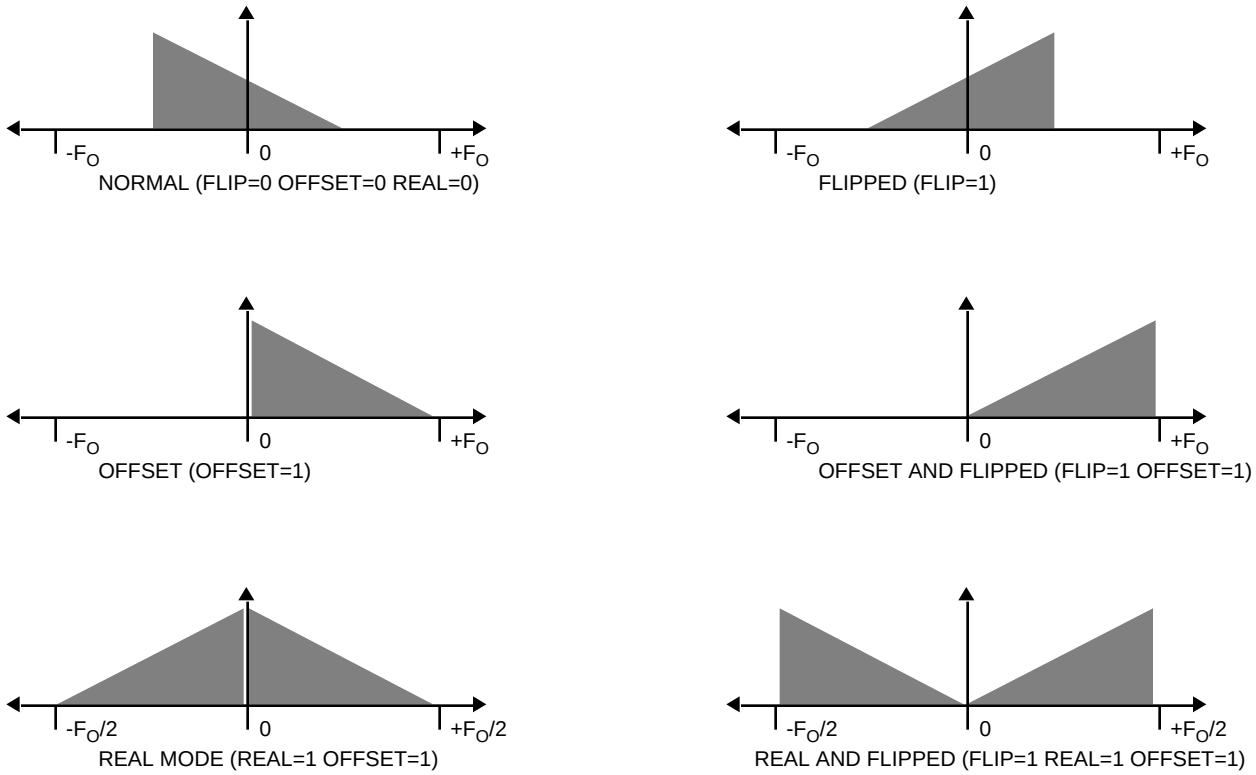


Figure 10. OUTPUT SPECTRAL FORMATS

The POWER_DOWN control bit is used in conjunction with the **$\overline{\text{AS}}$** input pin to decrease the power consumed by the GC1011A chip in a stand-by mode. The power can be reduced by a factor of N (to a minimum of about 1mW) by setting the POWER_DOWN control bit and then pulsing **$\overline{\text{AS}}$** low for one clock cycle out of N. All control registers retain their state during power down, but the chip's **I**, **Q**, **BS**, **FS** and **SO** output signals will not be valid. Note that an internal clock rate (F_{CK}/N) less than 10 Hz may damage the chip.

3.5 GAIN CONTROL REGISTER

This register sets the output gain.

ADDRESS 7: Gain Control Register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**GAIN[0:3]**	The 4 bit gain word. The gain is equal to $2^{\mathbf{GAIN}}$, allowing gain adjustments in 6 dB increments.
4-7	R/W	-	Unused

The chip has unity gain when the decimation in the programmable low-pass filter has been set to a power of two. If the decimation is not a power of two, then the gain is given by $G=(\mathbf{D}/\mathbf{P})^4$, where **D** is the decimation in the programmable low-pass filter (See Section 3.6) and **P** is the next power of two greater than **D**. For example, if **D** is 30 the gain would be $(30/32)^4=0.772$, or -2.2 dB. If **D** is 33 the gain would be $(33/64)^4=0.071$, or -23 dB. The nominal gain setting in the first example would be zero and would be 3 or 4 in the second example.

The overall gain of the chip is given by:

$$G = 2^{\mathbf{GAIN}}(\mathbf{D}/\mathbf{P})^4.$$

In dB this is approximately:

$$G_{dB} = (6x\mathbf{GAIN})+(80 \log(\mathbf{D}/\mathbf{P})).$$

If the gain is too high, the chip will clip the samples to +/- full scale and will set the overflow bit in the output status register (See Section 3.7).

3.6 DECIMATION CONTROL REGISTERS

These registers set the decimation ratio in the programmable low-pass filter.

ADDRESS 8: Decimation Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**DEC[0:7]**	8 LSBs of **DEC**

ADDRESS 9: Decimation Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-5	R/W	**DEC[8:13]**	6 MSBs of **DEC**
6,7	R/W	-	Unused

A decimation ratio of **D** is set by programming **DEC** to be equal to (**D**-1). The minimum value of **DEC** is 15 and the maximum is 16,383 corresponding to the minimum decimation of 16 and maximum of 16,384.

3.7 OUTPUT STATUS REGISTER

This register contains flags and status information for the output samples.

ADDRESS 10: Output Status Register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	READY	Tells the chip that the user is ready to capture an output sample. The chip clears this bit when it has captured the sample.
1	R/Clear	MISSED	The chip sets this bit high if a new output sample was ready but the user had not set READY high. This lets the user know if a sample has been missed. This bit is cleared by writing a 0 to the bit. Attempting to write a 1 to this bit does nothing.
2	R/W	OVERFLOW	The chip sets this bit when an overflow occurs. This bit can be used to indicate if the gain is set too high. This bit stays high until the user clears it.
3	R/W	INT_ENABLE	This bit is used in the interrupt mode (See bit 4 below) to turn on the interrupt output. If this bit is off the **$\overline{\text{INT}}$** output pin is forced high. When this bit is high the **$\overline{\text{INT}}$** output pin is equal to READY. When READY goes low, meaning that a new sample has been captured, the **$\overline{\text{INT}}$** pin will go low. If **$\overline{\text{INT}}$** is tied to a processor's interrupt input, then the processor will be interrupted whenever a new sample is ready.
4	R/W	INT_MODE	This bit selects the **$\overline{\text{INT}}$** signal for output on pin **$\overline{\text{SO}}$/$\overline{\text{INT}}$**. Normally **$\overline{\text{SO}}$** is output on the pin.
5	R/W	STROBE_MODE	This bit selects the one-shot sync strobe for output on the **$\overline{\text{SO}}$** pin. When this bit is low the **$\overline{\text{SO}}$** sync is determined by SS_MUX (see Section 3.2).
6	R/W	STROBE	This bit will generate a one clock cycle wide **$\overline{\text{SO}}$** strobe each time it is set. STROBE_MODE must be set before this bit is set and INT_MODE must be low. This bit must be cleared before a new strobe can be generated.
7	R/W	REAL_FS	Used in the real output mode to double the frame rate. If this bit is not set in the real mode, then the chip will operate in the GC1011 real output mode. In the GC1011 mode two real samples are output every frame and the frame rate remains the same as in the complex mode. The I stream will output the even indexed time samples (time=0,2,4,6,...) and the Q stream will output the odd time samples.

The READY signal is used to capture output samples and to read them into an external processor. The user captures outputs by setting the READY bit and then waiting for the bit to be cleared by the chip. When the bit goes low the processor can read the samples out of the I and Q output registers described in

section 3.9. The processor can wait for READY to go low by either continuously reading this register, or it can use the interrupt output **$\overline{\text{INT}}$** to tell it when the sample is ready. To use the interrupt output mode the user must tie the **$\overline{\text{SO}}$/$\overline{\text{INT}}$** output pin from the chip to an interrupt input of the processor and must set the INT_MODE bit in this register. The processor can then capture samples by setting READY and then setting INT_ENABLE (INT_ENABLE should be set after READY in order to avoid a spurious interrupt due to the interrupt being enabled before READY has settled to its high state). The processor will be interrupted when READY goes low again. When it is interrupted the processor can turn off INT_ENABLE, read the I/Q outputs, and then start over again.

The MISSED flag is provided to let the processor know if it has taken too long to read the I/Q samples before rearming the READY bit. If the processor wants to use the MISSED flag it should clear the flag the first time it sets the READY bit and then check it after setting the READY bit thereafter. The READY bit is set and the MISSED bit cleared by writing a 01(hex) to this register. The READY bit is set and the MISSED bit is left alone by writing a 03(hex) to this register. If interrupts are used, then the user should also set the INT_MODE bit at the same time by writing an 11(hex) or 13(hex) to the register followed by a 1B(hex) to enable the interrupts.

The one-shot strobe is generated by turning INT_MODE off, STROBE_MODE on and STROBE off. **$\overline{\text{SO}}$** strobes are then generated by setting the STROBE bit. This is done by writing a 20(hex) to this register followed by a 60(hex).

3.8 CHECKSUM REGISTER

This read-only register stores the checksums generated in the diagnostic mode.

ADDRESS 11: CHECKSUM

BIT	TYPE	NAME	DESCRIPTION
0-7	R	CHECK[0:7]	The 8 bit checksum. The checksum is generated as a non-linear feedback accumulation of the **BS**, **FS**, **I**, and **Q** output bits. The current checksum is stored in this register and the checksum generator is cleared whenever the internal sync goes low (see SS_MUX in Section 3.2 for the modes of the internal sync).

3.9 I AND Q OUTPUT REGISTERS

These registers are used to capture output samples.

ADDRESS 12: I-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[0:7]**	Least significant 8 bits of the **I** output.

ADDRESS 13: I-Output Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[8:15]**	Most significant 8 bits of the **I** output.

ADDRESS 14: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**Q[0:7]**	Least significant 8 bits of the **Q** output.

ADDRESS 15: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**QI[8:15]**	Most significant 8 bits of the **Q** output.

The user reads the **I** and **Q** outputs through these read-only registers. The captured samples can be used for gain control, analysis, display, or diagnostics.

4.0 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Referenced to GND:

PARAMETER		MIN	TYP	MAX	UNITS
V_{CC}	DC Supply Voltage	-0.3		7	V
V_{IN}	Input voltage (undershoot and overshoot)	-0.7		V_{CC}+0.7	V
T_{STG}	Storage Temperature	-65		150	°C
F_{CK}	Clock Rate[1]	10			Hz

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNITS
V_{CC}	DC Supply Voltage	3.0	5.0	6.0	V
T_A	Temperature Ambient, no air flow	0		60	°C

4.3 DC CHARACTERISTICS

All parameters are at V_{CC}=5V and temperature is 0 to 60 °C ambient unless noted

PARAMETER			MIN	TYP	MAX	UNITS
V_{IL}	Voltage input low				0.8	V
V_{IH}	Voltage input high	V_{CC}=5V	2.0			V
		V_{CC}=3.3V	1.5			V
I_{IN}	Input current (V_{IN}=0V)			+/-50		µA
V_{OL}	Voltage output low (I_{OL} = 4mA)				0.5	V
V_{OH}	Voltage output high (I_{OH} = -4ma)	V_{CC}=5V	2.5		5	V
		V_{CC}=3.3V	1.5		3.3	V
C_{IN}	Data input capacitance (All inputs except **CK** and **C[0:7]**)			4		pF
C_{CK}	Clock input capacitance (**CK** input)			8		pF
C_{CON}	Control data capacitance (**C[0:7]** I/O pins)			6		pF

1. The chip may be damaged if power is applied for more than 1 second and the clock is below this rate.

4.4 AC CHARACTERISTICS

Commercial temperature range (0 to 60°C), V_{CC} +/- 5%, unless noted.

PARAMETER					MIN	TYP	MAX	UNITS
F_{CK}	Clock frequency[1]	GC1011A	V_{CC}=	5v	0.1		70	MHz
				3.3v	0.1		42	
		GC1011	V_{CC}=	5v	20		70	MHz
				3.3v	0.1		42	
t_{CKL}	Clock low period (Below V_{IL})		V_{CC}=	5v	6			ns
				3.3V	10			
t_{CKH}	Clock high period (Above V_{IH})		V_{CC}=	5v	6			ns
				3.3v	10			
t_{SU}	Data setup (**X**,**$\overline{AS}$**, or **$\overline{SS}$**) before **CK** goes high							
			V_{CC}=	5v	2			ns
				3.3v	4			
t_{HD}	Data hold time (**X**,**$\overline{AS}$**, or **$\overline{SS}$**) after **CK** goes high				0			ns
t_{DLY}	Data output delay (**I**, **Q**, **BS**, **FS**, or **$\overline{SO}$**) from **CK**[2]							
			V_{CC}=	5v			9	ns
				3.3v			14	
t_{CSU}	Control setup before **$\overline{CS}$** goes low (**A**, **R/$\overline{W}$** during read, and **A**, **R/$\overline{W}$, C** during write)				5			ns
t_{CHD}	Control hold after **$\overline{CS}$** goes high (**A**, **R/$\overline{W}$** during read, and **A**, **R/$\overline{W}$, C** during write)				5			ns
t_{CSPW}	Control strobe pulse width (Write operation)				20			ns
t_{CDLY}	Control output delay to **C** after **$\overline{CS}$** goes low[3] (Read operation)						30	ns
t_{CZ}	Control tristate delay after **$\overline{CS}$** goes high						10	ns
I_{CCQ}	Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK}=100Hz)						200	µA
I_{CC}	Supply current (F_{CK}=50 MHz, V_{CC}=5.0V, **D**=64)						150	mA

$$ICC\ (MAX) = \left(\frac{VCC}{5}\right)\left(\frac{FCK}{50\ MHz}\right)\left(0.56 + 0.44\left(\frac{64}{D}\right)\right)150\ mA$$

1. The chip may not operate properly at clock frequencies below MIN and above MAX, **D** is the decimation ratio (see Section 3.6)
2. Capacitive output load is 20 pf. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or falling below V_{IL}.
3. Capacitive output load is 80 pf.

5.0 APPLICATION NOTES

5.1 POWER AND GROUND CONNECTIONS

The GC1011A chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC1011A chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 µf) adjacent to each GC1011A chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC1011A chip may not operate properly if these power and ground guidelines are violated.

5.2 STATIC SENSITIVE DEVICE

The GC1011A chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

5.3 70 MHZ OPERATION

Care must be taken in generating the clock when operating the GC1011A chip at its full 70 MHz clock rate. The user must insure that the clock is above 2 volts for at least 6 nanoseconds and is below 1 volt for at least 6 nanoseconds. At 70 MHz the clock period is only 14 nanoseconds so that the clock must have a duty cycle of exactly 50%, and the rise and fall times can only be one nanosecond each. One must also be careful to prevent clock undershoot below ground. An ideal clock at 70 MHz would be a square wave with a low voltage of 0.5 volts and a high voltage of 2.5 volts.

5.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC1011A chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements. When operating at a reduced voltage, GRAYCHIP recommends driving the GC1011A chip inputs with the 5 volt to 3 volt interface chips sold by Performance Semiconductor.

5.5 SYNCHRONIZING MULTIPLE GC1011A CHIPS

A system containing a bank of GC1011A chips will need to be synchronized so that the output frames from each chip are aligned, and, if desired, so that their frequency accumulators are running synchronously. The GC1000 Input Switch chip has built in sync counters which are designed specifically for this purpose. If the GC1000 chip is not used, then the one-shot strobe (see Section 3.7) can be used. The bank of chips should be interconnected so that the **$\overline{\text{SO}}$** pin of one GC1011A chip is tied to the **$\overline{\text{SS}}$** input of all of the chips. The one-shot strobe mode can then be used to simultaneously synchronize all of the chips. The **$\overline{\text{SO}}$** pin of a second GC1011A chip should be tied to the **$\overline{\text{AS}}$** input of all of the chips. The one-shot mode of the second chip can be used to synchronize the frequency accumulators whenever the tuning frequency has been changed.

5.6 PROCESSING COMPLEX DATA

Two GC1011A chips can be used to process complex input data by using one chip to process the I-input data and the other to process the Q-input data. If the two chips are synchronized as discussed above, then the complex output stream can be reconstructed by adding and subtracting the I and Q outputs of the two chips. A programmable gate array chip such as from XILINX would be ideal for this post-processing. The configuration for processing complex data is illustrated in Figure 11.

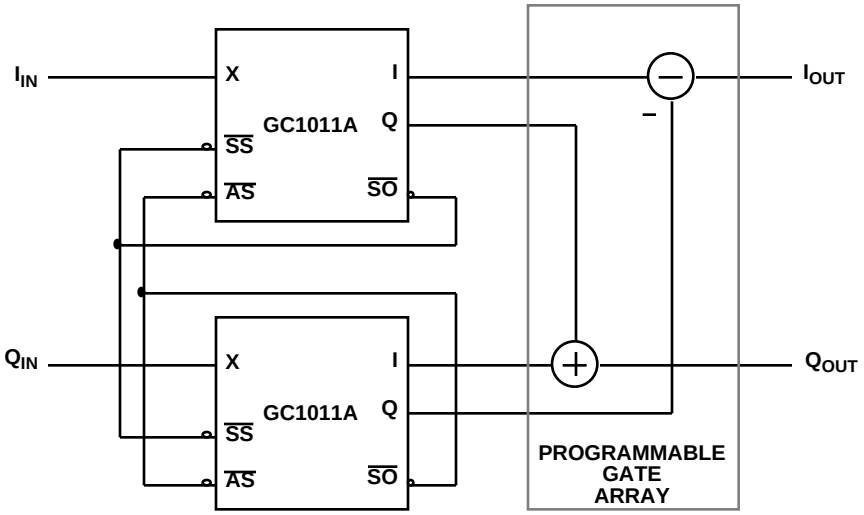


Figure 11. PROCESSING COMPLEX INPUT DATA

5.7 EXAMPLE RECEIVER ARCHITECTURE

An example digital receiver architecture using the GC1011A chip is shown in Figure 12.

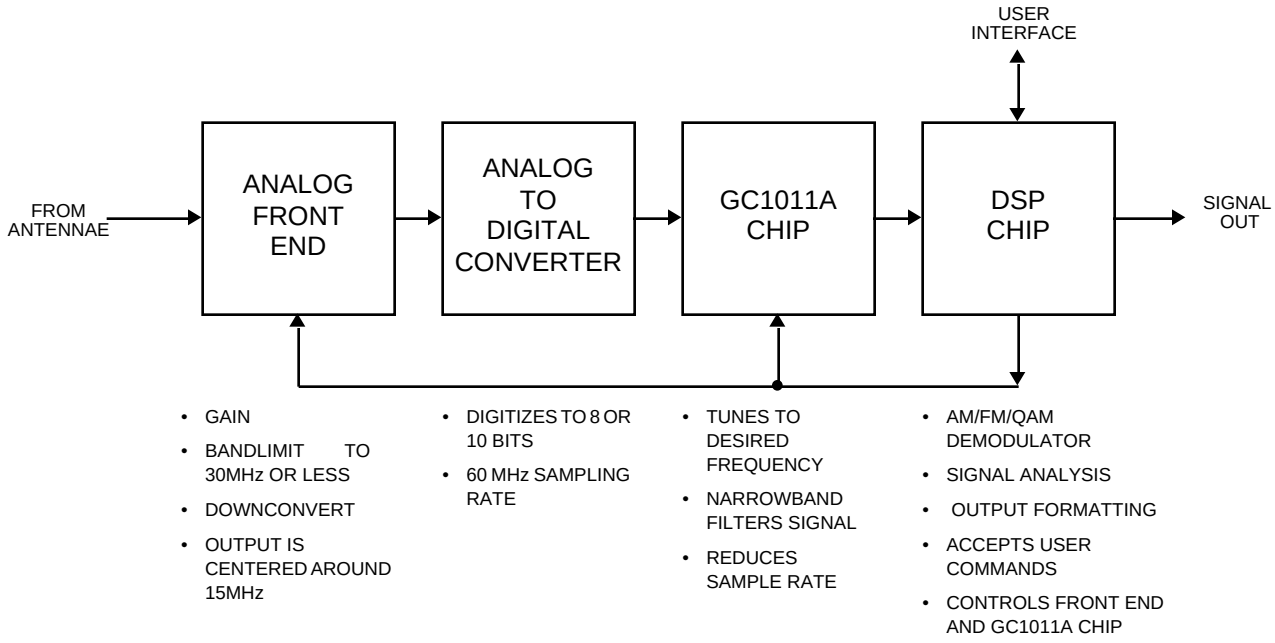


Figure 12. EXAMPLE DIGITAL RECEIVER ARCHITECTURE

The receiver contains an analog front end which downconverts up to 30MHz of radio spectrum to an IF frequency around 15MHz[1]. It also adjusts the gain of the signal so that it fills the dynamic range of the analog to digital converter (ADC). The ADC digitizes the signal to 8 or 10 bits[2] at a sampling rate of 60 MHZ. The GC1011A chip tunes, downconverts, and narrowband filters desired frequencies from within the 30 MHz band. The GC1011A output is then processed by a DSP chip for any final filtering, demodulation or signal analysis. The DSP chip also handles the user interface and provides tuning controls to the GC1011A chip and analog front end.

For applications which do not require the DSP chip at the back end, a simplified architecture can realized by replacing the DSP chip with an digital to analog converter.

1. Note that the HF spectrum (1 to 30MHz) can be digitized directly.
2. The GC1011A chip will accept a 12 bit ADC output as soon as 60 MHZ 12 bit ADCs are available.

GRAYCHIP
(415) 323-2933
FAX (415) 323-0206
DSP CHIPS AND SYSTEMS 2314 Ramona St. Palo Alto, CA. 94301

GC1011A

DIGITAL RECEIVER CHIP

DATASHEET

Revised

November 24, 1992

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265