Designer's™ Data Sheet

Fully Isolated TMOS E-FET™ High Energy Power MOSFET

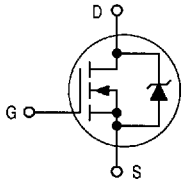
N–Channel Enhancement–Mode Silicon Gate

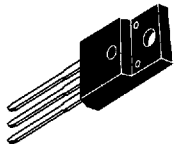
MTA30N06E
Motorola Preferred Device

TMOS POWER FET
30 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.025 OHM MAX

This advanced TMOS E–FET is designed to withstand high energy in the avalanche mode and operate reliably. This new high energy device also offers a drain–to–source diode with fast recovery time. The device is designed for high speed switching applications such as switching power supplies, PWM motor controls and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients. The device is housed in a fully isolated TO–220 package which has an isolation voltage rating of up to 4500 Volts.

- Avalanche Energy Specified
- Low Stored Gate Charge for Efficient Switching
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode
- Isolated Version of the MTP50N06E





CASE 221D–02, Style 1
(ISOLATED TO–220 TYPE)

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Volts
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Volts
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Volts
Drain Current — Continuous — Continuous @ 100°C — Pulsed	I_D I_D I_{DM}	30 20 160	Amps
RMS Isolation Voltage (t = 1 second, R.H. ≤ 30%, T_A = 25°C) Per Figure 18 Per Figure 19 Per Figure 20	V_{ISO1} V_{ISO2} V_{ISO3}	4500 3500 1500	Volts
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, Peak I_L = 30 A, L = 889 μH, R_G = 25 Ω)	E_{AS}	400	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)		—	65	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 V, V_{GS} = 0, T_J = 125°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Threshold Temperature Coefficient (negative)		—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 25 Adc)	$R_{DS(on)}$	—	0.017	0.025	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 50 Adc)	$V_{DS(on)}$	—	—	1.6	Vdc
(I_D = 25 Adc, T_J = 100°C)		—	—	1.2	
Forward Transconductance (V_{DS} ≥ 8.0 Vdc, I_D = 25 Adc)	g_{FS}	17	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	2500	3500	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	1000	1400	
Transfer Capacitance	C_{rss}	—	250	500	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	$t_{d(on)}$	—	23	46	ns
Rise Time (V_{DD} = 25 V, I_D = 50 A, V_{GS} = 10 V, R_G = 9.1 Ω)	t_r	—	160	320	
Turn–Off Delay Time	$t_{d(off)}$	—	70	140	
Fall Time	t_f	—	120	240	
Gate Charge	Q_T	—	75	100	nC
(V_{DS} = 48 V, I_D = 50 A, V_{GS} = 10 V)	Q_1	—	15		
	Q_2	—	45	—	
	Q_3	—	30	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (I_S = 50 A, V_{GS} = 0)	V_{SD}	—	1.1	2.5	Vdc
(I_S = 50 A, V_{GS} = 0, T_J = 125°C)		—	1.0	—	
Reverse Recovery Time (I_S = 25 A, di/dt = 100 A/μs)	t_{rr}	—	120	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die)	L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	
ISOLATION CAPACITANCE					
Isolation Capacitance, Drain–to–Heat Sink	C_{iso}	—	15	—	pF

(1) Pulse Test: Pulse Width ≤ 300 μs max, Duty Cycle = 2.0%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

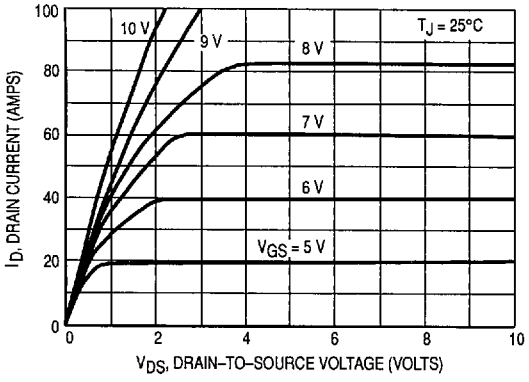

Figure 1. On–Region Characteristics

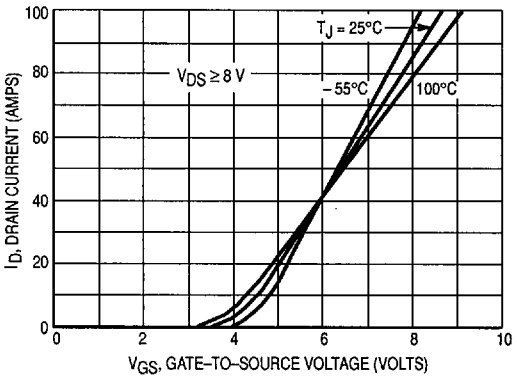

Figure 2. Transfer Characteristics

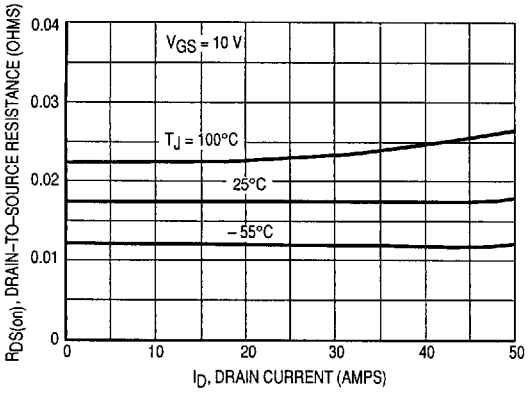

Figure 3. On–Resistance versus Drain Current

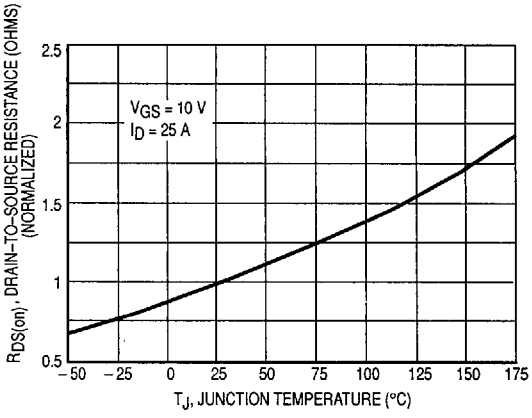

Figure 4. On–Resistance Variation With Temperature

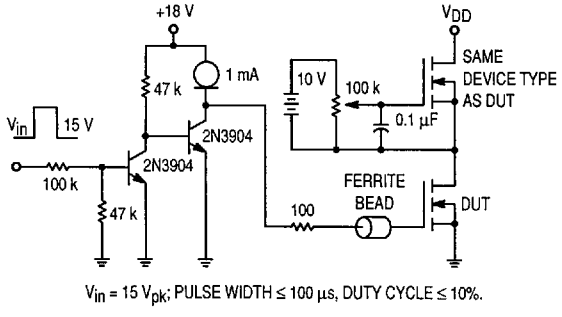

Figure 5. Gate Charge Test Circuit

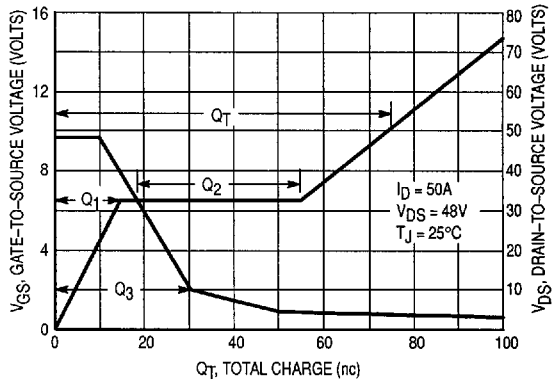

Figure 6. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

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SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA shown in Figure 9 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

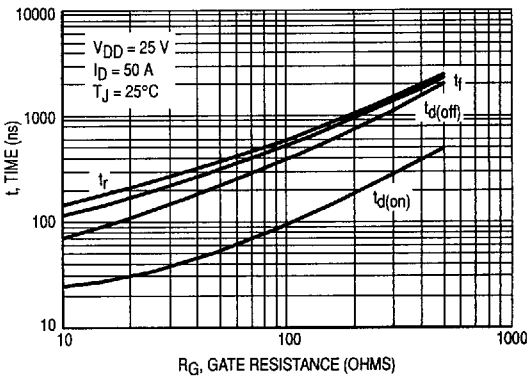

Figure 7. Resistive Switching Time Variation versus Gate Resistance

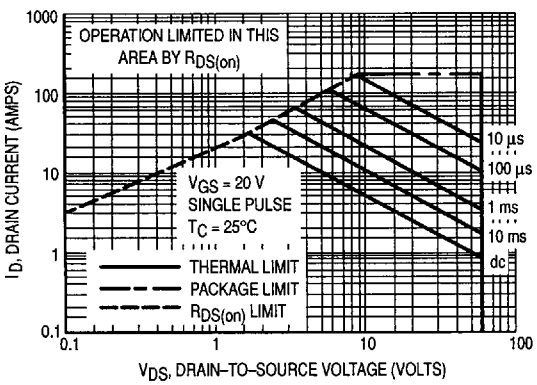

Figure 8. Maximum Rated Forward Biased Safe Operating Area

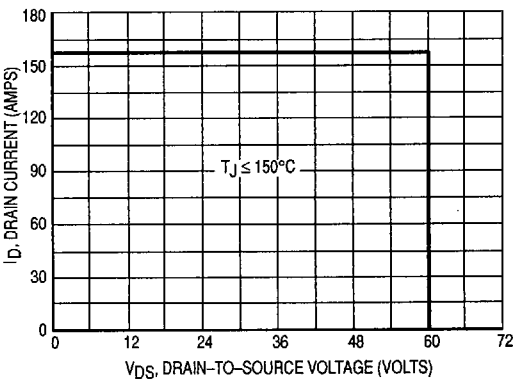

Figure 9. Maximum Rated Switching Safe Operating Area

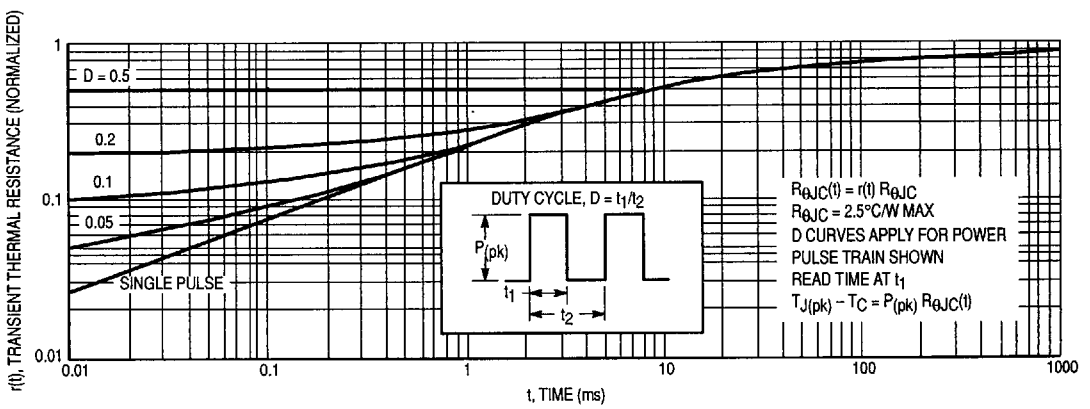

Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at rated $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

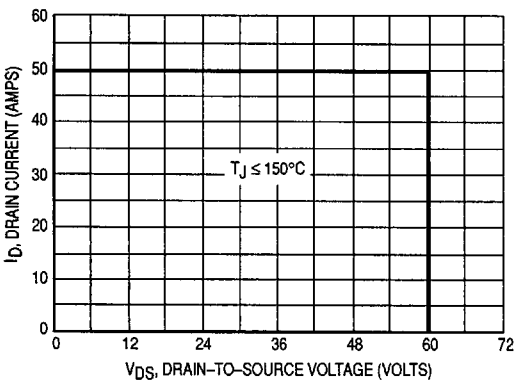

Figure 12. Commutating Safe Operating Area (CSOA)

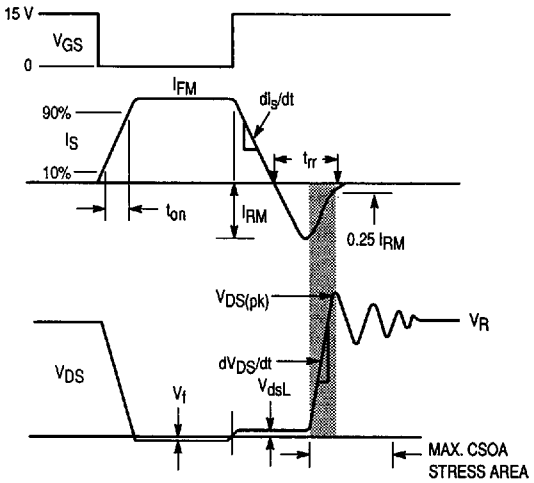

Figure 11. Commutating Waveforms

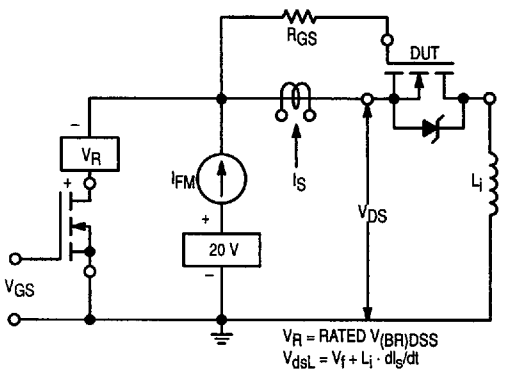

Figure 13. Commutating Safe Operating Area Test Circuit

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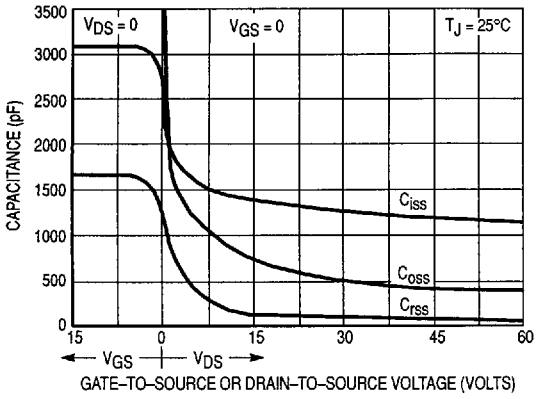

Figure 14. Capacitance Variation

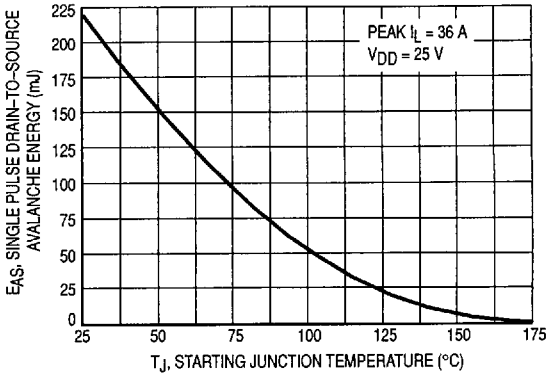

Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature

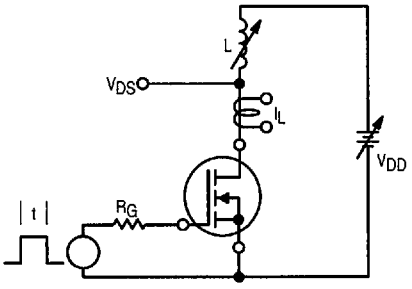

Figure 16. Unclamped Inductive Switching Test Circuit

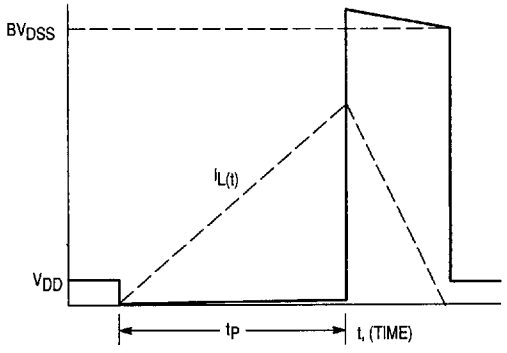

Figure 17. Unclamped Inductive Switching Waveforms

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TEST CONDITIONS FOR ISOLATION TESTS*

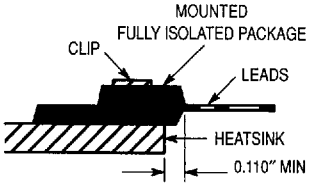


Figure 18. Clip Mounting Position for Isolation Test Number 1

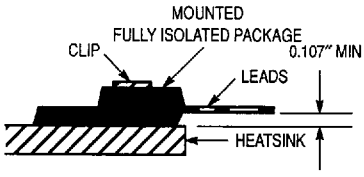


Figure 19. Clip Mounting Position for Isolation Test Number 2

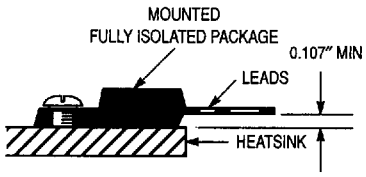
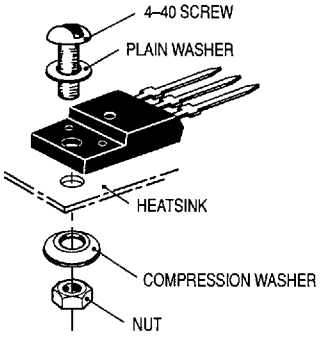


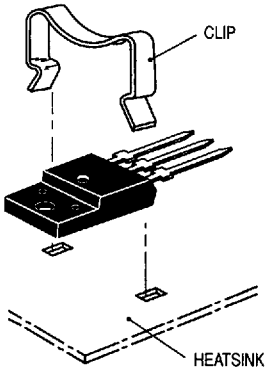
Figure 20. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**



21a. Screw–Mounted



21b. Clip–Mounted

Figure 21. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in • lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in • lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in • lbs without adversely affecting the package. However, in order to positively insure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in • lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

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