

841A•841B

T-46-07-12



# 74FCT841A•74FCT841B

## 10-Bit Transparent Latch with TRI-STATE® Outputs

### General Description

The bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841A/B is a 10-bit transparent latch, a 10-bit version of the 'FCT373A.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

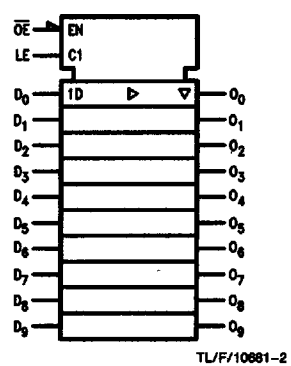
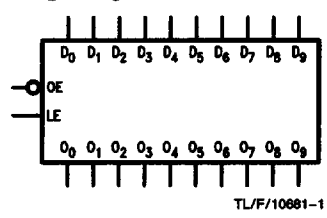
FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

### Features

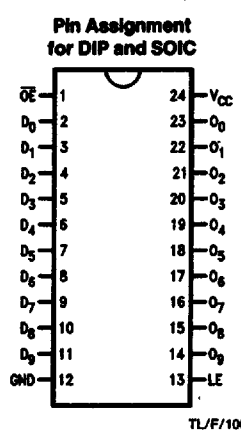
- NSC 74FCT841A/B is pin and functionally equivalent to IDT 74FCT841A/B
- High Speed parallel latches
- Buffered common latch enable
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- $I_{OL} = 48 \text{ mA (com)}$
- CMOS power levels
- 4 kV minimum ESD immunity

**Ordering Code:** See Section 8

### Logic Symbols



### Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>9</sub>	Data Inputs
O <sub>0</sub> -O <sub>9</sub>	TRI-STATE Outputs
OE	Output Enable
LE	Latch Enable

### Functional Description

The 'FCT841A/B consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

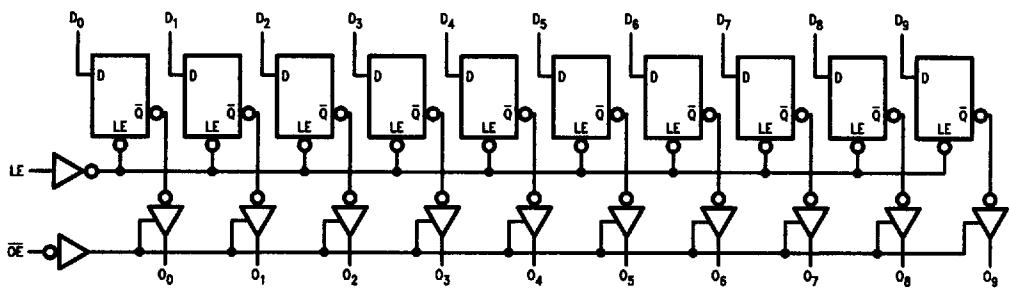
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
A	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 NC = No Change

### Logic Diagram



TL/F/10681-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND ( $V_{TERM}$ )	
74FCTA/B	-0.5V to +7.0V
Temperature under Bias ( $T_{BIAS}$ )	
74FCTA/B	-55°C to +125°C
Storage Temperature ( $T_{STG}$ )	
74FCTA/B	-55°C to +125°C
DC Output Current ( $I_{OUT}$ )	120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum ratings conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	4.75V to 5.25V
74FCTA/B	
Input Voltage	0V to $V_{CC}$
Output Voltage	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74FCTA/B	-0°C to +70°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

### DC Characteristics for 'FCTA/B Family Devices

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	74FCTA/B			Units	Conditions	
		Min	Typ	Max			
$V_{IH}$	Minimum High Level Input Voltage	2.0			V		
$V_{IL}$	Maximum Low Level Input Voltage			0.8	V		
$I_{IH}$	Input High Current			5.0 5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
$I_{IL}$	Input Low Current			-5.0 -5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = \text{GND}$
$I_{OZ}$	Maximum TRI-STATE Current			10.0 10.0 -10.0 -10.0	$\mu A$	$V_{CC} = \text{Max}$	$V_O = V_{CC}$ $V_O = 2.7V$ (Note 2) $V_O = 0.5V$ (Note 2) $V_O = \text{GND}$
$V_{IK}$	Clamp Diode Voltage	-0.7	-1.2		V	$V_{CC} = \text{Min}; I_{IN} = -18 \text{ mA}$	
$I_{OS}$	Short Circuit Current	-75	-120		mA	$V_{CC} = \text{Max}$ (Note 1) $V_O = \text{GND}$	
$V_{OH}$	Minimum High Level Output Voltage	2.8 $V_{HC}$ 2.4 2.4	3.0 $V_{CC}$ 4.3 4.3		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = -32 \mu A$ $V_{CC} = \text{Min}; V_{IN} = V_{IH}$ or $V_{IL}; I_{OL} = -24 \text{ mA}$ (Com)	
$V_{OL}$	Maximum Low Level Output Voltage	GND GND	0.2 0.2 0.3 0.5		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = 300 \mu A$ $V_{CC} = \text{Min}; V_{IN} = V_{IH}$ or $V_{IL}; I_{OH} = 300 \mu A; I_{OL} = 48 \text{ mA}$ (Com)	
$I_{CC}$	Maximum Quiescent Supply Current		0.2	1.5	mA	$V_{CC} = \text{Max}; V_{IN} \geq V_{HC}; V_{IN} \leq 0.2V; f_I = 0$	
$\Delta I_{CC}$	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}; V_{IN} = 3.4V$ (Note 3)	
$I_{CCD}$	Dynamic Power Supply Current (Note 4)			0.50	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open $OE = \text{GND}$ $LE = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

### DC Characteristics for 'FCTA/B Family Devices

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ;  $V_{OH} = V_{CC} - 0.2V$  (Continued)

Symbol	Parameter	74FCTA/B			Units	Conditions	
		Min	Typ	Max			
$I_C$	Total Power Supply Current (Note 6)			5.5	mA	$V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$ $LE = V_{CC}$ $f_i = 10 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				6.0			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$
				9.0		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$ $LE = V_{CC}$ $f_i = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				14.5			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$

**Note 1:** Maximum test duration not to exceed one second, not more than one output shorted at one time.

**Note 2:** This parameter is guaranteed but not tested.

**Note 3:** Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

**Note 4:** This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

**Note 5:** Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

**Note 6:**  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_T$  = Number of Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Input Frequency

$N_i$  = Number of Inputs at  $f_i$

All currents are in milliamperes and all frequencies are in megahertz.

### AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	Test Conditions	74FCTA		74FCTB		Units	Fig. No.
			$T_A, V_{CC} = \text{Com}$		$T_A, V_{CC} = \text{Com}$			
			Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Dn to Qn (LE = High)	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$		9.0		6.5	ns	2-9
$t_{PLH}$ $t_{PHL}$	Propagation Delay Dn to Qn (LE = High)	$C_L = 300 \text{ pF}$ (Note 1) $R_L = 500\Omega$		13.0		13.0	ns	2-9
$t_{SU}$	Data to LE Setup Time	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	2.5		2.5		ns	2-10
$t_H$	Data to LE Hold Time	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	2.5		2.5		ns	2-10
$t_{PHL}$ $t_{PLH}$	Propagation Delay LE to On	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$		12.0		8.0	ns	2-9
		$C_L = 300 \text{ pF}$ (Note 1) $R_L = 500\Omega$		16.0		15.5	ns	2-9
$t_W$	LE Pulse Width High	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	4.0		4.0		ns	2-9

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**AC Electrical Characteristics:** See Section 2 for Waveforms (Continued)

Symbol	Parameter	Test Conditions	74FCTA		74FCTB		Units	Fig. No.
			$T_A, V_{CC} = \text{Com}$		$T_A, V_{CC} = \text{Com}$			
			Min	Max	Min	Max		
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time (OE to On)	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω		11.5		8.0	ns	2-11
		C <sub>L</sub> = 300 pF (Note 1) R <sub>L</sub> = 500Ω		23.0		14.0	ns	2-11
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time (OE to On)	C <sub>L</sub> = 5 pF (Note 1) R <sub>L</sub> = 500Ω		7.0		6.0	ns	2-11
		C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω		8.0		7.0	ns	2-11

Note 1: These parameters are guaranteed but not tested.

**Capacitance** T<sub>A</sub> = +25°C, f = 1.0 MHz

Symbol	Parameter (Note 1)	Conditions	Typ	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

Note 1: This parameter is measured at characterization but not tested.