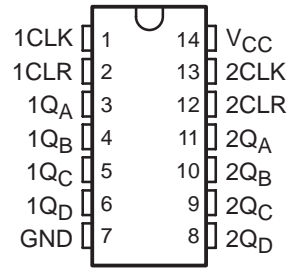


# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

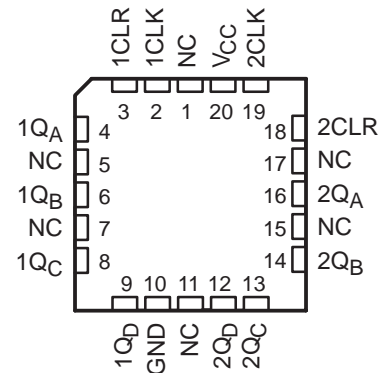
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 13$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Dual 4-Bit Binary Counters With Individual Clocks
- Direct Clear for Each 4-Bit Counter
- Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent

SN54HC393 . . . J OR W PACKAGE  
SN74HC393 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC393 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HC393 devices contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. These devices comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock (CLK) input. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'HC393 devices have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC393N	SN74HC393N
	SOIC – D	Tube of 50	SN74HC393D	HC393
		Reel of 2500	SN74HC393DR	
		Reel of 250	SN74HC393DT	
	SOP – NS	Reel of 2000	SN74HC393NSR	HC393
	SSOP – DB	Reel of 2000	SN74HC393DBR	HC393
	TSSOP – PW	Tube of 90	SN74HC393PW	HC393
Reel of 2000		SN74HC393PWR		
Reel of 250		SN74HC393PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC393J	SNJ54HC393J
	CFP – W	Tube of 150	SNJ54HC393W	SNJ54HC393W
	LCCC – FK	Tube of 55	SNJ54HC393FK	SNJ54HC393FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

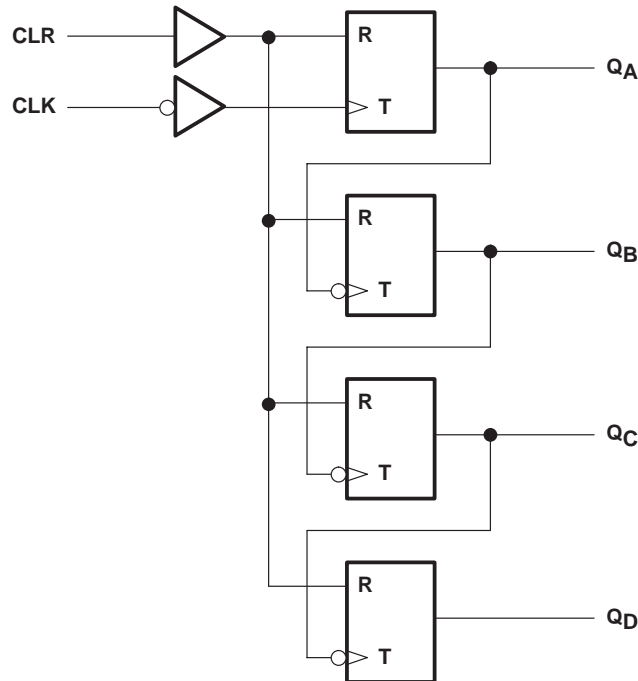
# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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FUNCTION TABLE COUNT SEQUENCE  
(each counter)

COUNT	OUTPUTS			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

logic diagram, each counter (positive logic)



# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	86°C/W
DB package .....	96°C/W
N package .....	80°C/W
NS package .....	76°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54HC393			SN74HC393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V			0.5	$V_{CC} = 2$ V		0.5
		$V_{CC} = 4.5$ V			1.35	$V_{CC} = 4.5$ V		1.35
		$V_{CC} = 6$ V			1.8	$V_{CC} = 6$ V		1.8
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$ †	Input transition rise/fall time	$V_{CC} = 2$ V			1000	$V_{CC} = 2$ V		1000
		$V_{CC} = 4.5$ V			500	$V_{CC} = 4.5$ V		500
		$V_{CC} = 6$ V			400	$V_{CC} = 6$ V		400
$T_A$	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

† If this device is used in the threshold region (from  $V_{ILmax} = 0.5$  V to  $V_{IHmin} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_f = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC393		SN74HC393		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		6		4.2		5	MHz
		4.5 V		31		21		25	
		6 V		36		25		28	
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80		120		100	ns
			4.5 V	16		24		20	
			6 V	14		20		18	
		CLR high	2 V	80		120		100	
			4.5 V	16		24		20	
			6 V	14		20		18	
t <sub>su</sub>	Setup time, CLR inactive	2 V		25		25		25	ns
		4.5 V		5		5		5	
		6 V		5		5		5	



# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLK	Q <sub>A</sub>	2 V	6	10		4.2		5	MHz	
			4.5 V	31	50		21		25		
			6 V	36	60		25		28		
t <sub>pd</sub>	CLK	Q <sub>A</sub>	2 V		50	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		13	20		31		26	
		Q <sub>B</sub>	2 V		72	190		285		240	
			4.5 V		22	38		57		47	
			6 V		18	32		48		40	
		Q <sub>C</sub>	2 V		91	240		360		300	
			4.5 V		28	48		72		60	
			6 V		22	41		61		51	
		Q <sub>D</sub>	2 V		100	290		430		360	
			4.5 V		32	58		87		72	
			6 V		24	50		74		62	
t <sub>PHL</sub>	CLR	Any	2 V		45	165		250		205	ns
			4.5 V		17	33		49		41	
			6 V		14	28		42		35	
t <sub>t</sub>		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

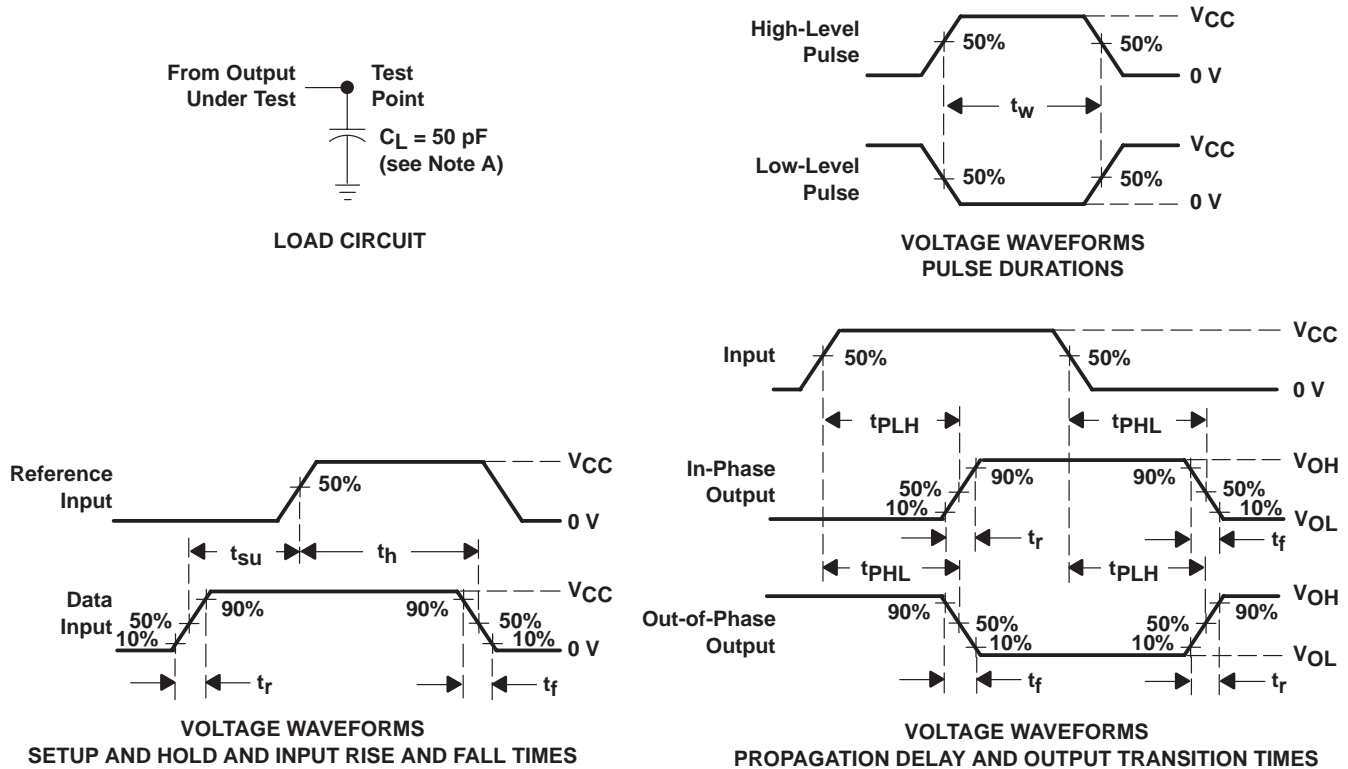
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per counter	No load	40	pF

# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84100012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84100012A SNJ54HC 393FK	<a href="#">Samples</a>
8410001CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8410001CA SNJ54HC393J	<a href="#">Samples</a>
8410001DA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8410001DA SNJ54HC393W	<a href="#">Samples</a>
JM38510/66309BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 66309BCA	<a href="#">Samples</a>
M38510/66309BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 66309BCA	<a href="#">Samples</a>
SN54HC393J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54HC393J	<a href="#">Samples</a>
SN74HC393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC393N	<a href="#">Samples</a>
SN74HC393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SN74HC393PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC393PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	<a href="#">Samples</a>
SNJ54HC393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84100012A SNJ54HC 393FK	<a href="#">Samples</a>
SNJ54HC393J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8410001CA SNJ54HC393J	<a href="#">Samples</a>
SNJ54HC393W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8410001DA SNJ54HC393W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC393, SN74HC393 :**

- Catalog: [SN74HC393](#)
- Military: [SN54HC393](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC393DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC393DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC393DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC393PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC393PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

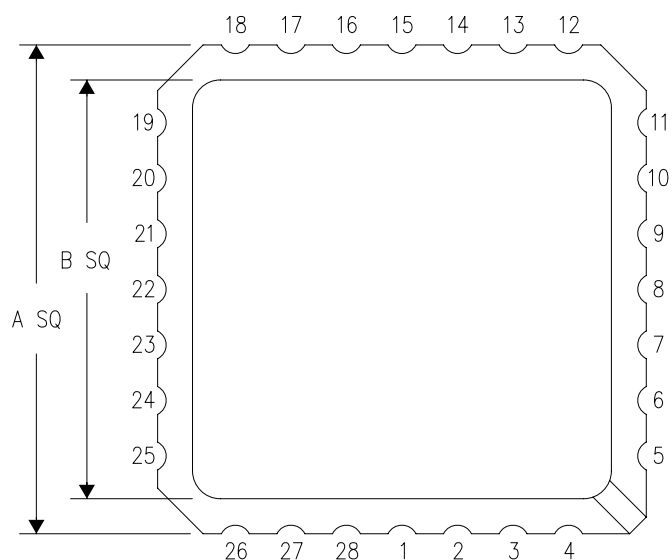

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC393DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC393DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC393DT	SOIC	D	14	250	210.0	185.0	35.0
SN74HC393PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC393PWT	TSSOP	PW	14	250	367.0	367.0	35.0

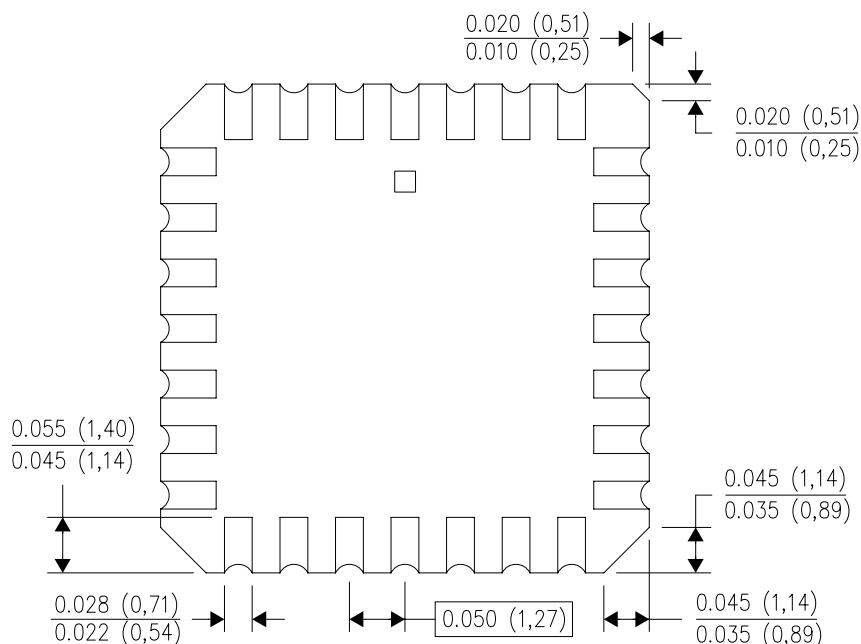
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

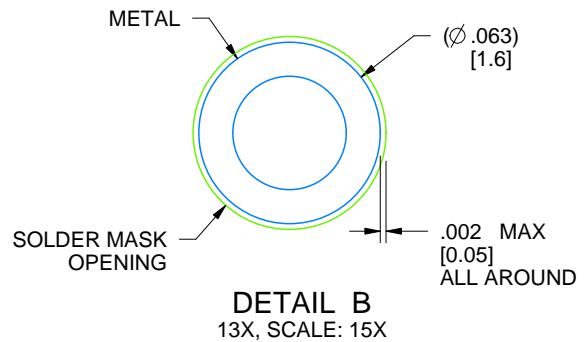
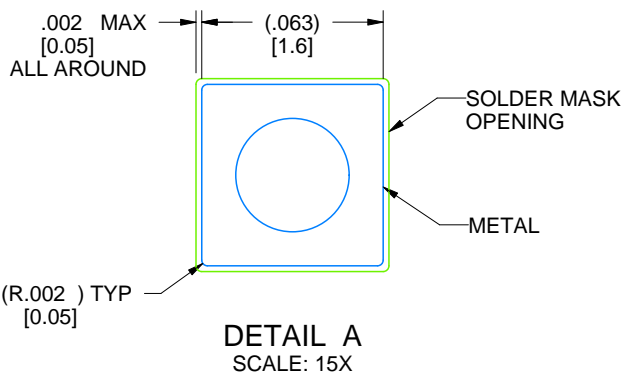
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



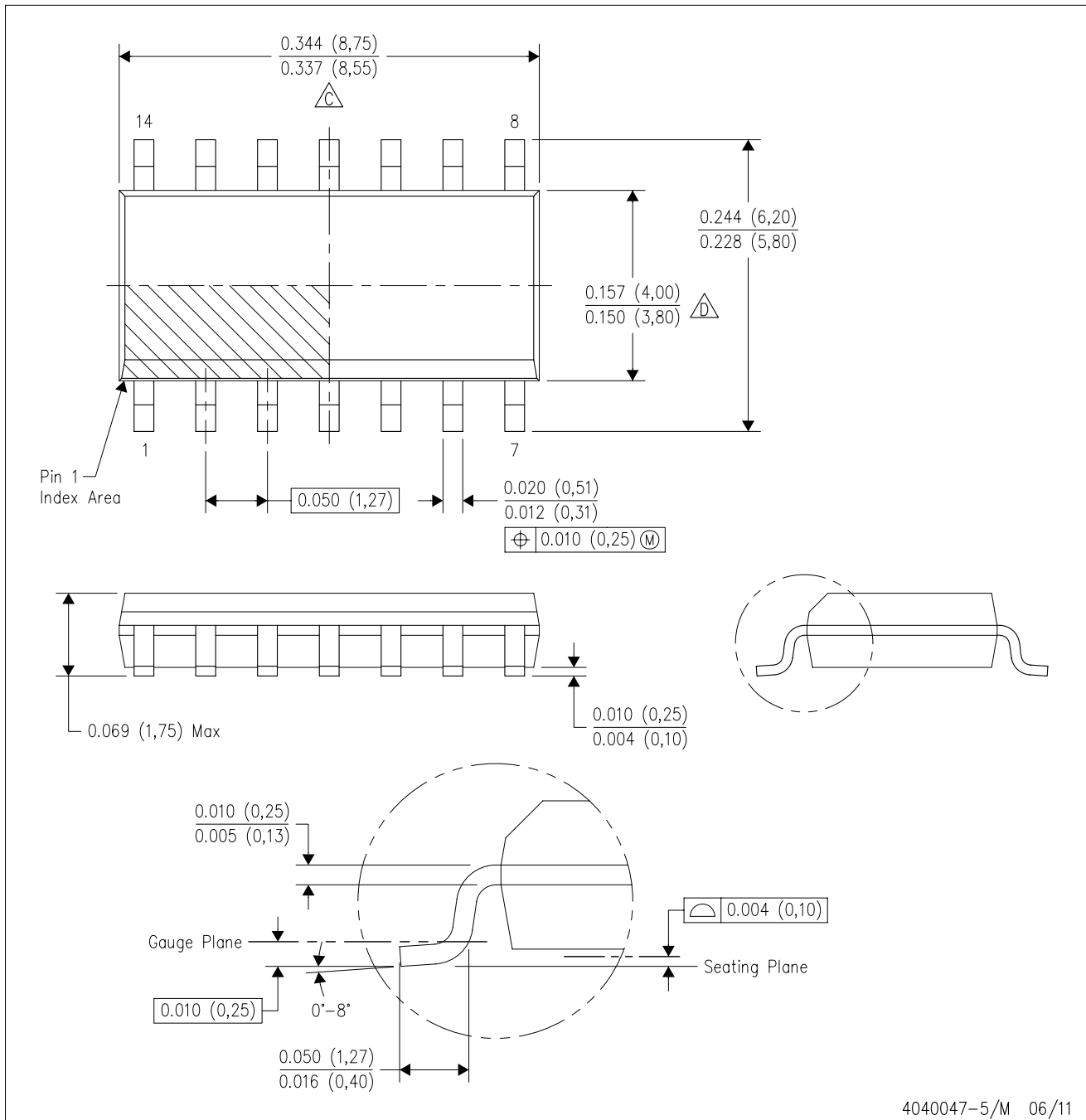
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X





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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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