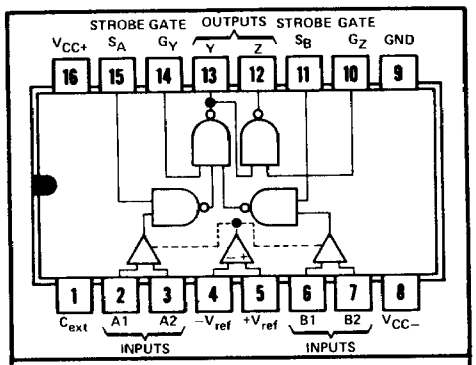
FUNCTION TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\bar{G}_Z$
H	X	X	X	H	X	H	$\bar{G}_Z$
X	H	X	X	X	H	H	$\bar{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \bar{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \bar{G}_Z + \overline{Y}$

$Z = \bar{G}_Z + G_Y(\bar{A} + \bar{S}_A)(\bar{B} + \bar{S}_B)$

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics (unless otherwise noted V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Differential input threshold voltage (see Note 3)	1	V_{ref} = 15 mV	SN7520	11	15	19	mV
				SN7521	8	15	22	
			V_{ref} = 40 mV	SN7520	36	40	44	
				SN7521	33	40	47	
V_{ICF}	Common-mode input firing voltage (see Note 4)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq$ 15 ns, $t_f \leq$ 15 ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3			2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3					0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

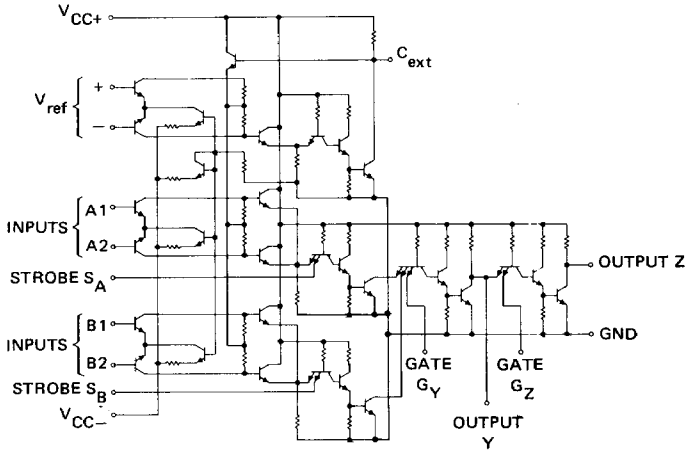
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	32	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	32	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	32	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	33	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	33	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	34	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$						10	20	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



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