General Information

The Advanced CMOS Frame Aligner (ACFA) PEB 2035 is a VLSI device used in interface modules with PCM systems.

Designed as an universal frame aligner, the ACFA will implement layer-1 (coding, decoding and synchronizing) functions for all PCM30 (32 channels) and PCM24 (24 channels) oriented applications. It complies with CCITT/ CEPT recommendations as well as with the AT&T DMI specifications (CCITT Rec. G 703, 704, 732, 733, November 1984; DMI specification April 1985).

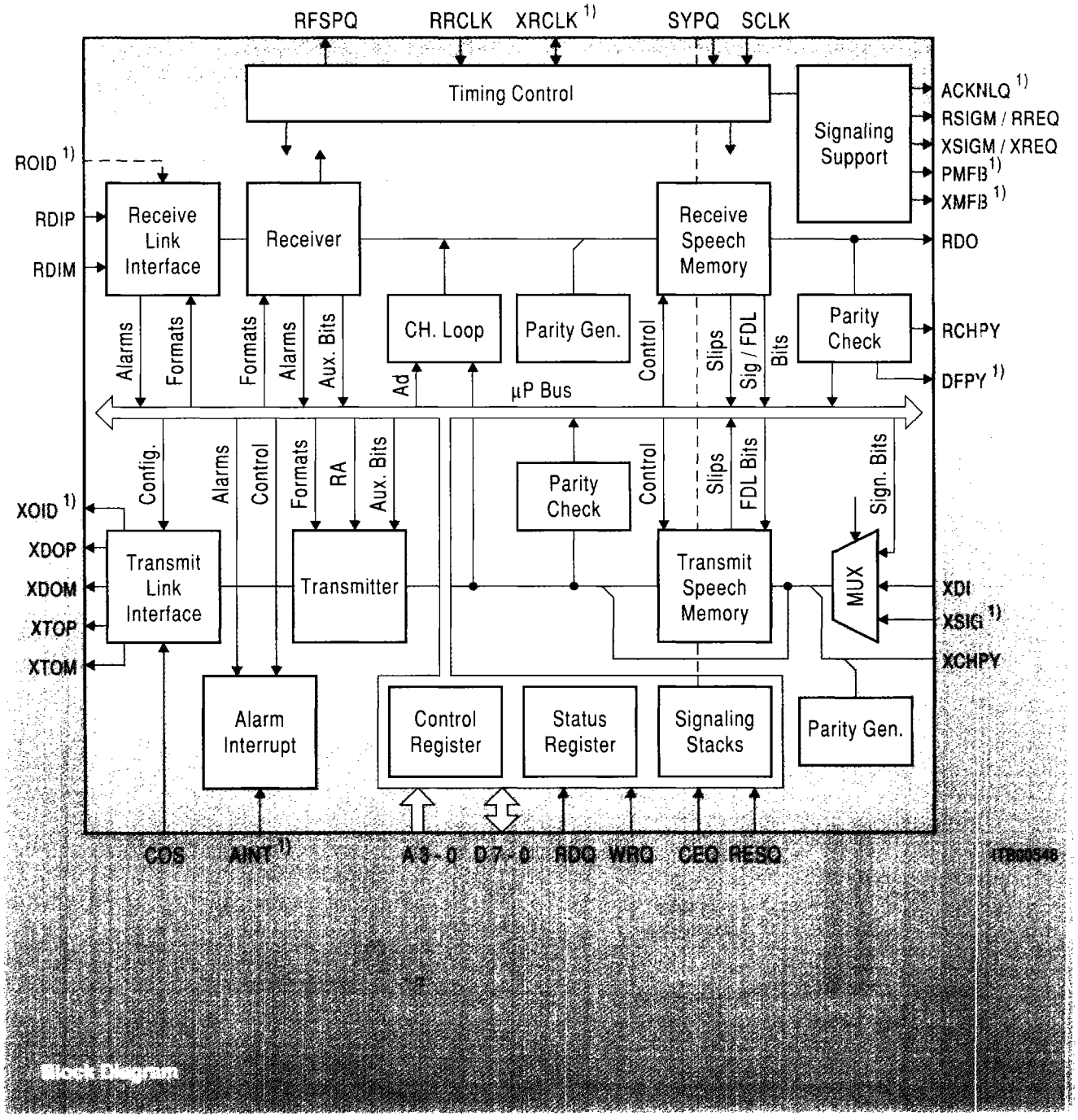
Switching between the PCM24 and the PCM30 modes is performed by programming via the microprocessor interface of the device. The extended features implemented in each of these two modes will meet most present and future requirements. A high degree of flexibility allows its use without addition of specialized hardware.

Besides interfacing to T1/CEPT routes and to an internal system highway, the ACFA supports the following interfaces:
– interface with fiber-optic transmission routes
– parallel microprocessor interface
– interface to support different signaling schemes
– testing and diagnostic interface

Type	Package
PEB 2035-N	P-LCC-44-1 (SMD)
PEB 2035-P	P-DIP-40-1
PEF 2035-N	P-LCC-44-1 (SMD)
PEF 2035-P	P-DIP-40-1

Features

- Frame alignment for 2.048-Mbit/s and 1.544 Mbit/s PCM system
- Meets CCITT Rec's (G 703, 704, 732, 733) and AT&T technical advisories
- Coding/decoding for HDB3, B8ZS and AMI-ZCS (zero code suppression) line codes
- Clear channel capability for AMI ZCS and CAS-BR
- Unipolar NRZ for interfacing fiber-optic transmission routes
- Error checking via CRC4 or CRC6
- Interfacing with a system internal 2.048-Mbit/s or 4.096-Mbit/s highway
- Elastic memory for route clock wander and jitter compensation
- Support for different signaling schemes
- Testing and diagnostics
- Single +5-V power supply
- Advanced CMOS technology
- Low power consumption


RFSPQ
RRCLK
XRCLK 1)
SYPQ
SCLK
Timing Control
Signaling Support
ACKNLQ 1)
RSIGM / RREQ
XSIGM / XREQ
PMFB 1)
XMFB 1)
ROID 1)
RDIP
RDIM
Receive Link Interface
Receiver
Receive Speech Memory
RDO
Alarms
Formats
Formats
Alarms
Aux. Bits
CH. Loop
Parity Gen.
Control
Slips
Sig / FDL
Bits
Parity Check
RCHPY
DFPY 1)
Ad
µP Bus
Config.
Alarms
Control
Formats
RA
Aux. Bits
Parity Check
Control
Slips
FDL Bits
Sign. Bits
XOID 1)
XDOP
XDOM
XTOP
XTOM
Transmit Link Interface
Transmitter
Transmit Speech Memory
MUX
XDI
XSIG 1)
XCHPY
Alarm Interrupt
Control Register
Status Register
Signaling Stacks
Parity Gen.
COS
AINT 1)
A3-0
D7-0
RDQ
WRQ
CEQ
RESQ
ITB00548
Block Diagram