SiT9367 Advanced Information

220 to 700 MHz Ultra-low Jitter Differential Oscillator

The Smart Timing Choice™

Features

- Any frequency between 220.000001 MHz and 700 MHz accurate to 6 decimal places
- LVPECL, LVDS and HCSL output signaling types
- 0.1ps RMS phase jitter (random) for Ethernet applications
- Frequency stability as low as ±10 ppm
- Wide temperature range from -40°C to 85°C
  Contact SiTime for higher temperature range options
- Industry-standard packages: 3.2x2.5, 7.0x5.0 mm
  Contact SiTime for 5.0 x 3.2 mm package

Applications

- 10/40GB Ethernet, SONET, SATA, SAS, Fibre Channel
- Telecom, networking, instrumentation, storage, servers

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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage

Table 1. Electrical Characteristics - Common to LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	220.000001	–	700	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_aging1	–	±1	–	ppm	At 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial. Contact SiTime for higher temperature range options
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 1, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Start-up Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	510	ns	f = 322.265652 MHz - For other frequencies, T_oe = 500ns + 3 period

Table 2. Electrical Characteristics - LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	84	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	55	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 2
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	250	–	ps	20% to 80%, see Figure 2
Jitter						
RMS Period Jitter[1]	T_jitt	–	1	2	ps	f = 322.265625 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.23	–	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdds

Notes:

1. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	76	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	55	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	450	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	–	340	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
Jitter						
RMS Period Jitter[2]	T_jitt	–	1	2	ps	f = 322.265625 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.23	–	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdds

Notes:

2. Measured according to JESD65B

Table 4. Electrical Characteristics – HCSL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	84	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	55	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Output High Voltage	VOH	0.6	–	0.8	V	See Figure 2
Output Low Voltage	VOL	-0.05	–	0.05	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1	1.4	1.8	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	350	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 2
Jitter						
RMS Period Jitter[3]	T_jitt	–	1	2	ps	f = 322.265625 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.23	–	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdds

Notes:

3. Measured according to JESD65B

Table 5. Pin Description

Pin	Map	Functionality	
1	OE/NC	Output Enable (OE)	H[4]: specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[5]

Notes:

4. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
5. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 pF capacitor between Vdd and GND is required for the best phase jitter performance

Top View

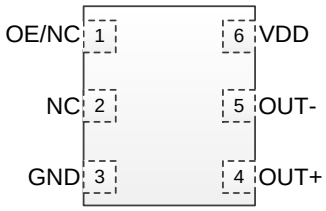


Figure 1. Pin Assignments

Table 6. Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge (HBM)	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Table 7. Thermal Consideration[6]

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
3225, 6-pin	TBD	TBD
7050, 6-pin	TBD	TBD

Notes:

6. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Table 8. Maximum Operating Junction Temperature[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80
85°C	95

Notes:

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Waveform Diagrams

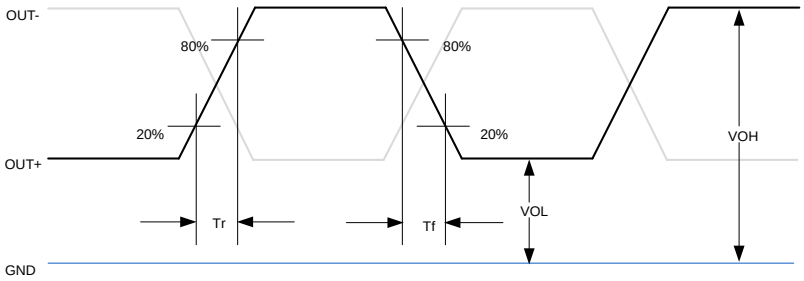


Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

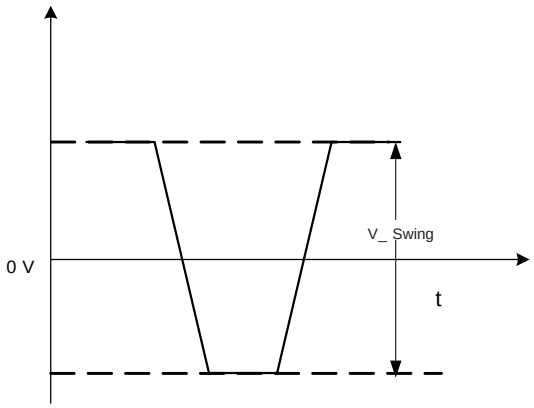


Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair

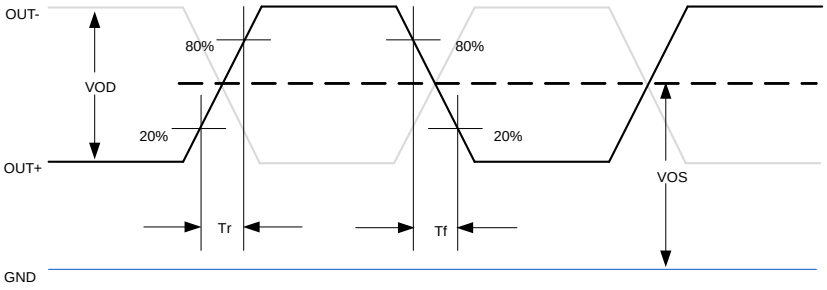


Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

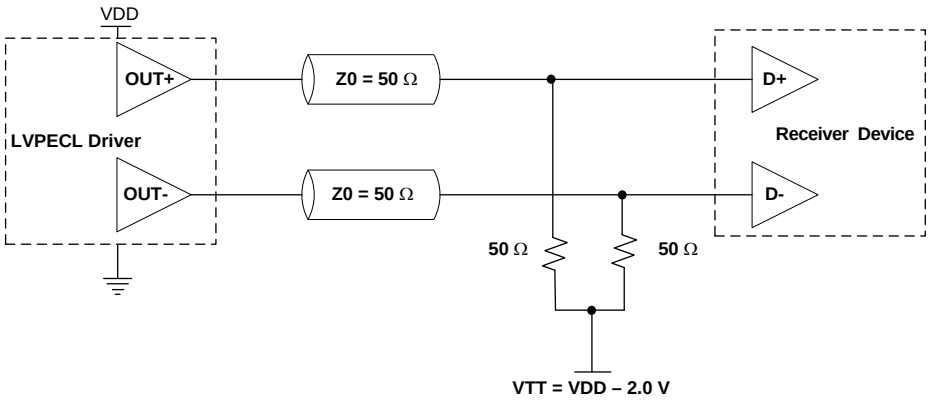


Figure 5. LVPECL Typical Termination

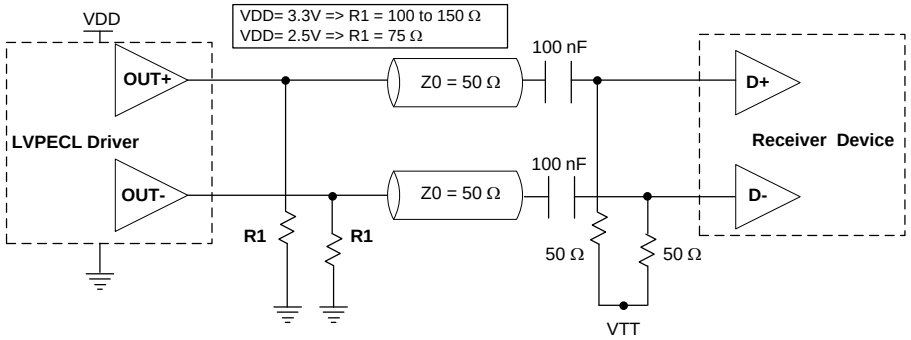


Figure 6. LVPECL AC Coupled Termination

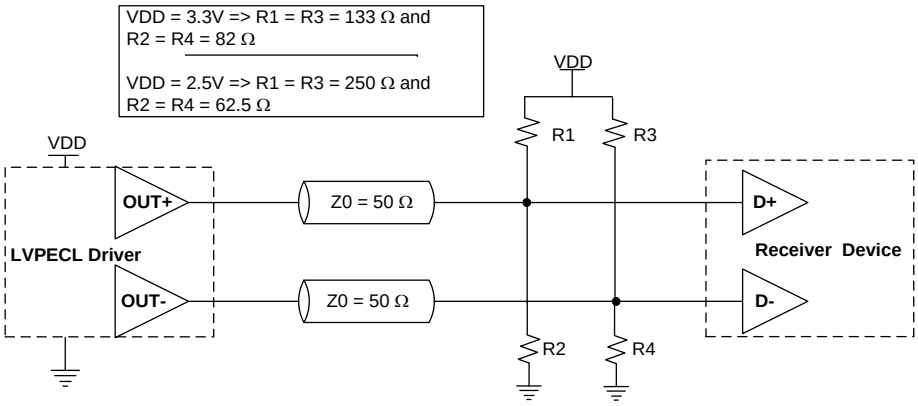


Figure 7. LVPECL with Thevenin Typical Termination

Termination Diagrams (Continued)

LVDS:

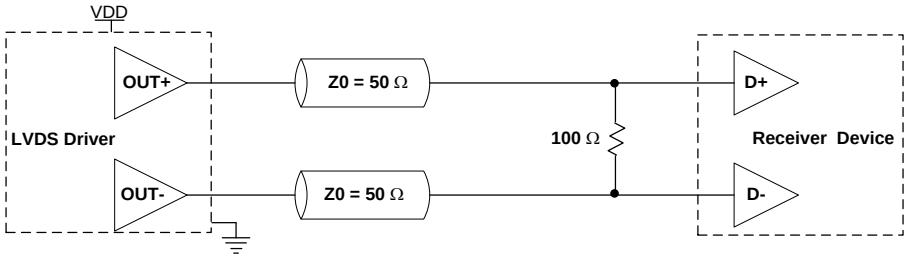


Figure 8. LVDS Single Termination (Load Terminated)

HCSL:

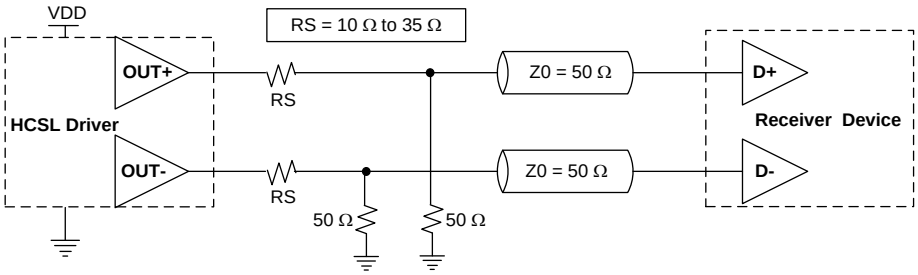
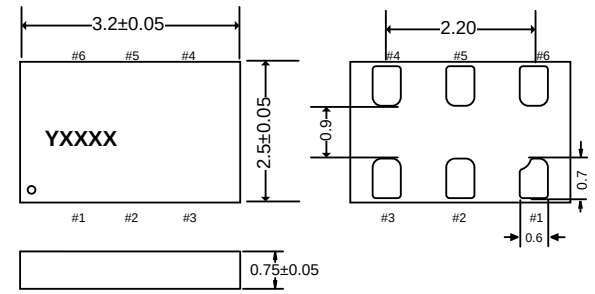
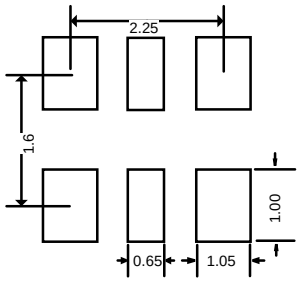
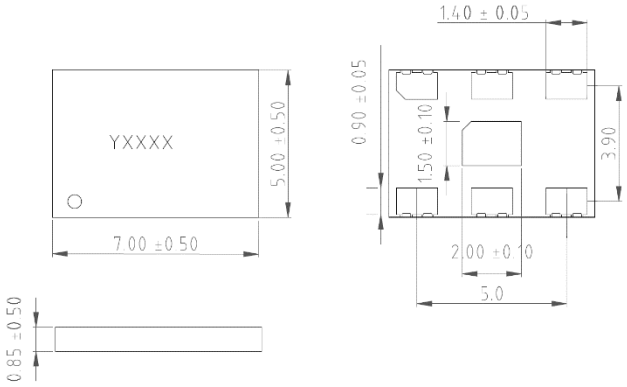
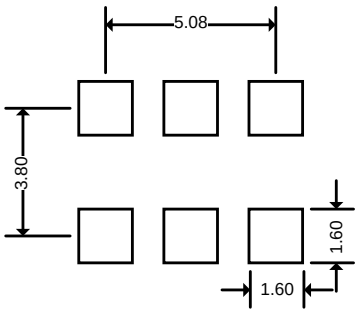


Figure 9. HCSL Typical Termination

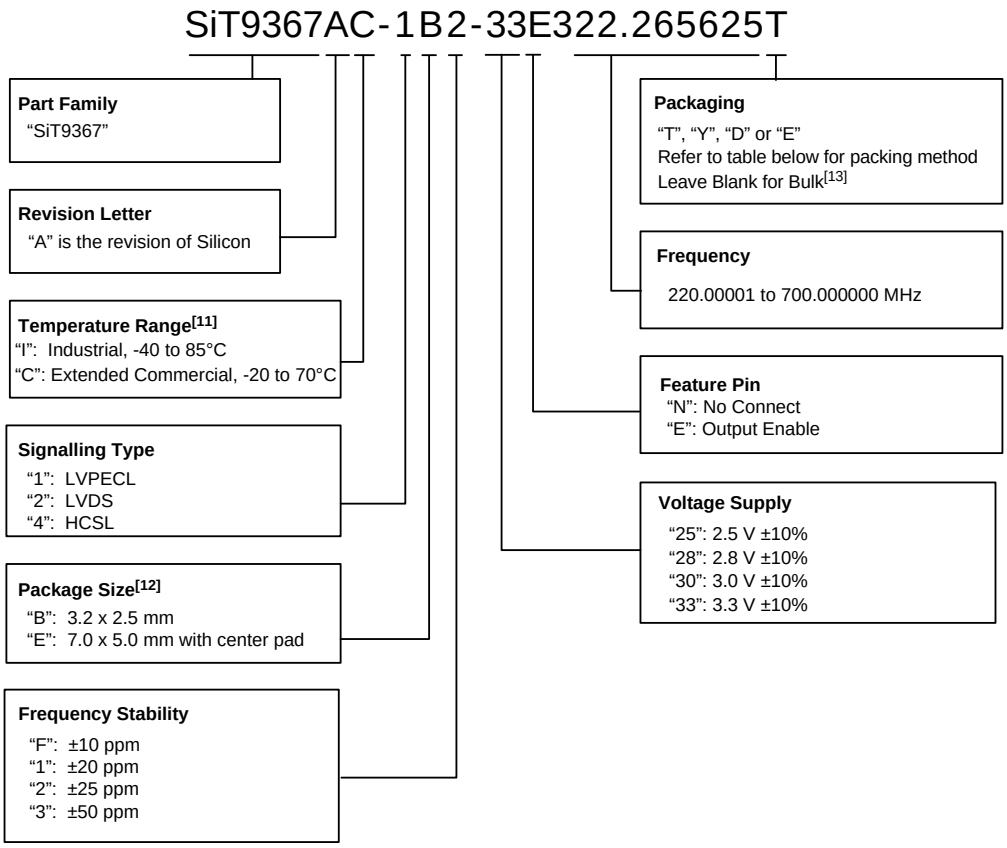
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[8]	Recommended Land Pattern (Unit: mm)[9]
3.2 x 2.5x 0.75 mm 	
7.0 x 5.0x 0.90 mm[10] 	

Notes:

8. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
9. A capacitor of value 0.1 µF or higher between Vdd and GND is required.
10. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information



Notes:

11. Contact SiTime for higher temperature range options
12. Contact SiTime for 5.0 x 3.2 package
13. Bulk is available for sampling only

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	T	Y	—	—

Table 11 .Revision History

Revision	Release Date	Change Summary
0.1	06/29/16	Initial draft
0.2	08/02/16	Revised T_jitt and T_phj values in electrical characteristics tables
0.21	08/25/16	Removed 5.0 x 3.2 mm package Revised the 12k -20 MHz phase jitter value
0.25	09/21/16	Revised the Electrical characteristics tables Revised 7050 package dimension