

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

December 1993

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
 - $I_{S(OFF)}$ 10pA
 - $I_{D(OFF)}$ 30pA
- Low Capacitance (Max)
 - $C_{S(OFF)}$ 10pF
 - $C_{D(OFF)}$ 25pF
- Off Isolation at 500kHz 55dB (Min)
- Low Charge Injection Error 20mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

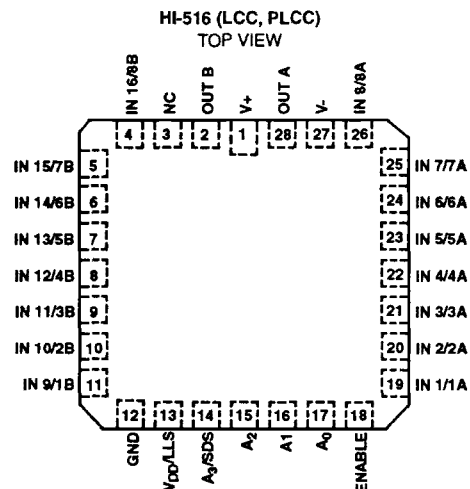
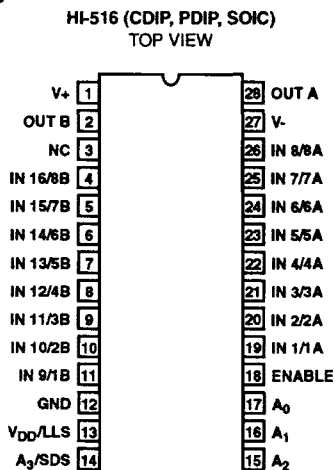
The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{DOFF} < 100pA$ at $+25^\circ C$) and fast settling ($t_{SETTLE} = 800ns$ to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

For MIL-STD-883 compliant parts, request the HI-516/883 data sheet.

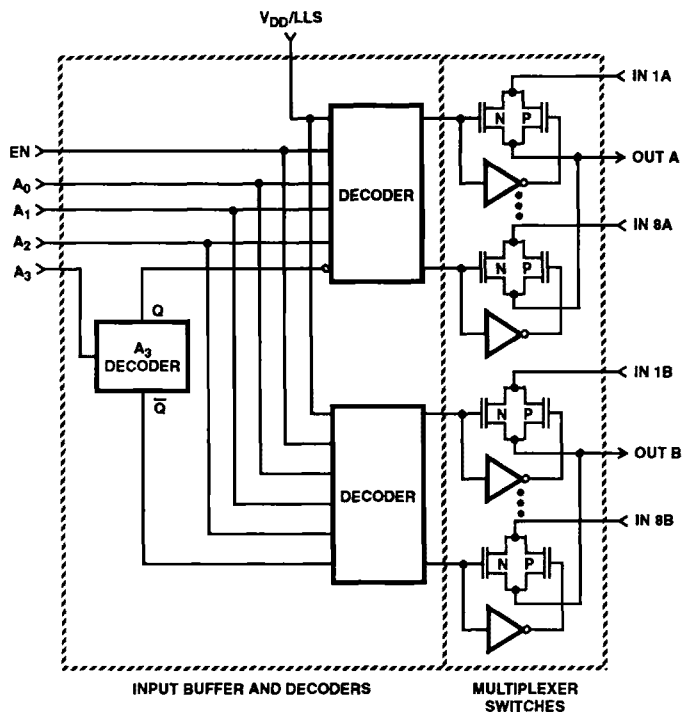
Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HI4P0516-5	0°C to +75°C	28 Lead PLCC
HI3-0516-5	0°C to +75°C	28 Lead Plastic DIP
HI1-0516-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0516-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0516-8	-55°C to +125°C	28 Lead Ceramic DIP
HI4-0516-8	-55°C to +125°C	28 Lead Ceramic LCC
HI9P0516-5	0°C to +75°C	28 Lead SOIC
HI9P0516-9	-40°C to +85°C	28 Lead SOIC
HI1-0516/883	-55°C to +125°C	28 Lead Ceramic DIP
HI4-0516/883	-55°C to +125°C	28 Lead Ceramic LCC

Pinouts



Functional Block Diagram



A ₃ DECODE		
A ₃	Q	\bar{Q}
H	H	L
L	L	H
V-	L	L

Specifications HI-516

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins	33V
Analog Input Voltage	
+V _{IN}	+V _{SUPPLY} +2V
-V _{IN}	-V _{SUPPLY} -2V
Digital Input Voltage	
TTL Levels Selected (V _{DD} /LLS Pin = GND or Open)	
+V _A	+6V
-V _A	-6V
+A ₃ /SDS	+V _{SUPPLY} +2V
-A ₃ /SDS	-V _{SUPPLY} -2V
CMOS Levels Selected (V _{DD} /LLS Pin = V _{DD})	
+V _A	+V _{SUPPLY} +2V
-V _A	-2V
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10s)	+300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	60°C/W	-
Plastic SOIC Package	70°C/W	-
Plastic PLCC Package	70°C/W	-
Ceramic DIP Package	50°C/W	18°C/W
Ceramic LCC Package	60°C/W	8°C/W
Junction Temperature		
Ceramic DIP, Ceramic LCC	+175°C	
Plastic DIP, Plastic SOIC, Plastic PLCC	+150°C	
Operating Temperature Ranges		
HI-516-2,-8	-55°C to +125°C	
HI-516-5	0°C to +75°C	
HI-516-9	-40°C to +85°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-516-2, -8			HI-516-5, -9			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
ANALOG CHANNEL CHARACTERISTICS										
Analog Signal Range, V _I	Note 2	Full	-14	-	+14	-15	-	+15	V	
On Resistance, R _{ON}	Note 3	+25°C	-	620	750	-	620	750	Ω	
		Full	-	-	1,000	-	-	1,000	Ω	
Off Input Leakage Current, I _{S(OFF)}		+25°C	-	0.01	-	-	0.01	-	nA	
		Full	-	-	50	-	-	50	nA	
Off Output Leakage Current, I _{D(OFF)}		+25°C	-	0.03	-	-	0.03	-	nA	
		Full	-	-	100	-	-	100	nA	
On Channel Leakage Current, I _{D(ON)}		+25°C	-	0.04	-	-	0.04	-	nA	
		Full	-	-	100	-	-	100	nA	
DIGITAL INPUT CHARACTERISTICS										
Input Low Threshold, V _{AL} (TTL)		Full	-	-	0.8	-	-	0.8	V	
Input High Threshold, V _{AH} (TTL)		Full	2.4	-	-	2.4	-	-	V	
Input Low Threshold, V _{AL} (CMOS)		Full	-	-	0.3V _{DD}	-	-	0.3V _{DD}	V	
Input High Threshold, V _{AH} (CMOS)		Full	0.7V _{DD}	-	-	0.7V _{DD}	-	-	V	
Input Leakage Current, I _{AH} (High)		Full	-	-	1	-	-	1	μ A	
Current, I _{AL} (Low)		Full	-	-	25	-	-	25	μ A	
SWITCHING CHARACTERISTICS										
Access Time, t _A		+25°C	-	130	175	-	130	175	ns	
		Full	-	-	225	-	-	225	ns	
Break-Before-Make Delay, t _{OPEN}		+25°C	10	20	-	10	20	-	ns	
Enable Delay (ON), t _{ON(EN)}		+25°C	-	120	175	-	120	175	ns	
Enable Delay (OFF), t _{OFF(EN)}		+25°C	-	140	175	-	140	175	ns	
Settling Time		+25°C	-	250	-	-	250	-	ns	
										0.1%
										0.01%
Charge Injection Error	Note 4	+25°C	-	-	20	-	-	20	mV	

Specifications HI-516

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; $V_{DD}/LLS = GND$.
(Note 1) Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP	HI-516-2, -8			HI-516-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS (Continued)									
Off Isolation	Note 5	+25°C	55	-	-	55	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	-	10	-	-	10	pF
Channel Output Capacitance, $C_{D(OFF)}$		+25°C	-	-	25	-	-	25	pF
Digital Input Capacitance, C_A		+25°C	-	-	10	-	-	10	pF
Input to Output Capacitance, $C_{DS(OFF)}$		+25°C	-	0.02	-	-	0.02	-	pF
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, PD		Full	-	-	750	-	-	900	mW
I+, Current	Note 6	Full	-	-	25	-	-	30	mA
I-, Current	Note 6	Full	-	-	25	-	-	30	mA

NOTES:

- V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
- At temperatures above +90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
- $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$.
- $V_{IN} = 0V$, $C_L = 100pF$, enable input pulse = 3V, $f = 500kHz$.
- $V_{EN} = 0.8V$, $V_S = 3V_{RMS}$, $f = 500kHz$, $C_L = 40pF$, $R_L = 1K$, Pin 3 grounded.
- $V_{EN} = +2.4V$.

TRUTH TABLE HI-516 Used as a 16-Channel Multiplexer or 8-Channel Differential Multiplexer (Note 1)

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

TRUTH TABLE HI-516 Used as a Differential 8-Channel Multiplexer

A_3 CONNECT TO V- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

NOTE:

- For 16-channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

Test Circuits

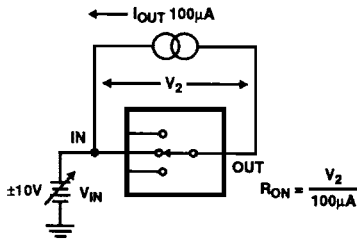


FIGURE 1. ON RESISTANCE vs INPUT SIGNAL LEVEL

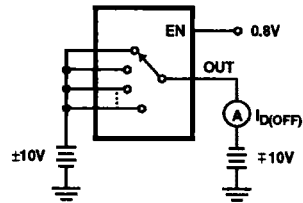


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

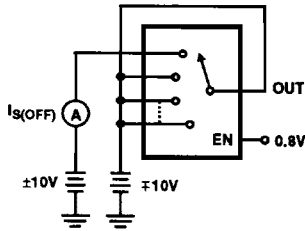


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

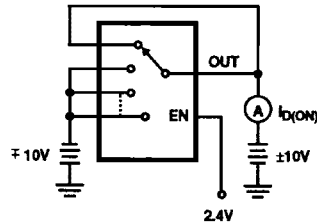


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

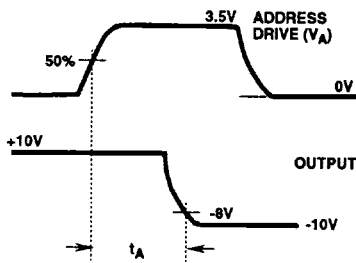


FIGURE 5A.

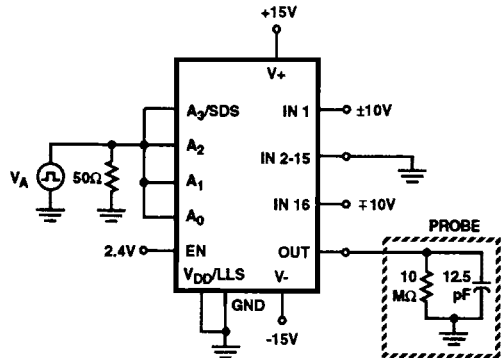


FIGURE 5B.

NOTE:

- Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

Test Circuits (Continued)

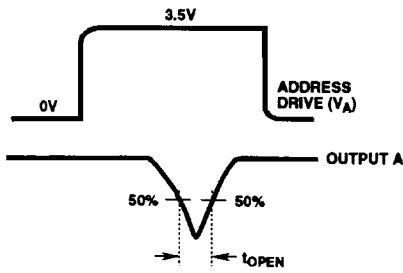


FIGURE 6A. ENABLE DRIVE

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

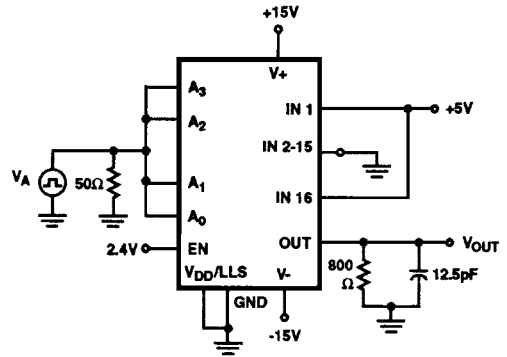


FIGURE 6B.

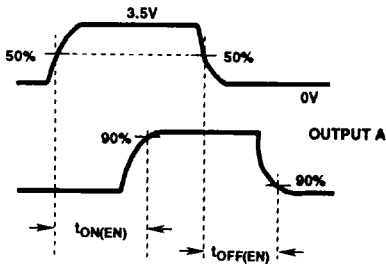


FIGURE 7A. ENABLE DRIVE

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

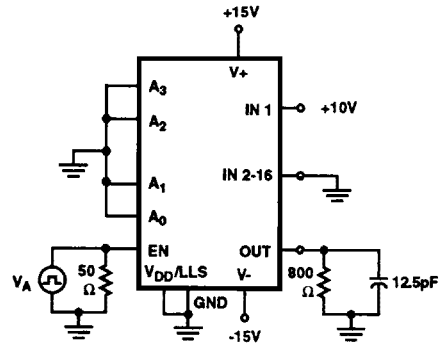


FIGURE 7B.

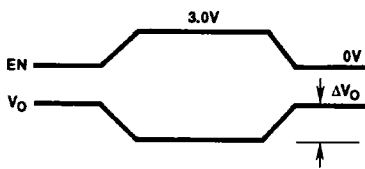


FIGURE 8A.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

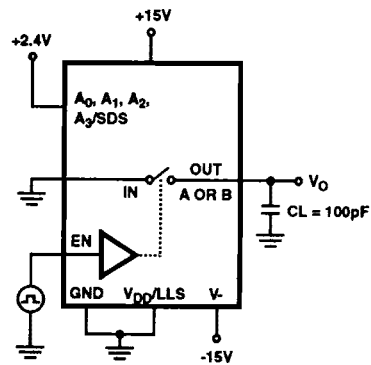


FIGURE 8B.

HI-516

Die Characteristics

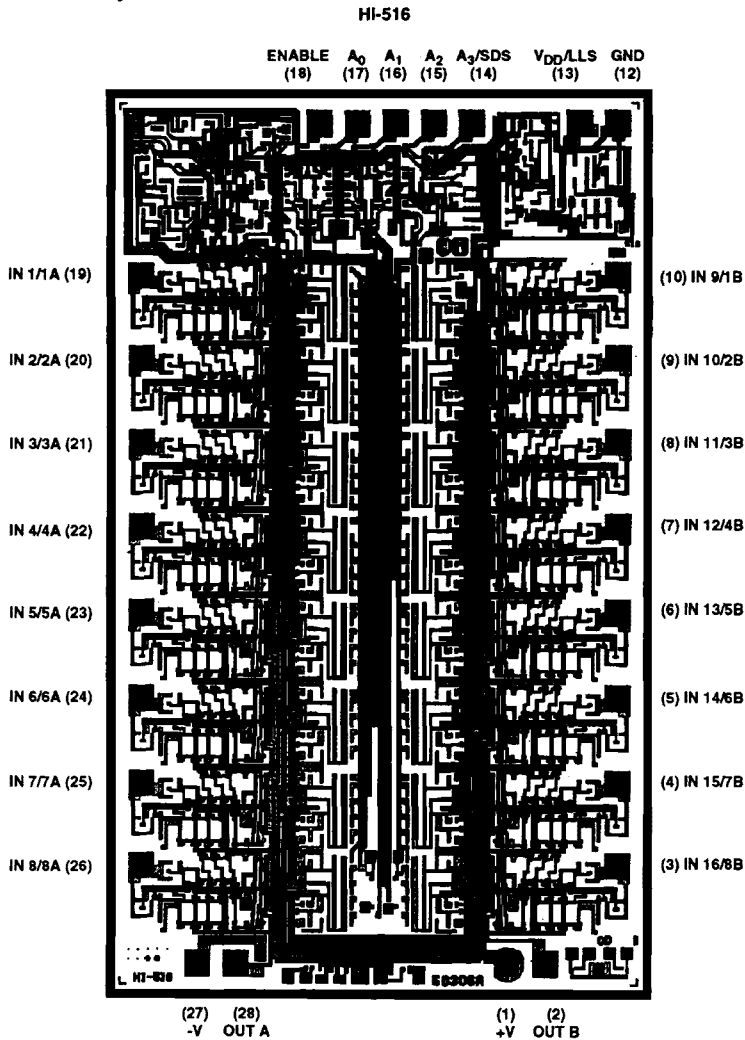
DIE DIMENSIONS:
2250 μ m x 3720 μ m x 485 μ m \pm 25 μ m

METALLIZATION:
Type: CuAl
Thickness: 16k Å \pm 2k Å

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5k Å \pm 1k Å
Silox Thickness: 12k Å \pm 2k Å

WORST CASE CURRENT DENSITY: 1.64 x 10⁵A/cm²

Metallization Mask Layout



MULTIPLEXERS 10