



Integrated Device Technology, Inc.

**64K/128K/256K/512K x 36  
SYNCHRONOUS SRAM  
MODULE FAMILY**

**PRELIMINARY  
IDT7MPV4160  
IDT7MPV4161  
IDT7MPV4162  
IDT7MPV4162A  
IDT7MPV4163**

**FEATURES:**

- Pin compatible flow-through synchronous SRAM module family
- 144 position SO-DIMM Connector,
  - Berg part number: 61178
- As fast as 9ns Clk to Data Times
- All Inputs and Outputs are LVTTTL Compatible
- Multiple Clock Pins for Reduced Loading
- Byte Write Capability
- Single 3.3V power supply ( $\pm 5\%$ )
- Multiple GND pins and decoupling capacitors for maximum noise immunity

**DESCRIPTION:**

The IDT7MPV416 module family consists of the following members:

Module	Configuration	Base SRAM
7MPV4160	64K x 36	64K x 36
7MPV4161	128K x 36	64K x 36
7MPV4162	256K x 36	256K x 18
7MPV4162A	256K x 36	128K x 18
7MPV4163	512K x 36	256K x 18

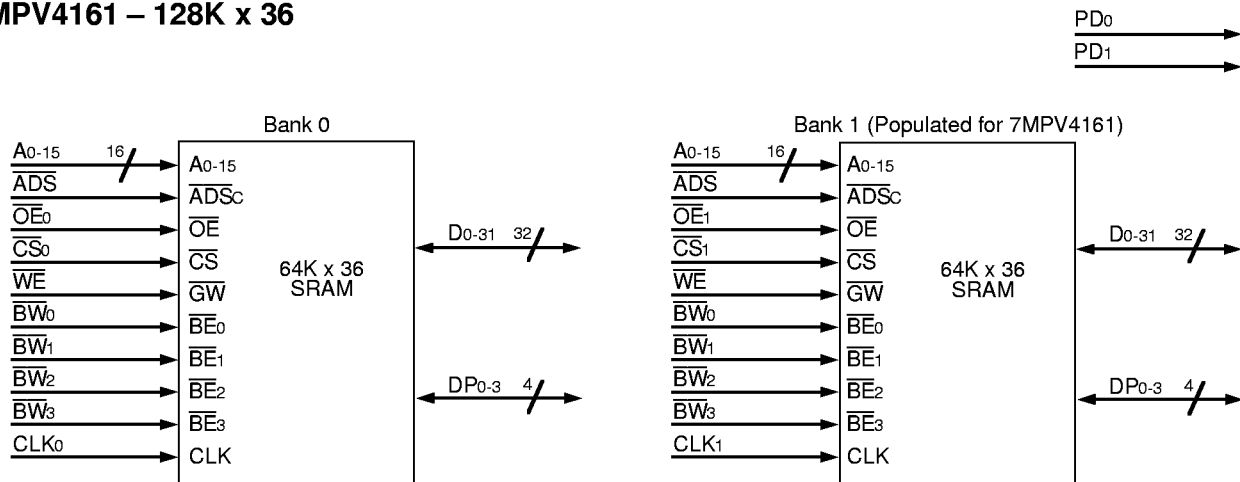
4055 tbl 01

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches of selective deep gold plating.

**FUNCTIONAL BLOCK DIAGRAM**

**IDT7MPV4160 – 64K x 36  
IDT7MPV4161 – 128K x 36**



**NOTE:**

1. D0 - D7 and DP0 are associated with  $\overline{BW0}$ , D8 - D15 and DP1 are associated with  $\overline{BW1}$ , D16 - D23 and DP2 are associated with  $\overline{BW2}$ , and D24 - D31 and DP3 are associated with  $\overline{BW3}$ .

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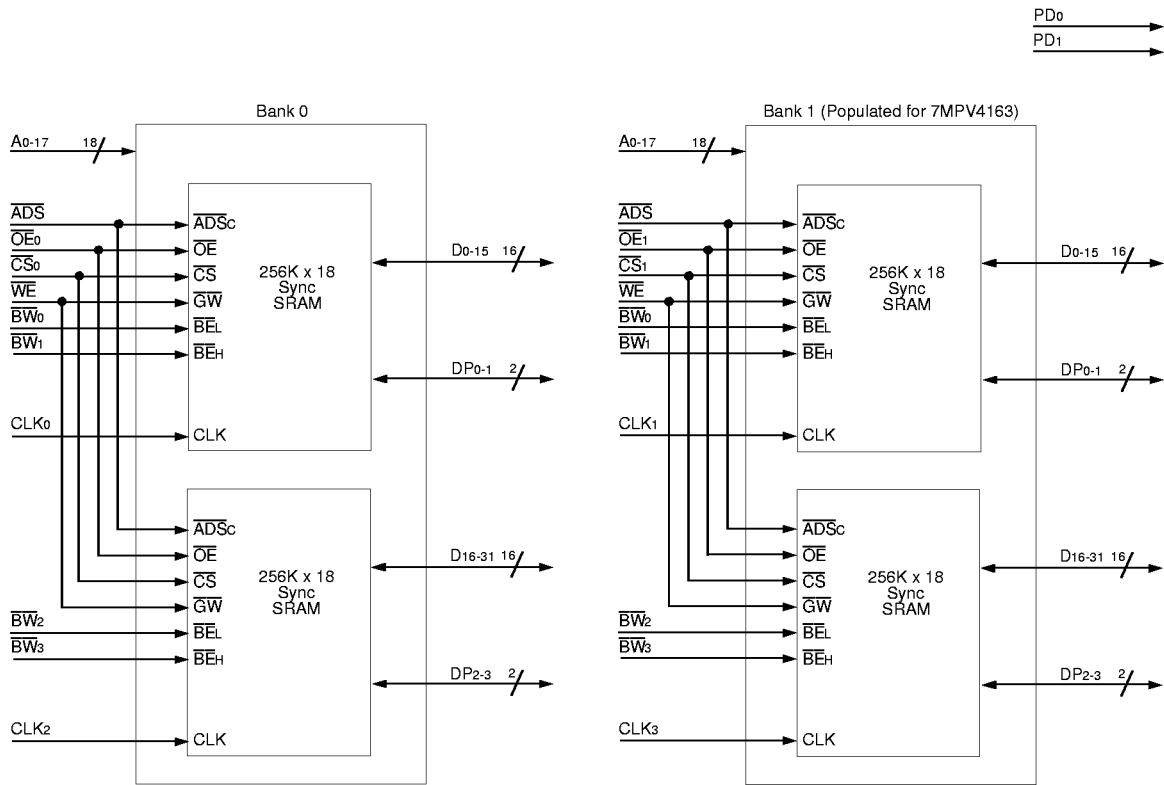
**COMMERCIAL TEMPERATURE RANGE**

**JANUARY 1998**

### FUNCTIONAL BLOCK DIAGRAM

IDT7MPV4162 – 256K x 36

IDT7MPV4163 – 512K x 36

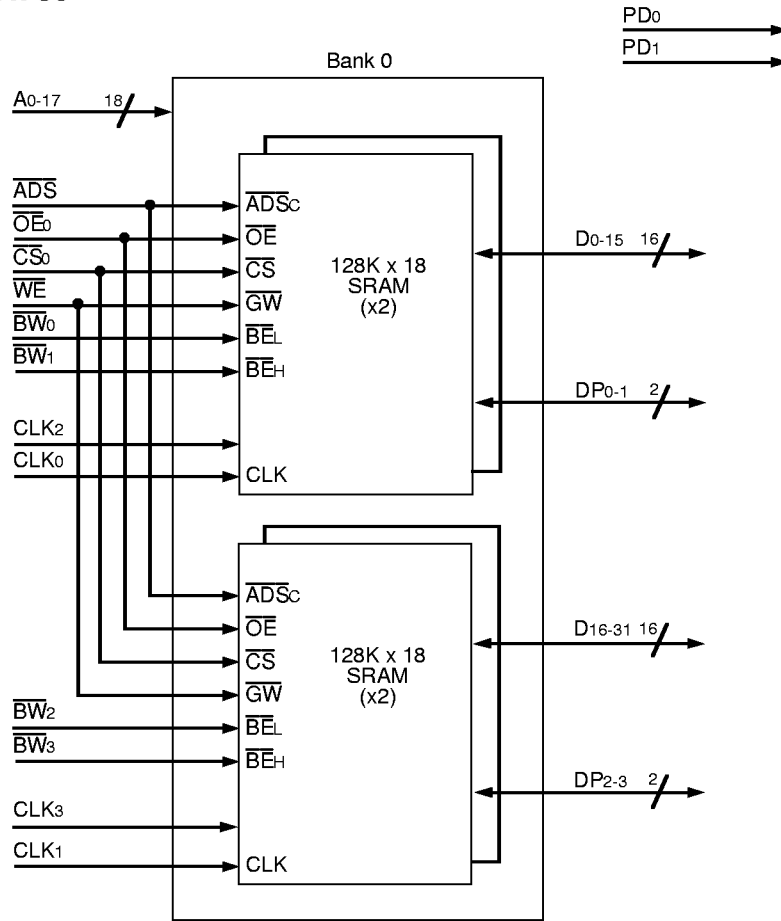


**NOTE:**

1. D<sub>0</sub> - D<sub>7</sub> and DP<sub>0</sub> are associated with  $\overline{BW}_0$ , D<sub>8</sub> - D<sub>15</sub> and DP<sub>1</sub> are associated with  $\overline{BW}_1$ , D<sub>16</sub> - D<sub>23</sub> and DP<sub>2</sub> are associated with  $\overline{BW}_2$ , and D<sub>24</sub> - D<sub>31</sub> and DP<sub>3</sub> are associated with  $\overline{BW}_3$ .

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**FUNCTIONAL BLOCK DIAGRAM**  
**IDT7MPV4162A – 256K x 36**



**NOTE:**

1. D0 - D7 and DP0 are associated with  $\overline{BW}_0$ , D8 - D15 and DP1 are associated with  $\overline{BW}_1$ , D16 - D23 and DP2 are associated with  $\overline{BW}_2$ , and D24 - D31 and DP3 are associated with  $\overline{BW}_3$ .

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### PIN NAMES

A0 – A17	Address Inputs
D0 – D31	Data Inputs/Outputs
DP0 – DP3	Data Parity Inputs/Outputs
$\overline{CS}_0-1$	Chip Select Inputs
$\overline{OE}_0-1$	Data Output Enable Inputs
$\overline{BW}_0 – \overline{BW}_3$	Data Write Enable Inputs
CLK0-3	Clock Inputs
$\overline{ADS}$	Address Status Inputs
$\overline{WE}$	Global Write Input
RES	Reserved Pins
NC	No Connect
PD0-PD1	Presence Detect Pins
GND	Ground
Vcc	3.3 Volt Power Supply

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### PRESENCE DETECT PINS

Configuration	PD <sub>1</sub>	PD <sub>0</sub>
IDT7MPV4160 - 64Kx36	GND	NC
IDT7MPV4161 – 128K x 36	NC	GND
IDT7MPV4162 – 256K x 36	GND	GND
IDT7MPV4162A - 256K x 36	GND	GND
IDT7MPV4163 – 512K x 36	NC	NC

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### MODULE PINOUT

GND	1	2	GND
A0	3	4	A1
A2	5	6	A3
A4	7	8	A5
Vcc	9	10	Vcc
(1) RES	11	12	RES (1)
(1) RES	13	14	RES (1)
GND	15	16	GND
A6	17	18	A7
A8	19	20	A9
A10	21	22	A11
NC	23	24	NC
Vcc	25	26	Vcc
A12	27	28	A13
A14	29	30	A15
A16	31	32	A17
GND	33	34	GND
PD0	35	36	PD1
GND	37	38	GND
$\overline{BW}_0$	39	40	$\overline{BW}_1$
$\overline{CS}_0$	41	42	$\overline{OE}_0$
GND	43	44	GND
CLK1	45	46	CLK0
GND	47	48	GND
D0	49	50	D1
Vcc	51	52	Vcc
D2	53	54	D3
D4	55	56	D5
D6	57	58	D7
GND	59	60	GND
Vcc	61	62	Vcc
D8	63	64	D9
D10	65	66	D11
GND	67	68	GND
D12	69	70	D13
D14	71	72	D15
DP0	73	74	DP1
(1) RES	75	76	RES (1)
(1) RES	77	78	RES (1)
GND	79	80	GND
$\overline{WE}$	81	82	$\overline{ADS}$
NC	83	84	NC
Vcc	85	86	Vcc
NC	87	88	NC
NC	89	90	NC
NC	91	92	NC
Vcc	93	94	Vcc
NC	95	96	NC
NC	97	98	NC
NC	99	100	NC
GND	101	102	GND
$\overline{BW}_2$	103	104	$\overline{BW}_3$
$\overline{CS}_1$	105	106	$\overline{OE}_1$
Vcc	107	108	Vcc
D16	109	110	D17
D18	111	112	D19
NC	113	114	NC
NC	115	116	NC
NC	117	118	NC
GND	119	120	GND
CLK3	121	122	CLK2
GND	123	124	GND
D20	125	126	D21
GND	127	128	GND
D22	129	130	D23
D24	131	132	D25
D26	133	134	D27
D28	135	136	D29
Vcc	137	138	Vcc
D30	139	140	D31
DP2	141	142	DP3
GND	143	144	GND

### SO-DIMM TOP VIEW

#### NOTES:

1. These pins are No Connects; they are reserved for future modules.

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## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 5%

4055 tbl 04

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0.0	V
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

### NOTE:

1. V<sub>IL</sub> = -1.0V for pulse width less than t<sub>CYC</sub>/2, once per cycle.

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V <sub>TERM</sub> for V <sub>CC</sub>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

### NOTE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V<sub>CC</sub> = 3.3V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CS} \geq V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>CC</sub> , V <sub>CC</sub> = Max.	—	10	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2 mA, V <sub>CC</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2 mA, V <sub>CC</sub> = Min.	2.4	—	V

4055 tbl 07

Symbol	Parameter	Test Condition	'4160	'4161	'4162	'4162A	'4163	Unit
I <sub>CC</sub> <sup>(3)</sup>	Operating Power Supply Current	$\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	330	390	600	860	930	mA
I <sub>SB</sub>	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ , Outputs Open, V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	60	120	330	520	660	mA

### NOTES:

- All values are maximum guaranteed values.
- At f = f<sub>MAX</sub>, address inputs are switching at 1/t<sub>CYC</sub> and CLK is cycling at 1/t<sub>CYC</sub>; f=0 means no input signals are changing.
- I<sub>CC</sub> specification for the 7MPV4161, 7MPV4162A, 7MPV4162A, and 7MPV4163 assumes that only one bank is selected.

4055 tbl 08

## CAPACITANCE

(T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	'4160 Max.	'4161 Max.	'4162 Max.	'4162A Max.	'4163 Max.	Unit
C <sub>IN1</sub>	Input Capacitance Address, $\overline{ADS}$ , $\overline{WE}$	V <sub>IN</sub> = 3dV	10	20	20	35	35	pF
C <sub>IN2</sub>	Input Capacitance $\overline{OE}$ , $\overline{CS}$	V <sub>IN</sub> = 3dV	10	10	20	35	20	pF
C <sub>IN3</sub>	Input Capacitance $\overline{BW}_{0-3}$	V <sub>IN</sub> = 3dV	10	20	10	20	20	pF
C <sub>INCLK</sub>	Input Capacitance Clock	V <sub>IN</sub> = 3dV	10	10	10	10	10	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	10	20	10	20	20	pF

### NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

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### AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

4055 tbl 09

### AC TEST LOADS

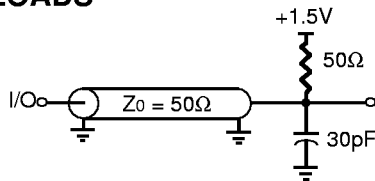


Figure 1. AC Test Load

4055 drw 04

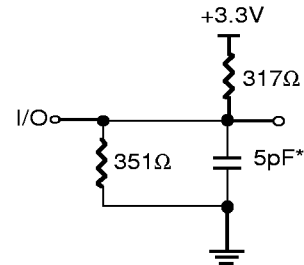
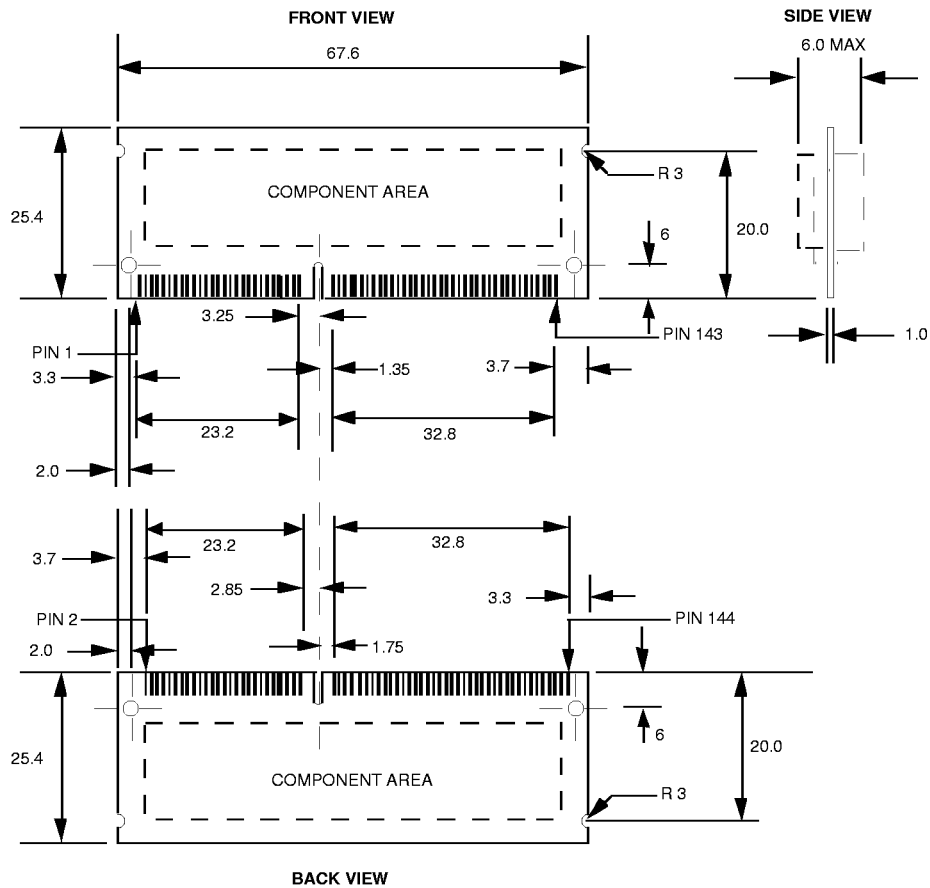


Figure 2. AC Test Load  
(for toHZ, tCHZ, toLZ, and tbc1)

4055 drw 05

\* Including scope and jig

### PACKAGE DIMENSIONS

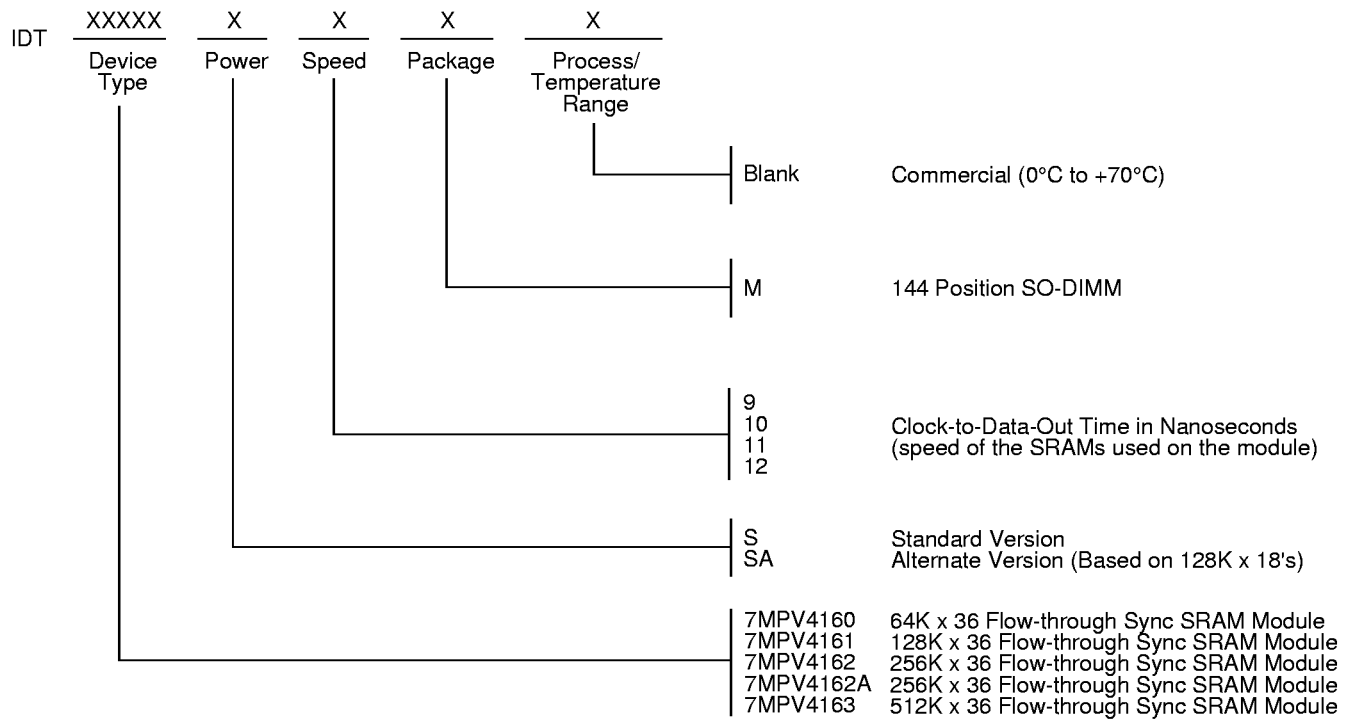


#### NOTES:

1. All dimensions are in millimeters.
2. Dimensions conform to the small outline DIMM 144 position connector from Berg (part number 61178).
3. Tolerances on all dimensions are  $\pm 0.15\text{mm}$ .

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**ORDERING INFORMATION**



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Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

**Integrated Device Technology, Inc.**

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