

FSA2147 — Low-Voltage, DPST Analog Switch with Negative Signal Capability and Built-in Termination to Eliminate Pop

Features

- Built-In Termination on Unselected Audio Paths Inhibits Audio Pop
- 6pF Typical Switch Off Capacitance
- 2.5Ω Typical On Resistance
- Negative-Swing-Capable
- Power-Off Protection
- Flow-Through Pin Out Eliminates PCB Vias

Description

The FSA2147 is a Double-Pole, Single Throw (DPST) switch. The audio path defaults to audio mute and is enabled with /OE. The FSA2147 includes a power-off feature on the common port when $V_{CC}=0V$ to guarantee signal isolation.

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Applications

- MP3 Player, Cell Phone, PDA, Digital Camera, and Notebook Computers

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Eco Status	Package Description	Packing Method
FSA2147K8X	2147	-40°C to +85°C	RoHS	8-Lead US8, JEDEC MO-187, Variation CA, 3.0mm Wide Package	3000 Units Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

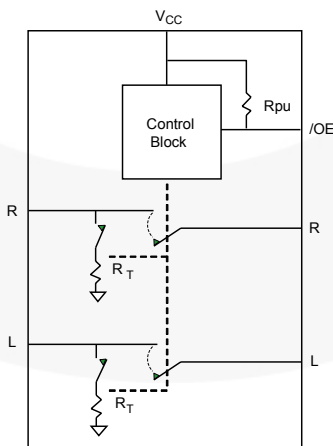


Figure 1. Analog Symbol

Pin Configuration

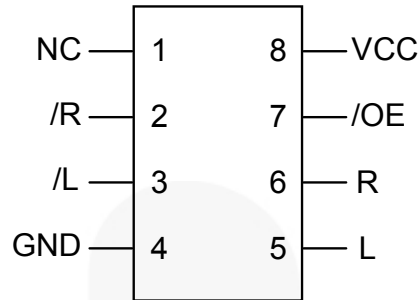


Figure 2. 8-Pin US8

Pin Descriptions

Pin #	Name	Description
8	V _{CC}	Power supply.
7	/OE	Output enable. This pin defaults HIGH, allowing the user to mute the audio channel during power up. The audio path is only connected when /OE is driven LOW.
6, 5	R, L	Audio right and left input sources.
2, 3	/R, /L	Audio common connector port.

Truth Table

V _{CC}	/OE	Switch
LOW		OPEN
HIGH	LOW	ON
HIGH	HIGH	OPEN

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	4.6	V
/OE	Output Enable Control Signal	-0.5	4.6	V
V_{SW}	Switch I/O Voltage ⁽¹⁾	$V_{CC}-4.6$	4.6	V
I_{IK}	Input Clamp Diode Current		-50	mA
I_{SW}	Switch I/O Current (Continuous)		100	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)		150	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)		+260	°C
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND	12	kV
		All Other Pins	2	
		V_{CC} to GND	12	
	Charged Discharge Model, JEDEC: JESD22-C101	2		

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2.7	4.3	V
/OE	Output Enable Control Signal	3.0	4.3	V
V_{SW}	Switch I/O Voltage	$V_{CC}-4.3$	4.3	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = -40 to +85°C			Unit
				Min.	Typ. ⁽⁵⁾	Max.	
Common Pins							
V _{IK}	Clamp Diode Voltage	3.0	I _{IK} = -18mA			-1.2	V
V _{IH}	Control Input Voltage HIGH	2.7 to 4.3		1.7			
V _{IL}	Control Input Voltage LOW	2.7 to 4.3				0.6	
I _{IN}	/OE Input Leakage Current	4.3	V _{IN} = 4.3V	1		-1	μA
I _{OFF}	Power Off Leakage Current (Common Port Only /R, /L)	0	Common Port (/R, /L) V _{SW} = 4.3V or Floating	-10		10	μA
I _{NC(ON)}	On-Leakage Current of Port /R or /L	4.3	/R, /L = 0.3V, 4.0V R, L = Floating Figure 8	-250	1	250	nA
R _{PU}	/OE Internal Pull-Up Resistor	4.3			3		MΩ
R _T	Audio Path Termination Resistors	4.3	V _{IN} =0.3V or 4.0V		100		Ω
V _{Audio}	Analog Signal Range	2.7 to 4.3		V _{CC} -4.3V		V _{CC}	V
R _{ONAudio}	Switch On Resistance ⁽²⁾	2.7	V _{L/R} = -1.5V, 0V, 1.5V I _{ON} = 60mA		1.5	3.0	Ω
ΔR _{ONAudio}	Delta R _{ON} ⁽³⁾	2.7	V _{L/R} = 0.7V I _{ON} = 60mA		0.4		Ω
R _{FLAT(Audio)}	R _{ON} Flatness ⁽⁴⁾	2.7	V _{SW} =-1.5V to 1.5V, I _{ON} = 60mA		0.4	0.8	Ω
Power Supply							
I _{CC}	Quiescent Supply Current	4.3	/OE = Low or V _{CC} , I _{OUT} = 0		1.5	15	μA

Notes:

2. On resistance is determined by the voltage drop between the A and B pins at the indicated current through the switch.
3. Δ R_{ON} = R_{ON max} – R_{ON min} measured at identical V_{CC}, temperature, and voltage.
4. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.
5. Guaranteed by characterization; not production tested.

AC Electrical Characteristics

All typical value are for $V_{CC} = 3.6V$ at $25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = -40$ to $+85^{\circ}C$			Unit
				Min.	Typ. ⁽⁶⁾	Max.	
t_{ON}	Turn-On Time, /OE to Output	2.7 to 4.3	$V_{R/L} = 1.0V$ $R_L = 50\Omega$, $C_L = 50pF$ Figure 9, Figure 10, Figure 11		2		μs
t_{OFF}	Turn-Off Time, /OE to Output	2.7 to 4.3	$V_{R/L} = 1.0V$ $R_L = 50\Omega$, $C_L = 50pF$ Figure 9, Figure 10, Figure 11		2		μs
Xtalk	Non-Adjacent Channel Crosstalk (Audio Mode)	3.3 to 4.3	$f = 20kHz$, $R_T = 32\Omega$, $C_L = 0pF$ Figure 16		-75		dB
THD	Total Harmonic Distortion (Audio Mode)	3.0 to 4.3	$f = 20Hz$ to $20kHz$ $R_L = 32\Omega$, $V_{IN} = 2V_{PP}$ Figure 14		0.05		%
SNR	Signal-to-Noise Ratio (Audio Mode)	3.3 to 4.3	$f = 20kHz$ to $20kHz$, $R_L = 32\Omega$, $V_{IN} = 2V_{PP}$ Figure 14		80		dB

Note:

6. Guaranteed by characterization; not production tested.

Capacitance

All typical values are at $25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = -40$ to $+85^{\circ}C$			Unit
				Min.	Typ. ⁽⁷⁾	Max.	
C_{IN}	Control Pin Input Capacitance	3.0 to 4.3	$V_{BIAS} = 0.2V$		2.5		pF

Note:

7. Guaranteed by characterization; not production tested.

Typical Characteristics

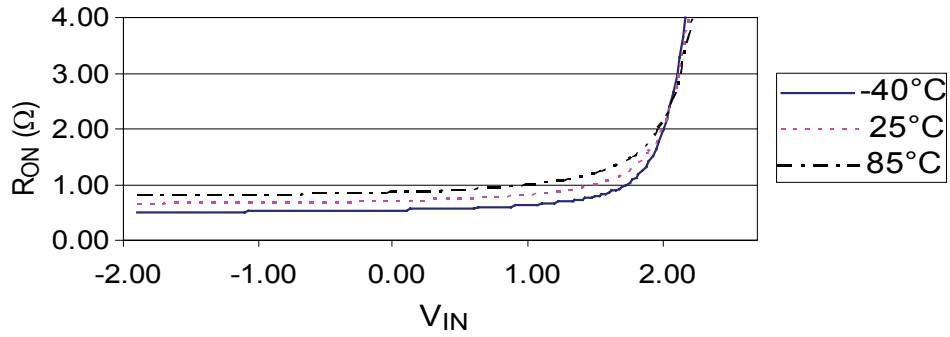


Figure 3. $R_{ON}, V_{CC}=2.7V$

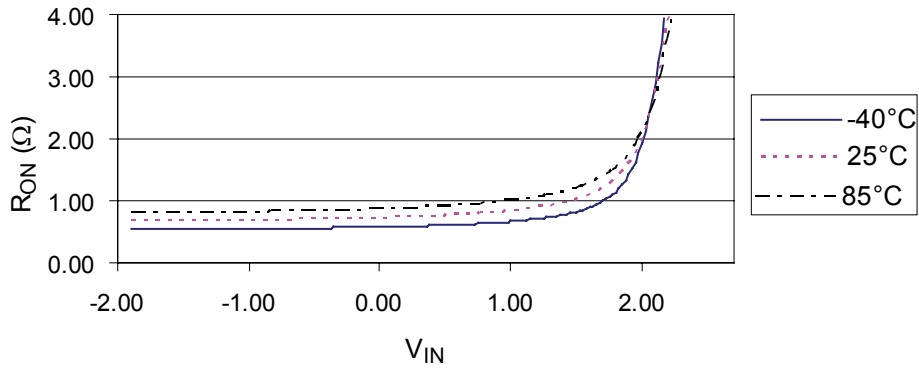


Figure 4. $R_{ON}, V_{CC}=2.7V$

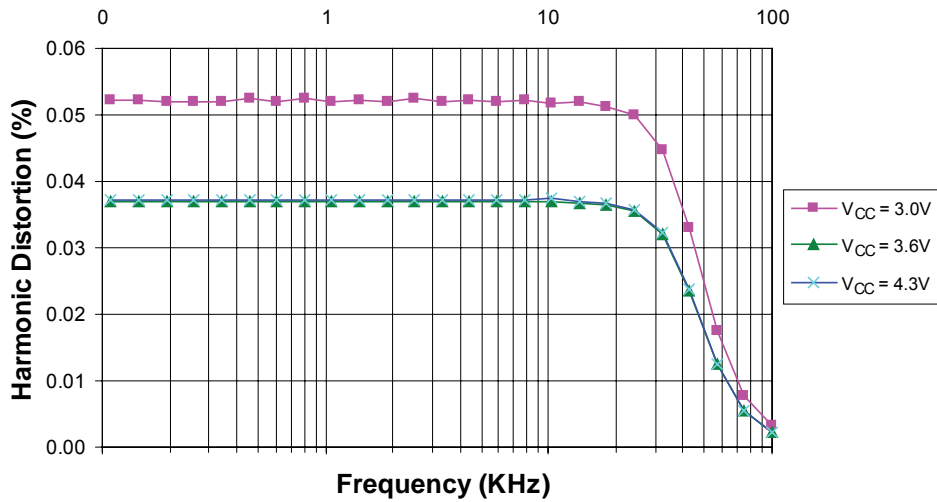


Figure 5. Total Harmonic Distortion

Test Diagrams

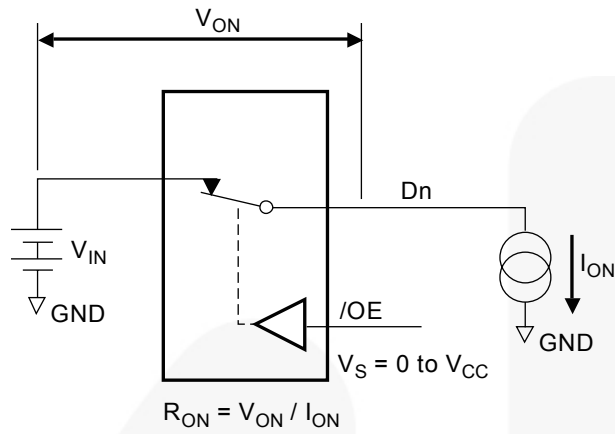


Figure 6. On Resistance

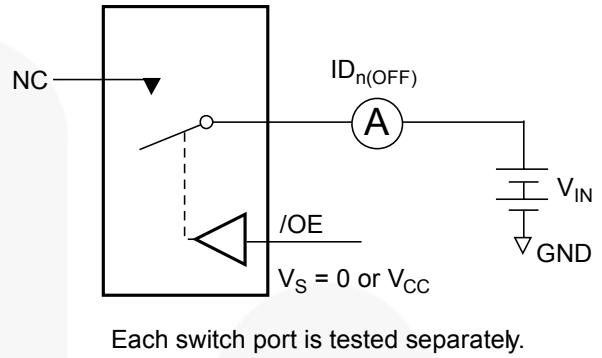


Figure 7. Off Leakage

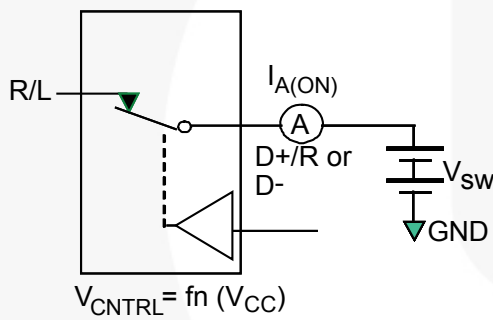
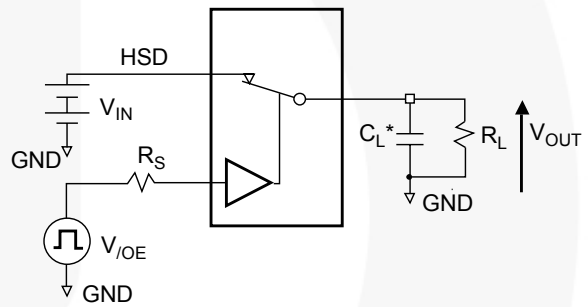


Figure 8. On Leakage



R_L , R_S , and C_L are functions of the application environment (see tables for specific values).

* C_L includes test fixture and stray capacitance.

Figure 9. AC Test Circuit Load

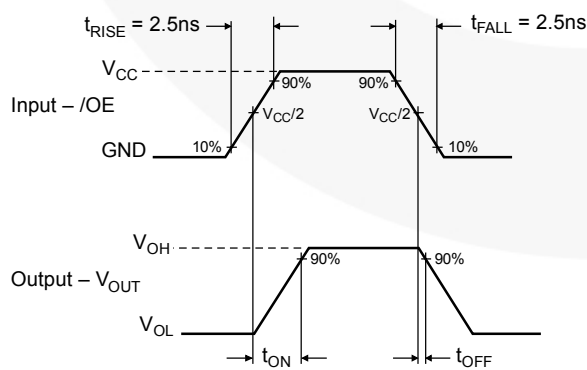


Figure 10. Turn-On / Turn-Off Waveforms

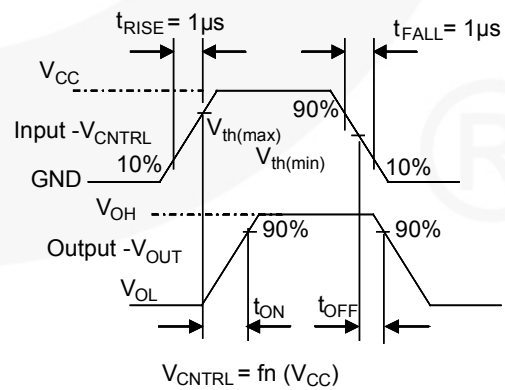


Figure 11. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)

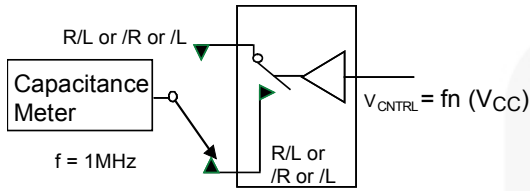


Figure 12. Channel Off Capacitance

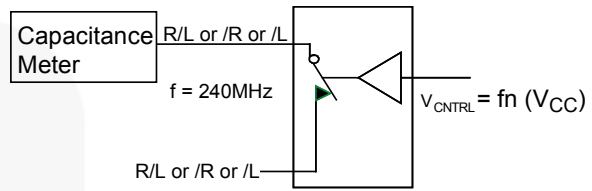


Figure 13. Channel On Capacitance

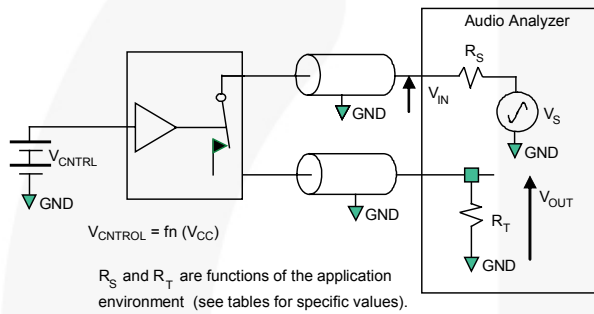


Figure 14. Total Harmonic Distortion

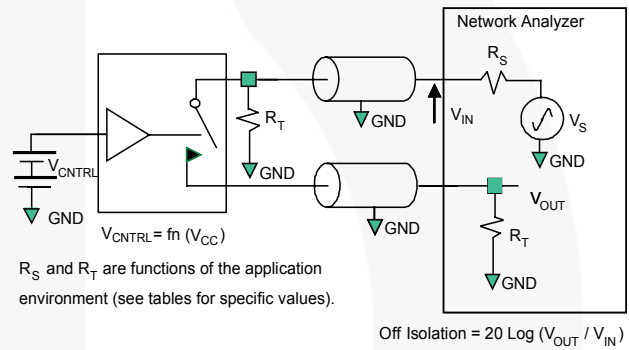


Figure 15. Channel Off Isolation

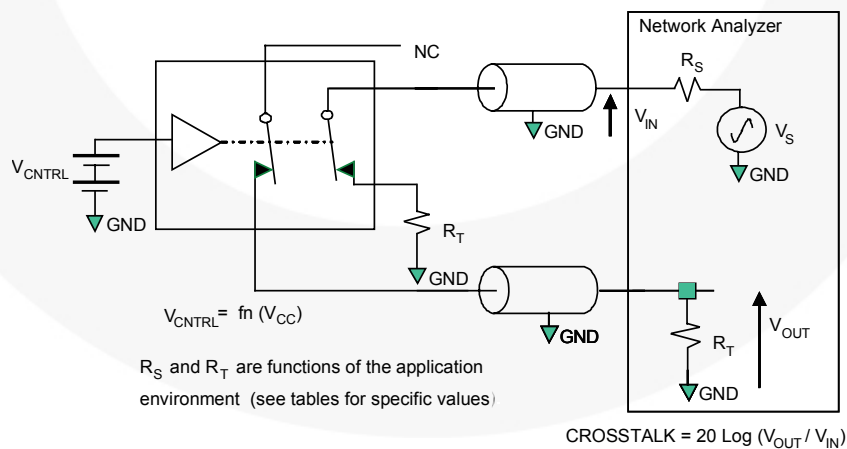
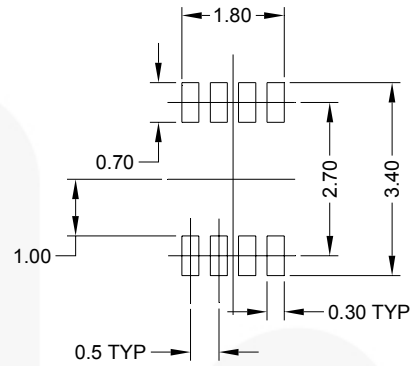
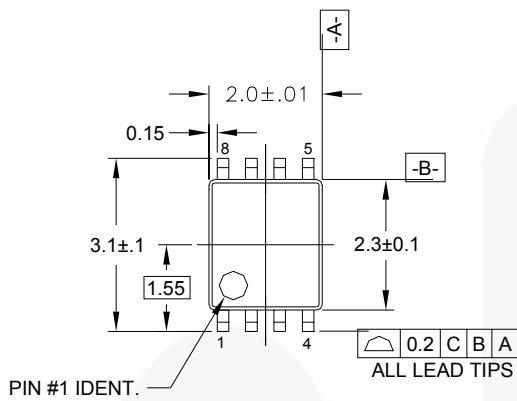
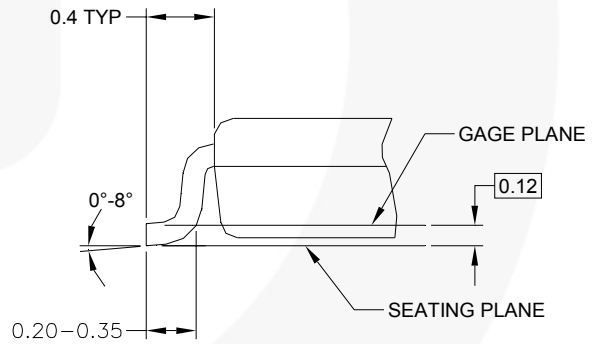
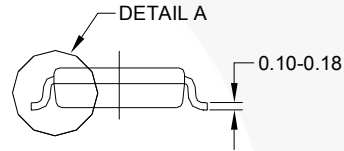
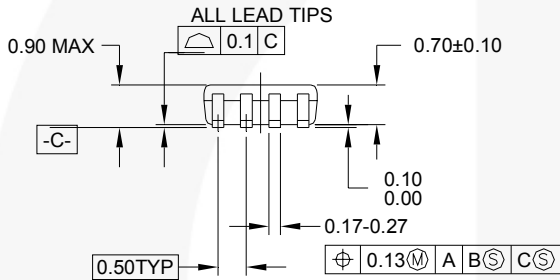


Figure 16. Non-Adjacent Channel-to-Channel Crosstalk

Physical Dimensions



LAND PATTERN RECOMMENDATION



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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Figure 17. 8-Lead US8, JEDEC MO-187, Variation CA, 3.0mm Wide Package

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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