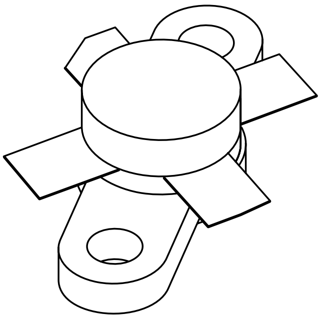
DATA SHEET



BLF175
HF/VHF power MOS transistor

Product specification
Supersedes data of 1997 Dec 15

2003 Jul 22

Philips
Semiconductors

PHILIPS

HF/VHF power MOS transistor BLF175

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF/VHF frequency range.

The transistor has a 4-lead, SOT123A flange package, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the handbook 'General' section for further information.

PINNING - SOT123A

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

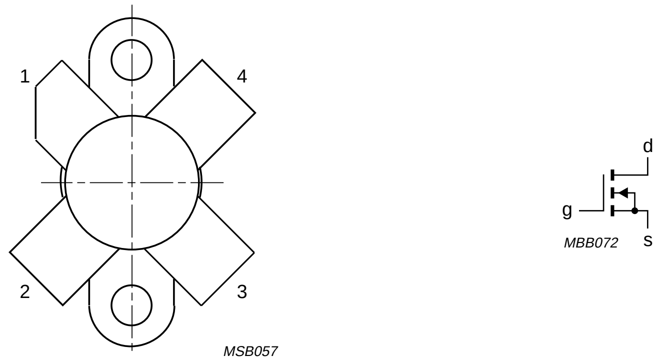


Fig.1 Simplified outline and symbol.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)
class-A	28	50	800	8 (PEP)	>24	–	<–40
class-AB	28	50	150	30 (PEP)	typ. 24	typ. 40(1)	typ. –35
CW, class-B	108	50	30	30	typ. 20	typ. 65	–

Note

1. 2-tone efficiency.

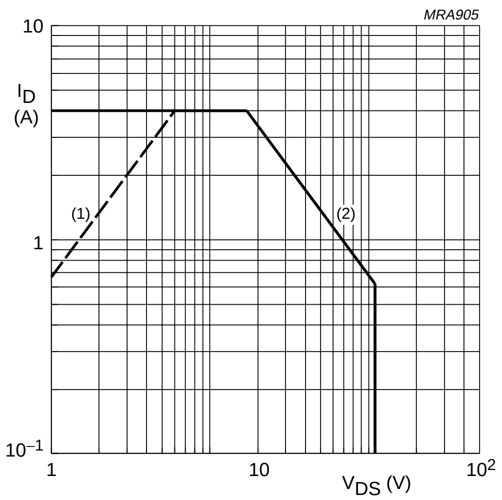
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	125	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	68	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

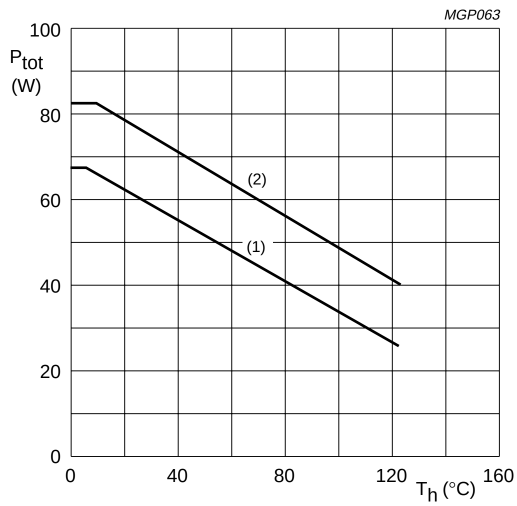
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 68 W	2.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 68 W	0.3	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

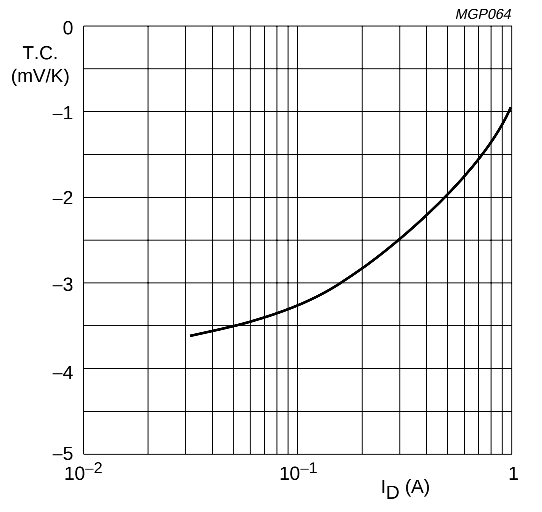
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 100 mA; V_{GS} = 0	125	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	100	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1 A; V_{DS} = 10 V	1.1	1.6	–	S
R_{DSon}	drain-source on-state resistance	I_D = 1 A; V_{GS} = 10 V	–	0.75	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5.5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	130	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	36	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	3.7	–	pF

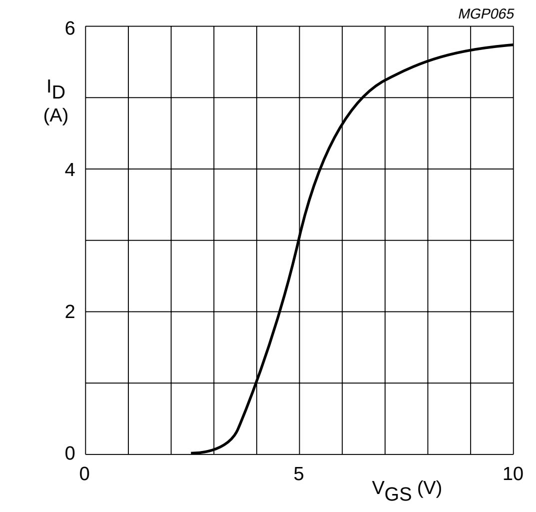
V_{GS} group indication

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



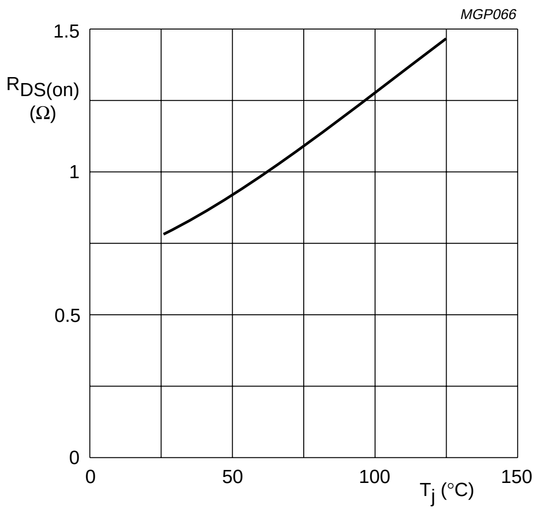
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



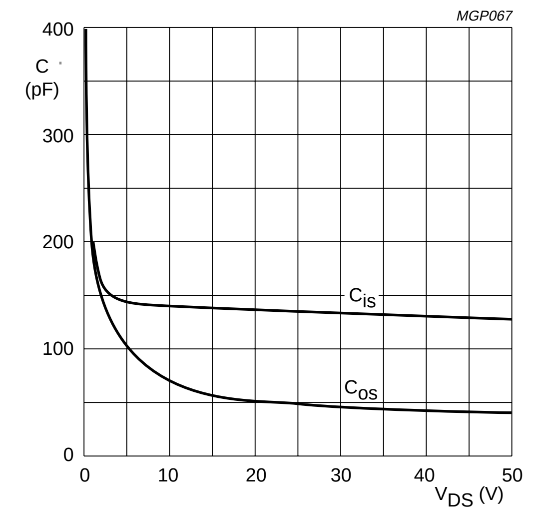
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.



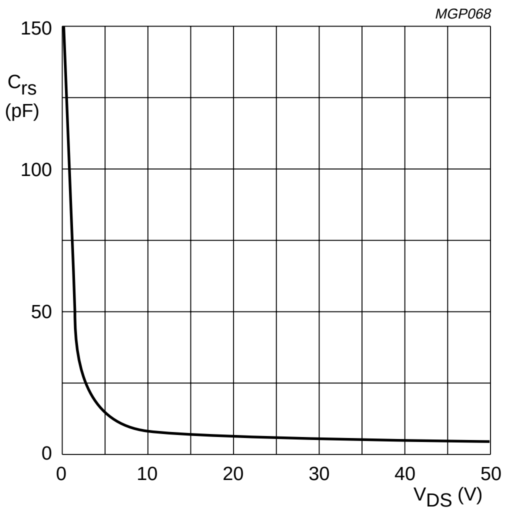
I_D = 1 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.

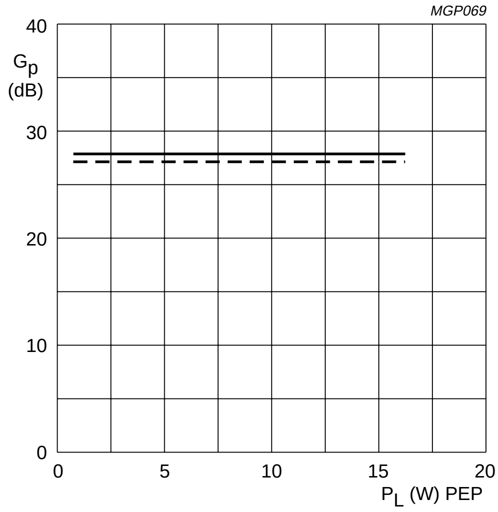
RF performance in SSB operation in a common source circuit.

f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_p (dB)	d_3 (dB)(1)	d_5 (dB)(1)	R_{GS} (Ω)
0 to 8 (PEP)	28	50	800	> 24 typ. 28	> –40 typ. –44	< –40 typ. –64	24 24

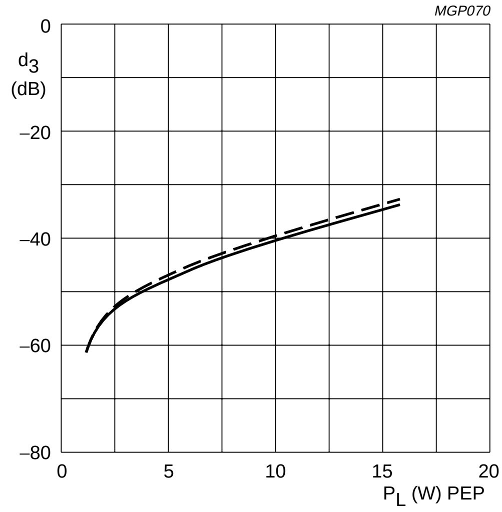
Note

1. Maximum values at drive levels within the specified PEP values for either amplified tone. For the peak envelope power the values should be decreased by 6 dB.



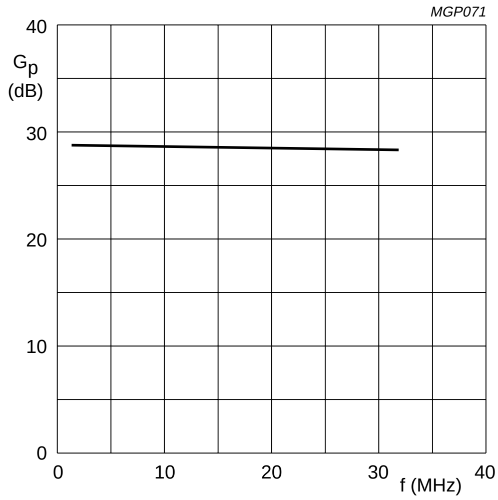
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power; typical values.



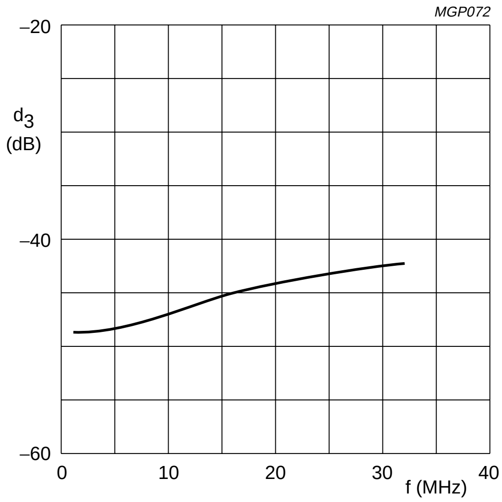
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power; typical values.



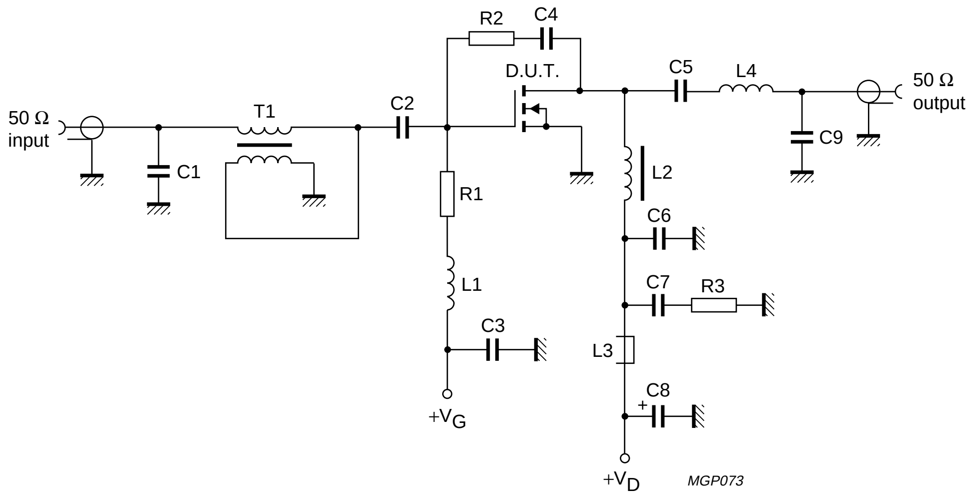
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.11 Power gain as a function of frequency; typical values.



Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.12 Third order intermodulation distortion as a function of frequency; typical values.



f = 28 MHz.

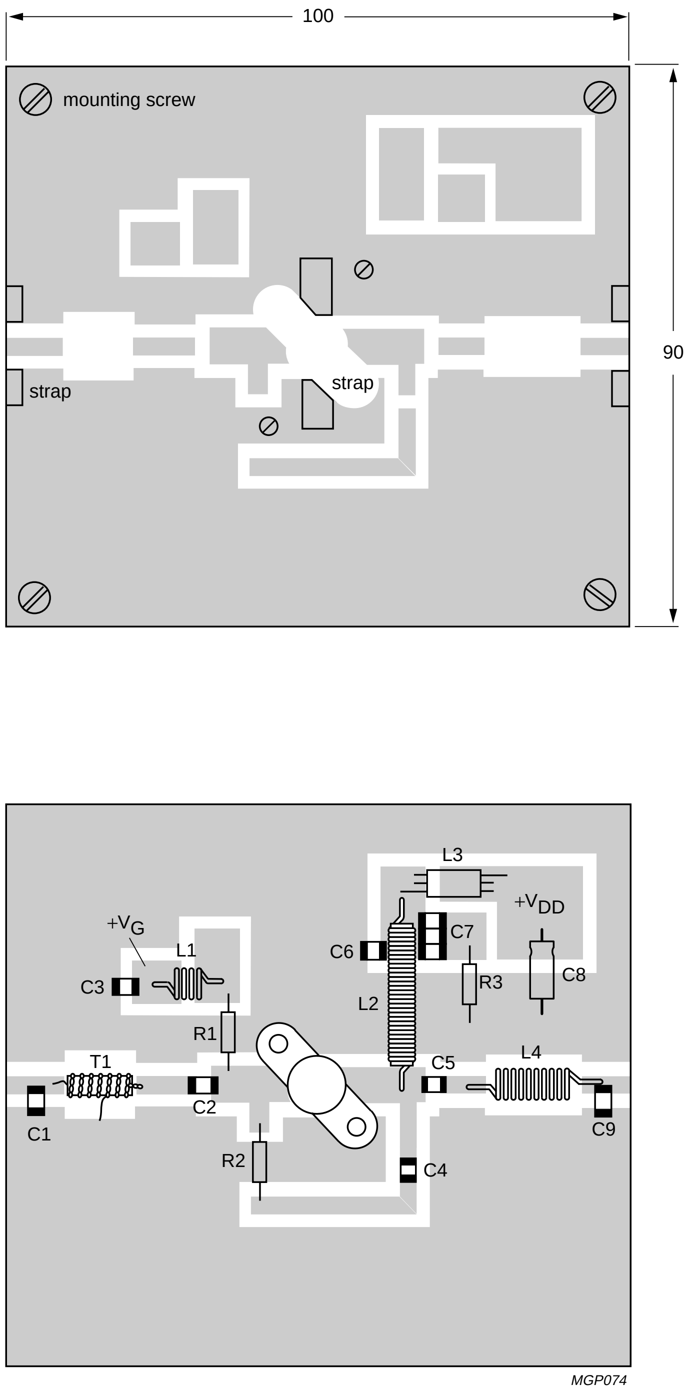
Fig.13 Test circuit for class-A operation.

List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor (note 1)	39 pF		
C2	multilayer ceramic chip capacitor	3 × 10 nF		2222 852 47103
C3, C4, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C8	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
C9	multilayer ceramic chip capacitor (note 1)	24 pF		
L1	4 turns enamelled 0.6 mm copper wire	86 nH	length 3.3 mm; int. dia. 5 mm; leads 2 × 2 mm	
L2	36 turns enamelled 0.7 mm copper wire wound on a rod grade 4B1 Ferroxcube drain choke	20 μH	length 30 mm; int. dia. 5 mm	4330 030 30031
L3	grade 3B Ferroxcube wideband RF choke			4312 020 36640
L4	8 turns enamelled 1 mm copper wire	189 nH	length 9.5 mm; int. dia. 5 mm; leads 2 × 3 mm	
R1	0.4 W metal film resistor	24 Ω		
R2	0.4 W metal film resistor	1500 Ω		
R3	0.4 W metal film resistor	10 Ω		
T1	4 : 1 transformer; 18 turns twisted pair of 0.25 mm copper wire with 10 twists per cm, wound on a grade 4C6 toroidal core		dimensions 9 × 6 × 3 mm	4322 020 97171

Note

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.



Dimensions in mm.

The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

Fig.14 Component layout for 28 MHz class-A test circuit.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_p (dB)	η_D (%)	d_3 (dB)(1)	d_5 (dB)(1)	R_{GS} (Ω)
30 (PEP)	28	50	150	typ. 24	typ. 40(2)	typ. –35	typ. –40	22

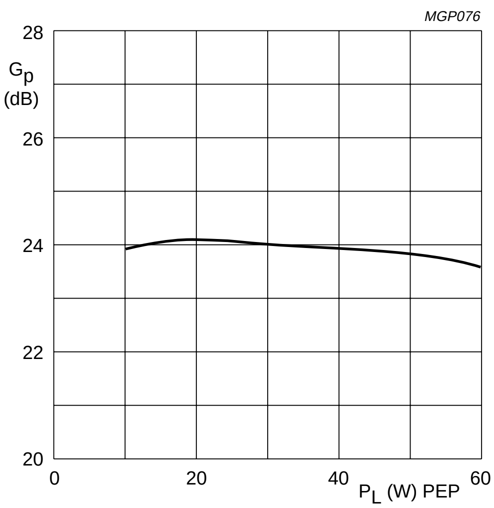
Notes

1. Maximum values at drive levels within the specified PEP values for either amplified tone. For the peak envelope power the values should be decreased by 6 dB.
2. 2-tone efficiency.

Ruggedness in class-AB operation

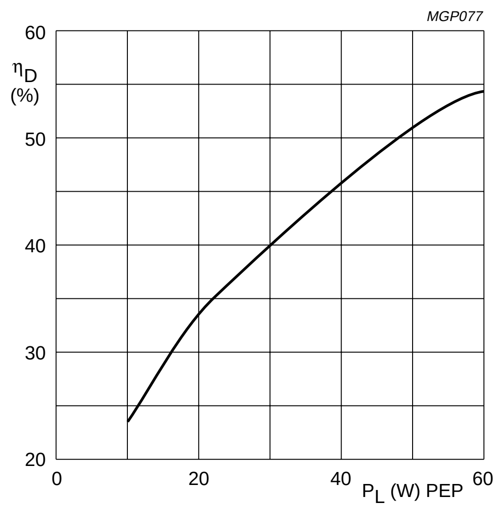
The BLF175 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at P_L = 30 W single tone under the following conditions:

V_{DS} = 50 V; f = 28 MHz.



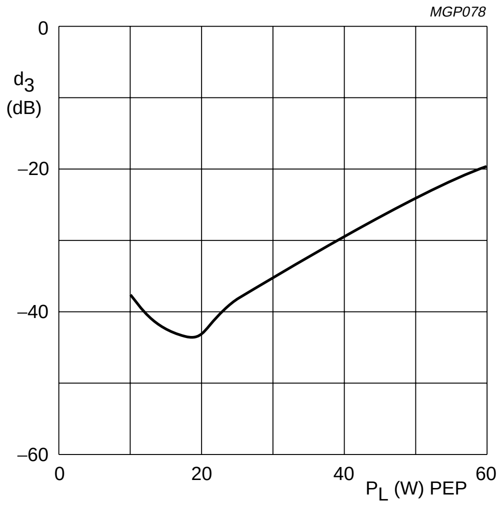
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.15 Power gain as a function of load power; typical values.



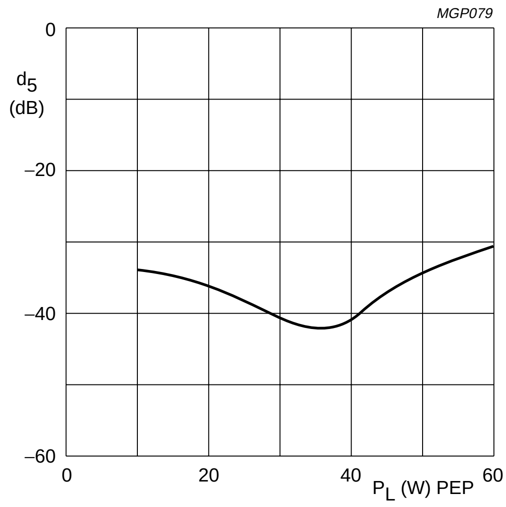
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.16 Two tone efficiency as a function of load power; typical values.



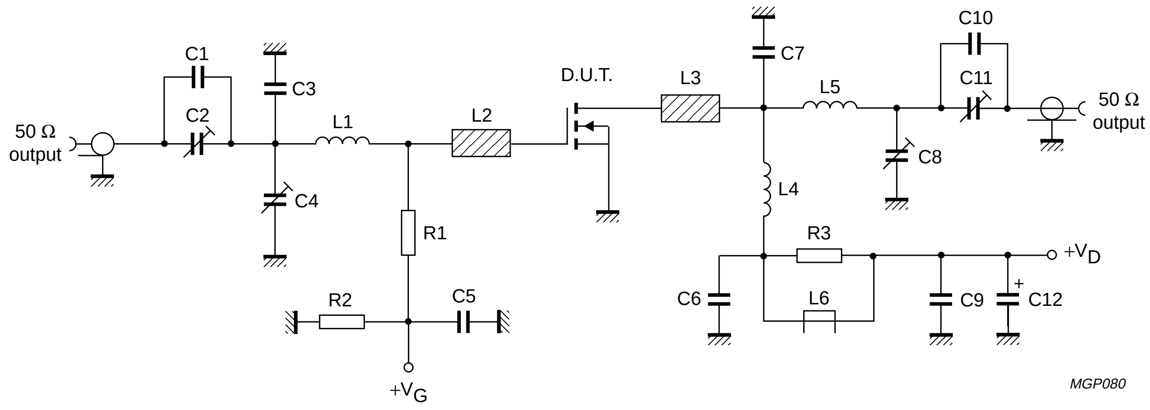
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.17 Third order intermodulation distortion as a function of load power; typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.18 Fifth order intermodulation distortion as a function of load power; typical values.



f = 28 MHz.

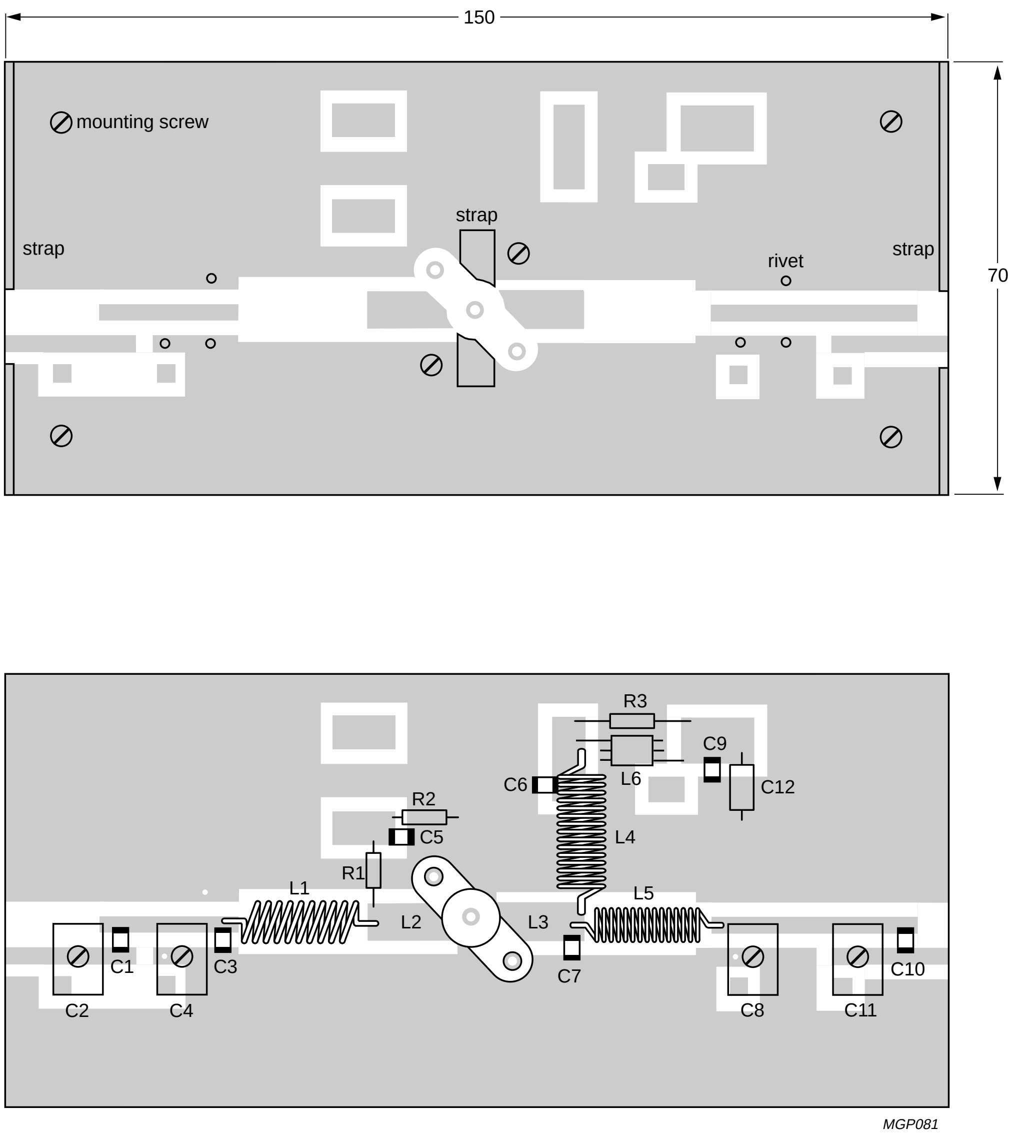
Fig.19 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C10	multilayer ceramic chip capacitor (note 1)	62 pF		
C2, C4, C8, C11	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor (note 1)	51 pF		
C5, C6, C9	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor (note 1)	10 pF		
C12	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
L1	9 turns enamelled 1 mm copper wire	280 nH	length 11 mm; int. dia. 6 mm; leads 2 × 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 10 mm; width 6 mm	
L4	14 turns enamelled 1 mm copper wire	1650 nH	length 20 mm; int. dia. 12 mm; leads 2 × 2 mm	
L5	10 turns enamelled 1 mm copper wire	380 nH	length 13 mm; int. dia. 7 mm; leads 2 × 3 mm	
L6	grade 3B Ferroxcube wideband RF choke			4312 020 36640
R1	0.4 W metal film resistor	22 Ω		
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

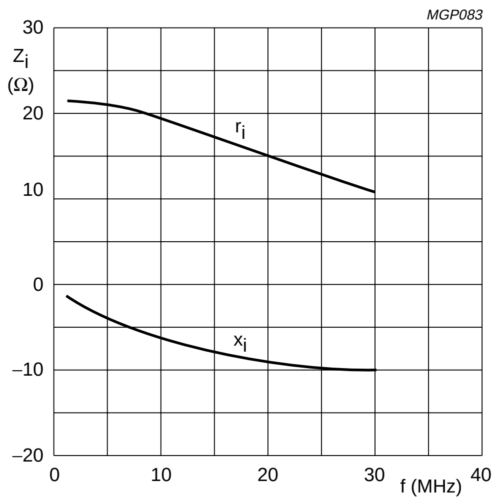
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness 1.6 mm.



Dimensions in mm.

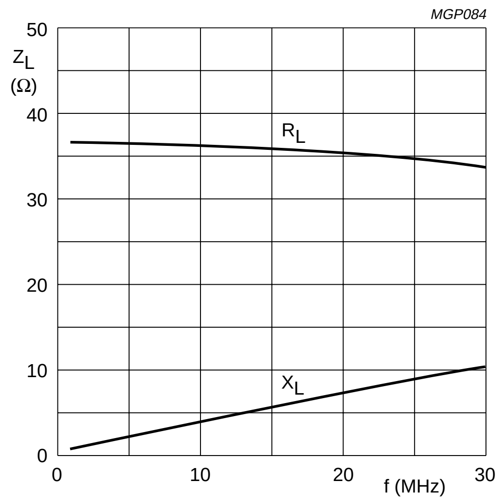
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

Fig.20 Component layout for 28 MHz class-AB test circuit.



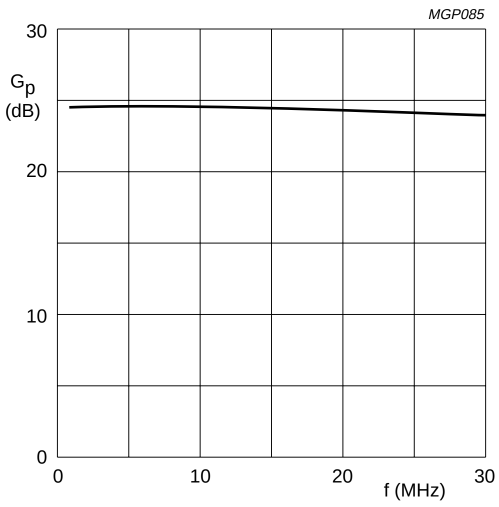
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.21 Input impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.22 Load impedance as a function of frequency (series components); typical values.



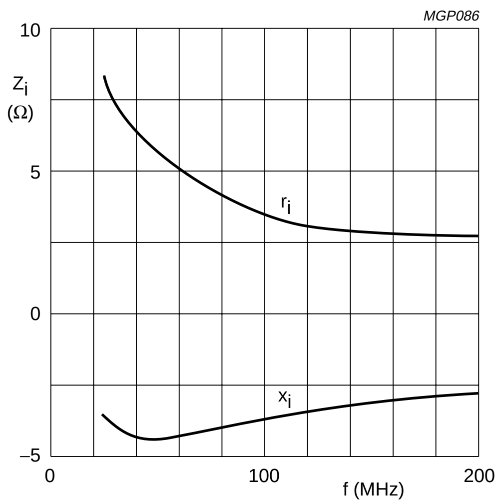
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.23 Power gain as a function of frequency; typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

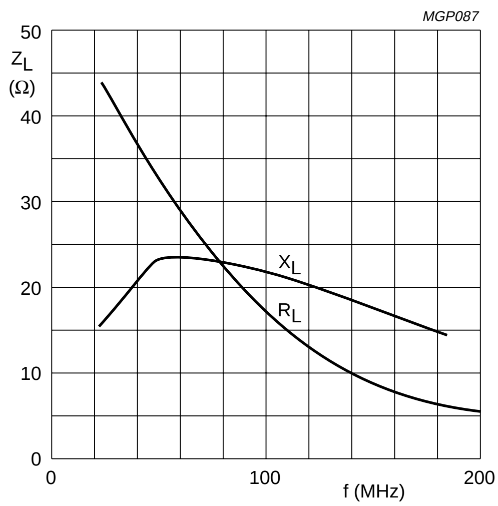
RF performance in SSB operation in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	R_{GS} (Ω)
CW, class-B	108	50	30	30	typ. 20	typ. 65	10



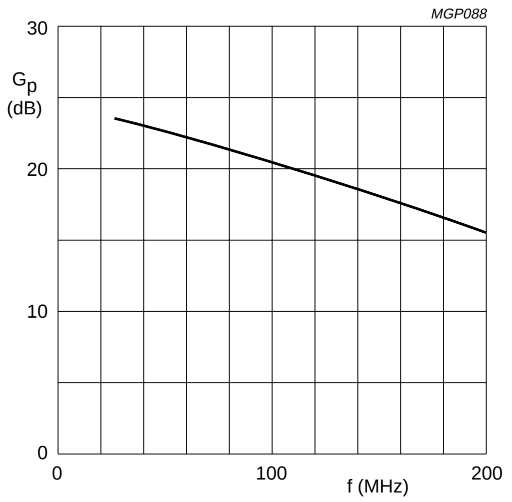
Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.24 Input impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.25 Load impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.26 Power gain as a function of frequency; typical values.

BLF175 scattering parameters

V_{DS} = 50 V; I_D = 100 mA; note 1.

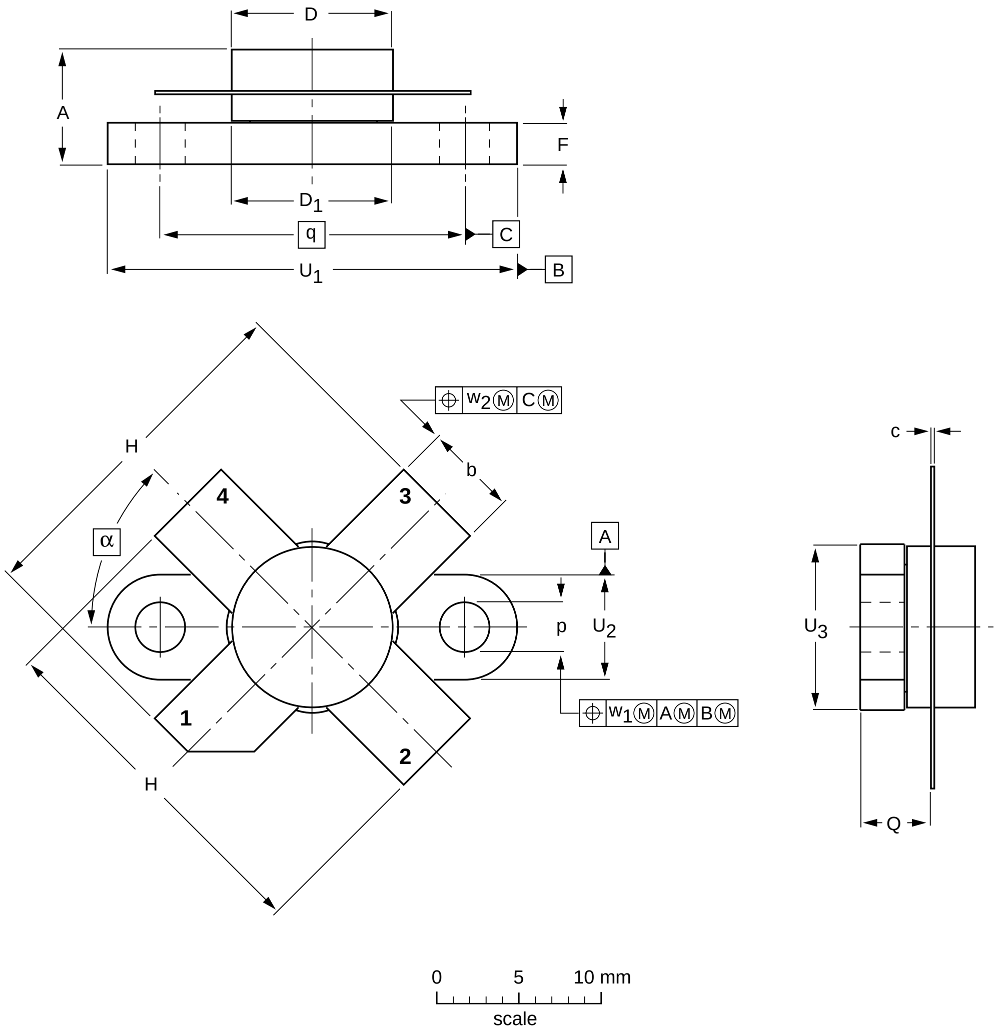
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\lvert s_{11} \rvert$	∠ Φ	$\lvert s_{21} \rvert$	∠ Φ	$\lvert s_{12} \rvert$	∠ Φ	$\lvert s_{22} \rvert$	∠ Φ
5	0.86	–110.20	36.90	114.20	0.02	25.20	0.64	–84.90
10	0.83	–139.40	20.39	93.30	0.02	5.10	0.55	–112.00
20	0.85	–155.70	9.82	72.60	0.02	–13.40	0.60	–129.30
30	0.88	–161.50	5.96	59.30	0.02	–24.70	0.69	–138.00
40	0.90	–164.90	3.98	49.30	0.02	–31.70	0.76	–144.30
50	0.92	–167.10	2.83	41.90	0.01	–35.80	0.82	–149.30
60	0.94	–169.00	2.11	36.00	0.01	–36.80	0.86	–153.50
70	0.96	–170.70	1.63	31.20	0.01	–33.70	0.89	–157.00
80	0.96	–172.20	1.29	27.40	0.00	–23.00	0.91	–159.90
90	0.97	–173.40	1.04	24.20	0.00	3.30	0.92	–162.40
100	0.97	–174.30	0.86	21.70	0.00	42.50	0.94	–164.50
125	0.99	–176.50	0.57	16.40	0.01	81.60	0.95	–168.80
150	0.99	–178.10	0.40	13.40	0.01	88.70	0.97	–171.90
175	0.99	–179.80	0.30	11.60	0.02	90.70	0.98	–174.50
200	1.00	179.20	0.23	11.00	0.02	90.80	0.98	–176.70
250	1.00	177.00	0.15	11.70	0.03	90.50	0.99	179.80
300	1.00	175.10	0.11	16.70	0.03	89.60	0.99	176.90
350	0.99	173.30	0.08	24.10	0.04	88.30	0.99	174.30
400	1.00	171.80	0.07	33.10	0.05	88.00	0.99	171.90
450	0.99	170.10	0.07	42.70	0.05	87.80	0.99	169.60
500	0.99	168.50	0.07	51.90	0.06	86.50	0.99	167.40
600	0.99	165.40	0.07	64.20	0.07	84.90	0.99	163.10
700	0.99	162.30	0.09	70.60	0.09	83.10	0.98	158.90
800	0.99	158.90	0.10	73.80	0.10	82.20	0.98	154.80
900	0.99	155.30	0.12	74.90	0.12	80.70	0.97	150.60
1000	0.98	151.80	0.14	76.40	0.14	79.80	0.97	146.20

Note

1. For more extensive s-parameters see internet website: http://www.semiconductors.philips.com.markets/communications/wirelesscommunicationms/broadcast

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads **SOT123A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.78 9.42	2.72 2.31	20.71 19.93	3.33 3.04	4.63 4.11	18.42	24.87 24.64	6.48 6.22	9.78 9.39	0.25	0.51	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.385 0.371	0.107 0.091	0.815 0.785	0.131 0.120	0.182 0.162	0.725	0.980 0.970	0.255 0.245	0.385 0.370	0.010	0.020	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						99-03-29

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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SCA75

Printed in The Netherlands 613524/03/pp21 Date of release: 2003 Jul 22 Document order number: 9397 750 11582

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