500mA CMOS LDO Regulator

FEATURES

- **Guaranteed 500mA peak output current**
- **Low dropout voltage of 300mV typical at 500mA**
- **Stable with ceramic output capacitor**
- **External 10nF bypass capacitor for low noise**
- **Quick-start feature**
- **Under voltage lockout**
- **No-load ground current of 55µA typical**
- **Full-load ground current of 85µA typical**
- **±1.0% initial accuracy ($V_{OUT} \geq 2.0V$)**
- **±2.0% accuracy over temperature ($V_{OUT} \geq 2.0V$)**
- **"Zero" current shutdown mode**
- **Current limit and thermal protection**
- **5-lead TSOT-23 and 6-pad TDFN packages**

APPLICATIONS

- **Cellular phones**
- **Battery-powered devices**
- **Consumer Electronics**

DESCRIPTION

The CAT6219 is a 500mA CMOS low dropout regulator that provides fast response time during load current and line voltage changes.

The quick-start feature allows the use of an external bypass capacitor to reduce the overall output noise without affecting the turn-on time of just 150µs.

With zero shutdown current and low ground current of 55µA typical, the CAT6219 is ideal for battery-operated devices with supply voltages from 2.3V to 5.5V. An internal under voltage lockout circuit disables the output at supply voltages under 2.15V typical.

The CAT6219 offers 1% initial accuracy and low dropout voltage, 300mV typical at 500mA. Stable operation is provided with a small value ceramic capacitor, reducing required board space and component cost.

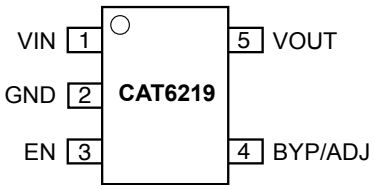
Other features include current limit and thermal protection.

The LDO is available in fixed and adjustable output in the low profile (1mm max height) 5-lead TSOT23 and in the 6-pad 2mm x 2mm TDFN packages.

For Ordering Information details, see page 9.

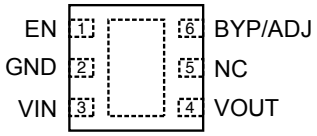
PIN CONFIGURATION

5-Lead TSOT-23
(1mm height)



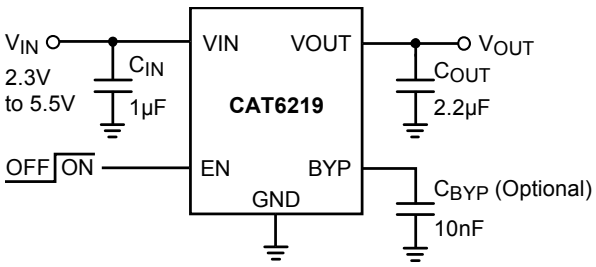
Top View

6-Pad TDFN
(2mm x 2mm)



Top View

TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTIONS

Pin #	Name	Function
1	VIN	Supply voltage input.
2	GND	Ground reference.
3	EN	Enable input (active high); a 2.5MΩ pull-down resistor is provided.
4	BYP	Optional bypass capacitor connection for noise reduction and PSRR enhancing.
4	ADJ	Adjustable input. Feedback pin connected to resistor divider.
5	VOUT	LDO Output Voltage.

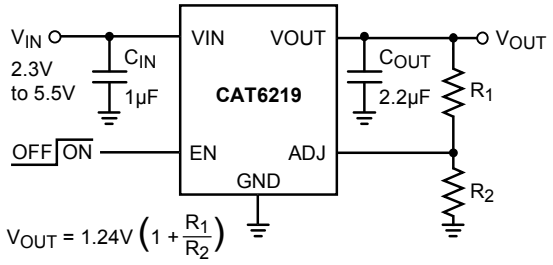


Figure 1. Adjustable Output LDO

PIN FUNCTION

VIN is the supply pin for the LDO. A small 1µF ceramic bypass capacitor is required between the V_{IN} pin and ground near the device. When using longer connections to the power supply, C_{IN} value can be increased without limit. The operating input voltage range is from 2.3V to 5.5V.

EN is the enable control logic (active high) for the regulator output. It has a 2.5MΩ pull-down resistor, which assures that if EN pin is left open, the circuit is disabled.

VOUT is the LDO regulator output. A small 2.2µF ceramic bypass capacitor is required between the VOUT pin and ground. For better transient response, its value can be increased to 4.7µF.

The capacitor should be located near the device. For the SOT23-5 package, a continuous 500mA output current may turn-on the thermal protection. A 250Ω internal shutdown switch discharges the output capacitor in the no-load condition.

GND is the ground reference for the LDO. The pin must be connected to the ground plane on the PCB.

BYP is the reference bypass pin. An optional 0.01µF capacitor can be connected between BYP pin and GND to reduce the output noise and enhance the PSRR at high frequency.

ADJ is the adjustable input pin for the adjustable LDO. The pin is connected to the resistor voltage divider.

ABSOLUTE MAXIMUM RATINGS [(1)]

Parameter	Rating	Unit
V_{IN}	0 to 6.5	V
V_{EN}, V_{OUT}	-0.3 to V_{IN}+0.3	V
Junction Temperature, T_J	+150	°C
Power Dissipation, P_D	Internally Limited [(2)]	mW
Storage Temperature Range, T_S	-65 to +150	°C
Lead Temperature (soldering, 5 sec.)	260	°C
ESD Rating (Human Body Model)	3	kV

RECOMMENDED OPERATING CONDITIONS [(3)]

Parameter	Range	Unit
V_{IN}	2.3 to 5.5	V
V_{EN}	0 to V_{IN}	V
Junction Temperature Range, T_J	-40 to +125	°C
Package Thermal Resistance (SOT23-5), θ_{JA}	235	°C/W

Typical application circuit with external components is shown on page 1.

Notes:

(1) Exceeding maximum rating may damage the device.

(2) The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

(3) The device is not guaranteed to work outside its operating rating.

ELECTRICAL OPERATING CHARACTERISTICS [1]

V_{IN} = V_{OUT} + 1.0V, V_{EN} = High, I_{OUT} = 100µA, C_{IN} = 1µF, C_{OUT} = 2.2µF, ambient temperature of 25ºC (over recommended operating conditions unless specified otherwise). **Bold numbers** apply for the entire junction temperature range.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OUT-ACC}$	Output Voltage Accuracy	Initial accuracy for $V_{OUT} \geq 2.0V$ [4]	-1.0		+1.0	%
			-2.0		**+2.0**	
TC_{OUT}	Output Voltage Temp. Coefficient			40		ppm/ºC
V_{R-LINE}	Line Regulation	V_{IN} = V_{OUT} + 1.0V to 5.5V	-0.2	±0.1	+0.2	%/V
			-0.4		**+0.4**	
V_{R-LOAD}	Load Regulation	I_{OUT} = 100µA to 500 mA		1	1.5	%
					2	
V_{DROP}	Dropout Voltage [2]	I_{OUT} = 500mA		300	400	mV
					500	
I_{GND}	Ground Current	I_{OUT} = 0µA		55	75	µA
					90	
		I_{OUT} = 500mA		85		
I_{GND-SD}	Shutdown Ground Current	V_{EN} < 0.4V			1	µA
					2	
PSRR	Power Supply Rejection Ratio	f = 1kHz, C_{BYP} = 10nF		64		dB
		f = 20kHz, C_{BYP} = 10nF		54		
I_{SC}	Output short circuit current limit	V_{OUT} = 0V	**600**	800		mA
T_{ON}	Turn-On Time	C_{BYP} = 10nF		150		µs
e_N	Output Noise Voltage [3]	BW = 10Hz to 100kHz		45		µVrms
R_{OUT-SH}	Shutdown Switch Resistance			250		Ω
R_{EN}	Enable pull-down resistor			2.5		MΩ
$V_{IN-UVLO}$	Under voltage lockout threshold			2.15		V
ESR	C_{OUT} equivalent series resistance		5		500	mΩ
V_{ADJ}	Adjustable input voltage	I_{OUT} = 100µA	1.2	1.24	1.27	V
Enable Input						
V_{HI}	Logic High Level	V_{IN} = 2.3 to 5.5V	**1.8**			V
		V_{IN} = 2.3 to 5.5V, 0ºC to +125ºC junction temperature	1.6			
V_{LO}	Logic Low Level	V_{IN} = 2.3 to 5.5V			**0.4**	V
I_{EN}	Enable Input Current	V_{EN} = 0.4V		0.15	1	µA
		V_{EN} = V_{IN}		1.5	4	
Thermal Protection						
T_{SD}	Thermal Shutdown			160		ºC
T_{HYS}	Thermal Hysteresis			10		ºC

Notes:

(1) Specification for 2.85V output version unless specified otherwise.

(2) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. During test, the input voltage stays always above the minimum 2.3V.

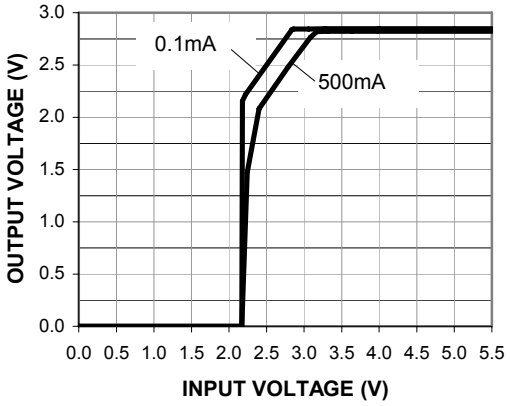
(3) Specification for 1.8V output version.

(4) For VOUT < 2.0V, the initial accuracy is ±2% and across temperature ±3%.

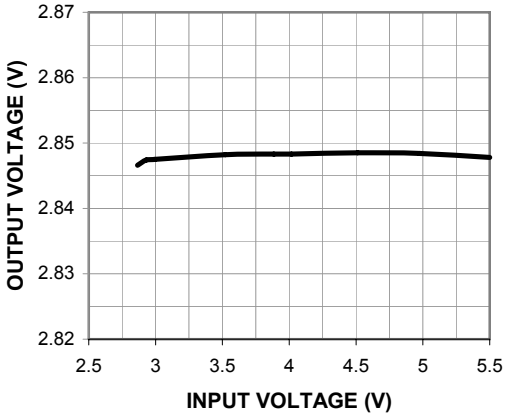
TYPICAL CHARACTERISTICS (shown for 2.85V output version)

V_{IN} = 3.85V, I_{OUT} = 100µA, C_{IN} = 1µF, C_{OUT} = 2.2µF, C_{BYP} = 10nF, T_A = 25°C unless otherwise specified.

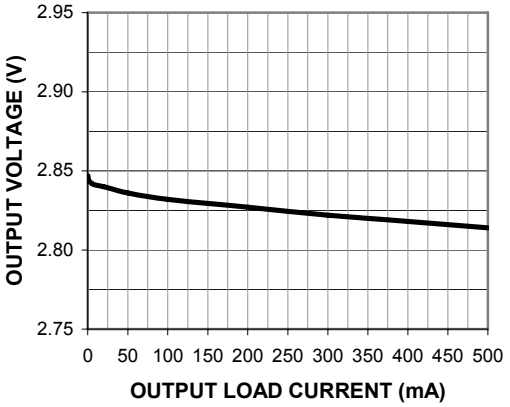
Dropout Characteristics



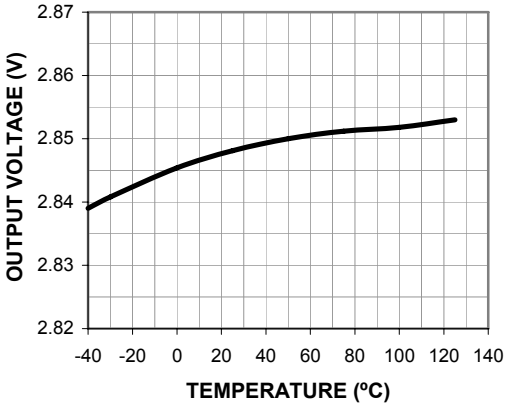
Line Regulation



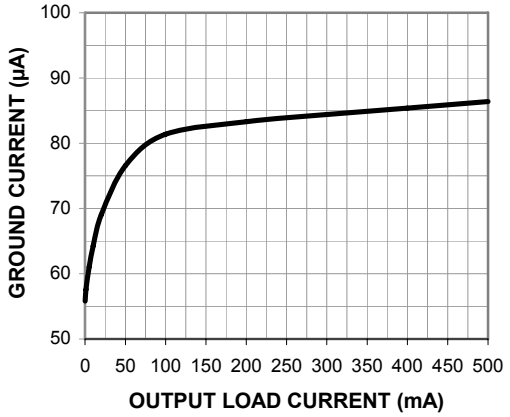
Load Regulation



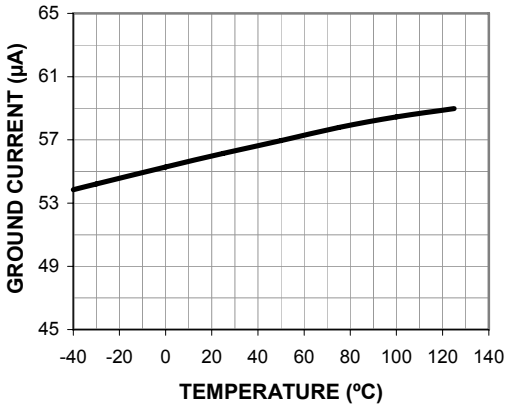
Output Voltage vs. Temperature



Ground Current vs. Load Current



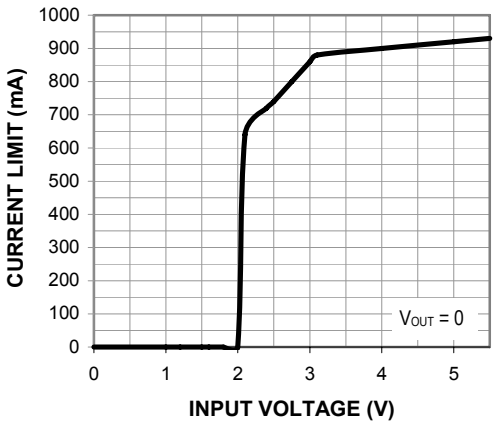
Ground Current vs. Temperature



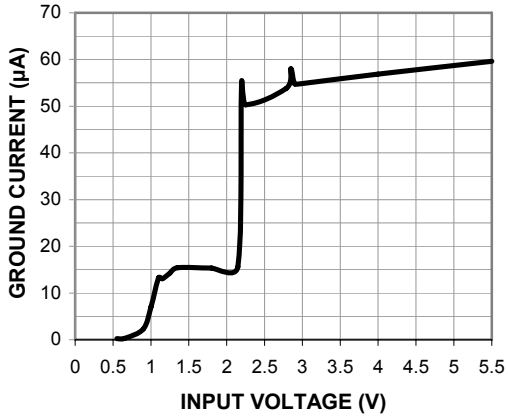
TYPICAL CHARACTERISTICS (shown for 2.85V output option)

V_{IN} = 3.85V, I_{OUT} = 100µA, C_{IN} = 1µF, C_{OUT} = 2.2µF, C_{BYP} = 10nF, T_A = 25°C unless otherwise specified.

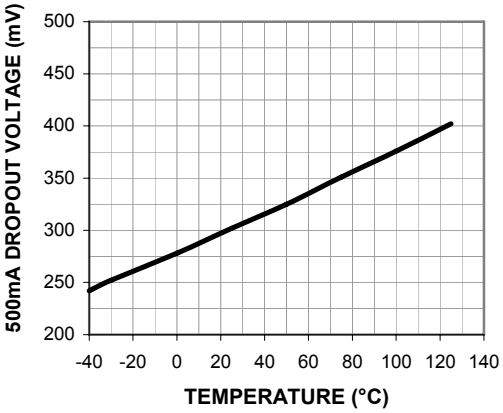
Output Short-circuit Current vs. Input Voltage



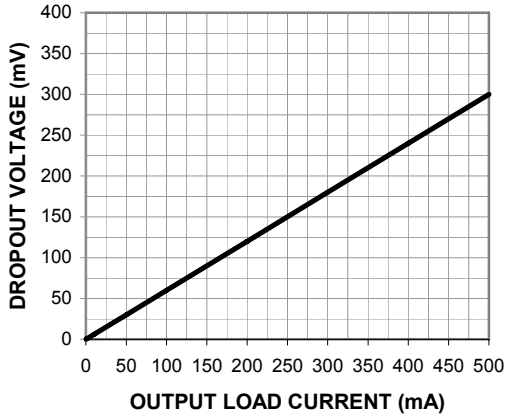
Ground Current vs. Input Voltage



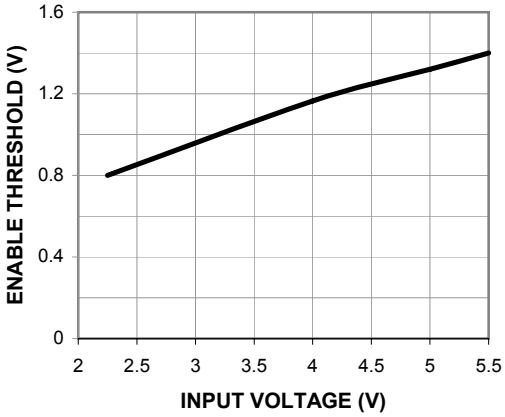
Dropout vs. Temperature (500mA Load)



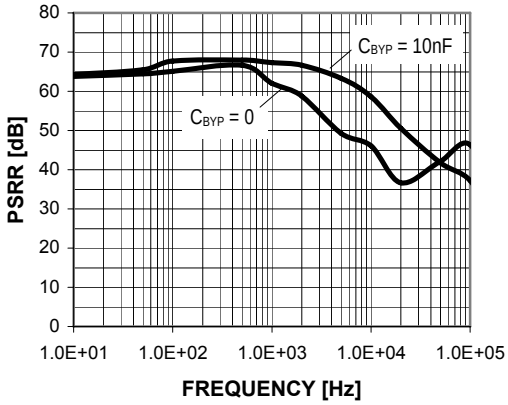
Dropout vs. Load Current



Enable Threshold vs. Input Voltage



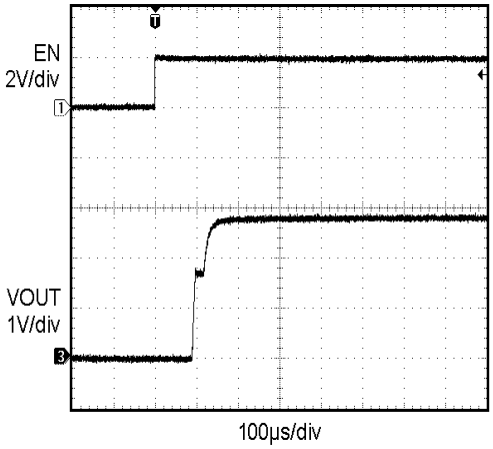
PSRR vs. Frequency (10mA Load)



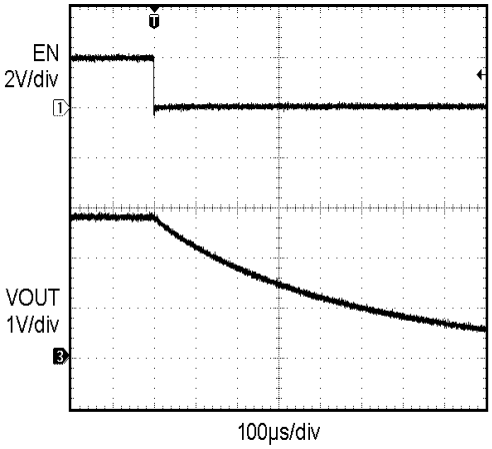
TRANSIENT CHARACTERISTICS (shown for 2.85V output option)

V_{IN} = 3.85V, I_{OUT} = 100µA, C_{IN} = 1µF, C_{OUT} = 2.2µF, C_{BYP} = 10nF, T_A = 25°C unless otherwise specified.

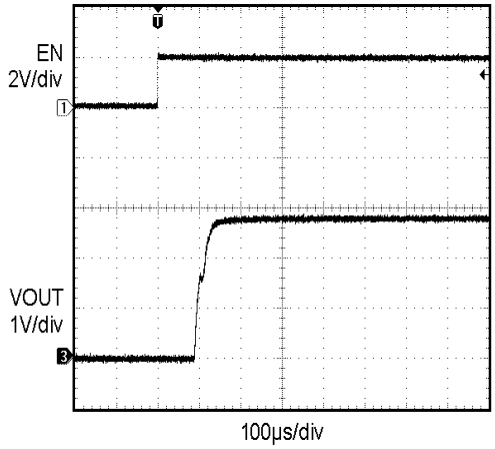
Enable Turn-On (100µA Load)



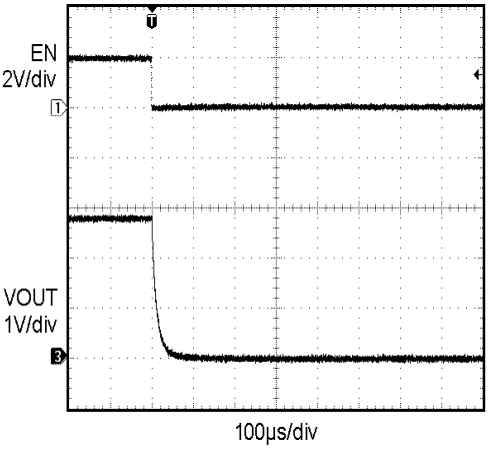
Enable Turn-Off (100µA Load)



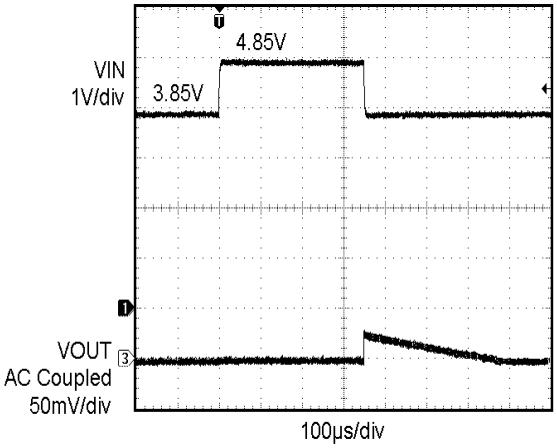
Enable Turn-On (500mA Load)



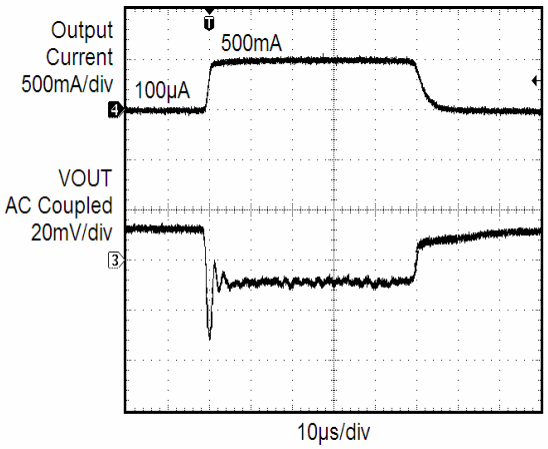
Enable Turn-Off (500mA Load)



Line Transient Response (3.85V to 4.85V)

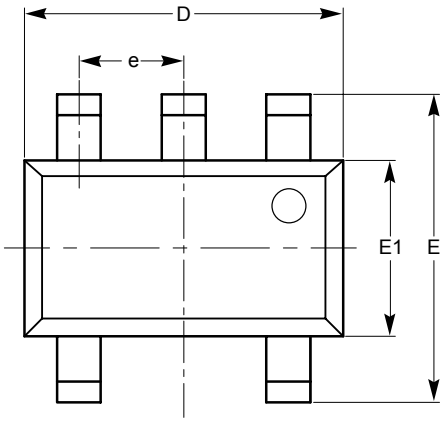


Load Transient Response (0.1mA to 500mA)



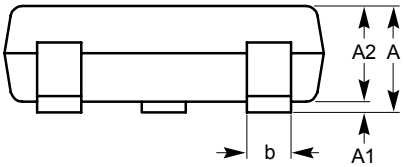
PACKAGE OUTLINE DRAWINGS

TSOT-23 5-Lead (TD) (1)(2)

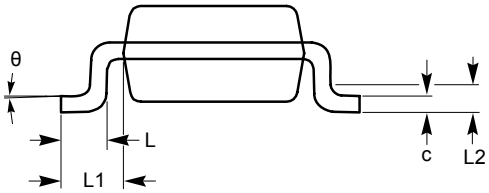


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
θ	0º		8º



SIDE VIEW



END VIEW

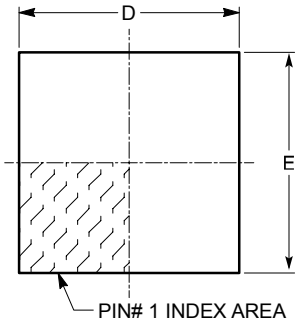
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

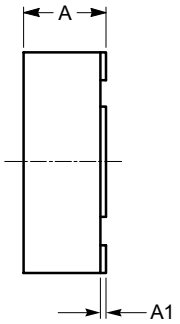
(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC standard MO-193.

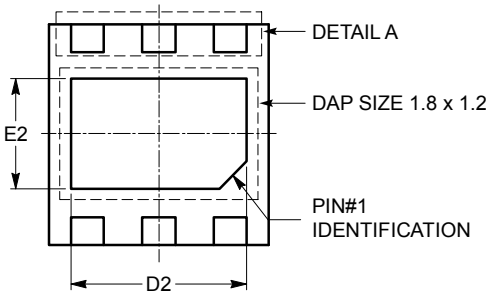
TDFN 6-Pad 2mm x 2mm (VP5) (1)(2)



TOP VIEW

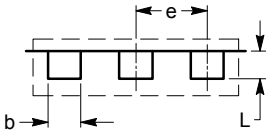


SIDE VIEW

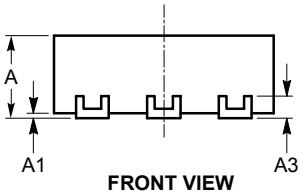


BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e		0.65 TYP	
L	0.15	0.25	0.35



DETAIL A



FRONT VIEW

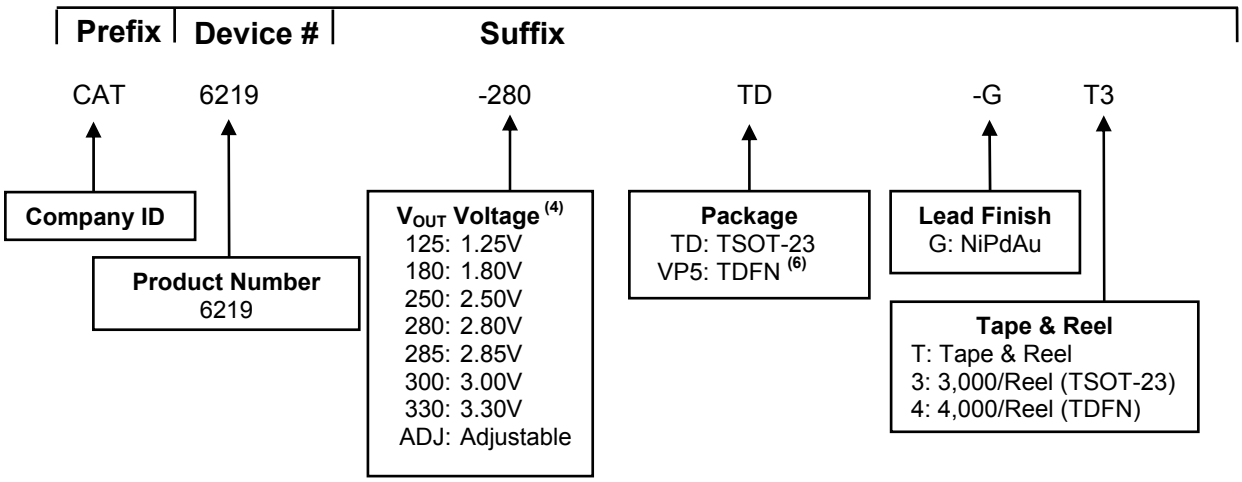
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC standard MO-229.

EXAMPLE OF ORDERING INFORMATION



Ordering Number	V_{OUT} Voltage(5)	Package	Quantity per Reel
CAT6219-125TD-GT3	1.25V	TSOT-23-5	3,000
CAT6219-180TD-GT3	1.80V	TSOT-23-5	3,000
CAT6219-250TD-GT3	2.50V	TSOT-23-5	3,000
CAT6219-280TD-GT3	2.80V	TSOT-23-5	3,000
CAT6219-285TD-GT3 (4)	2.85V	TSOT-23-5	3,000
CAT6219-300TD-GT3	3.00V	TSOT-23-5	3,000
CAT6219-330TD-GT3	3.30V	TSOT-23-5	3,000
CAT6219-ADJTD-GT3	1.25V to 5V	TSOT-23-5	3,000
CAT6219-330VP5-GT4	3.30V	TDFN-6	4,000

For Product Top Mark Codes, click here:
http://www.catsemi.com/techsupport/producttopmark.asp

Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu pre-plated (PPF) lead frames.
(3) The device used in the above example is a CAT6219-280TD-GT3 (V_{OUT} = 2.80V, in a TSOT-23 package, NiPdAu, Tape & Reel, 3,000/Reel).
(4) Standard voltages are 1.80V, 2.80V and 3.30V. For other voltage options, please contact your nearest Catalyst Semiconductor Sales office.
(5) All output voltage options have the same marking.
(6) Contact factory for availability.
(7) Package Marking for CAT6219 family is “RV.

REVISION HISTORY

Date	Rev.	Reason
20-Apr-07	A	Initial Release
07-Nov-07	B	Update Package Outline Drawings Update Example of Ordering Information Add “MD-“ to Document Number
08-Feb-08	C	Update Electrical Operating Characteristics
20-May-08	D	Add Adjustable and other voltage options Update Package Outline Drawing – TDFN 6-Pad Add link to Top Mark Codes

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Document No: MD-10009
Revision: D
Issue date: 05/20/08