Features

- **Fast**
  - **— CY7C901–23 has a 23-ns read-modify-write cycle; Commercial 25% faster than "C" Spec 2901**
  - **— CY7C901–27 has a 27-ns read-modify-write cycle; Military 15% faster than "C" Spec 2901**
- **Low power**
  - **— 70 mA (commercial)**
  - **— 90 mA (military)**
- **V_{CC} of 5V ±10% (commercial and military)**
- **Eight-function ALU**
- **Infinitely expandable in 4-bit increments**
- **Four status flags: carry, overflow, negative, zero**
- **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functional equivalent to Am2901B, C**

Functional Description

The CY7C901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU, and the required data manipulation and control logic.

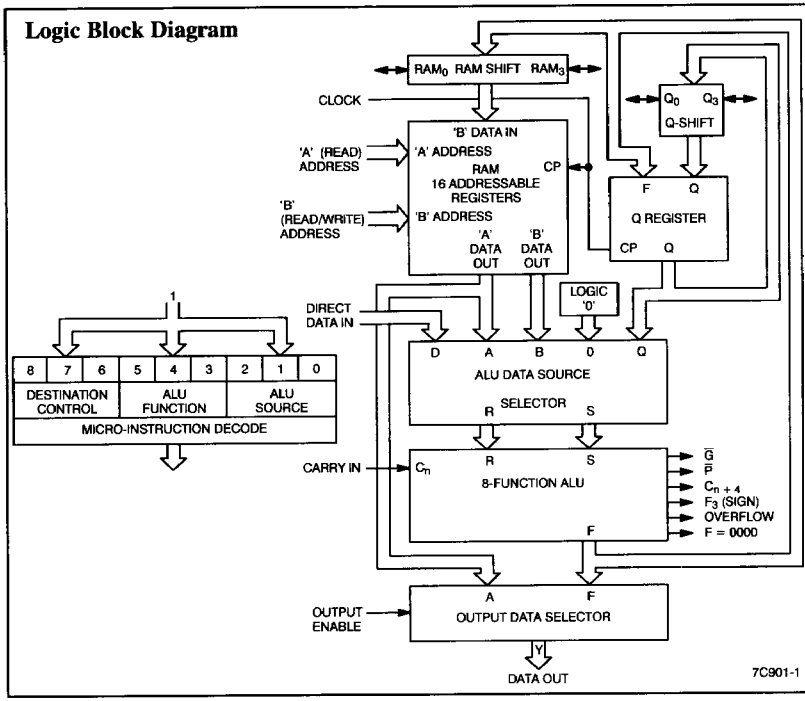
The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from a micro-instruction register.

The CY7C901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full look-ahead carry or a ripple carry.

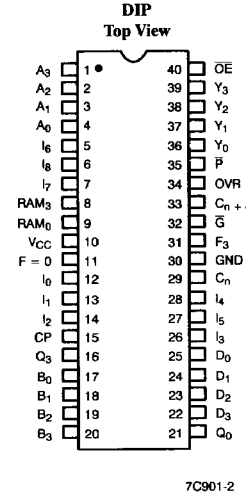
The CY7C901 is a pin-compatible, functionally equivalent, improved-performance replacement for the Am2901.

The CY7C901 is fabricated using an advanced 1.2-micron CMOS process that eliminates latch-up, provides ESD protection over 2000V, and achieves superior performance at low-power dissipation.

Logic Block Diagram



Pin Configurations

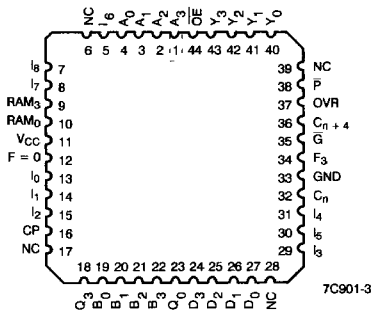


Selection Guide

Minimum Read-Modify-Write Cycle (ns)	Maximum Operating I_{CC} (mA)	Operating Range	Part Number
23	80	Commercial	CY7C901–23
27	90	Military	CY7C901–27
31	70	Commercial	CY7C901–31
32	90	Military	CY7C901–32

Pin Configurations (continued)

LCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 11 to Pin 33) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current (Outputs) ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	− 55°C to +125°C	5V ±10%

Notes:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_3$	I	These four address lines select one of the registers in the stack and output its contents on the (internal) A port.
$B_0 - B_3$	I	These four address lines select one of the registers in the stack and output its contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
$I_0 - I_8$	I	These nine instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$), and what data is to be written into either the Q register or the register file ($I_{6, 7, 8}$).
$D_0 - D_3$	I	These are four data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
$Y_0 - Y_3$	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the $Y_0 - Y_3$ outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high-impedance state.
CP	I	Clock Input. The LOW level of the clock writes data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL-compatible CMOS inputs. **Outputs:** When the destination code on lines $I_{6, 7, 8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM_3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.

6 LOGIC

Pin Definitions (continued)

Signal Name	I/O	Description
$\overline{G}$, $\overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4 bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only when the sign bits of the operands are identical (add) or opposite (substract).
F = 0	O	Open collector output that goes HIGH if the data on the ALU outputs ($F_{0,1,2,3}$) are all LOW. It indicates that the result of an ALU operation is zero.
F_3	O	The most significant bit of the ALU output.

Description of Architecture

General Description

A block diagram of the CY7C901 is shown in *Figure 1*. The circuit is a 4-bit slice consisting of a register file (16 x 4 dual-port RAM), the ALU, the Q register, and the necessary control logic. It is expandable in 4-bit increments.

RAM

The RAM is addressed by two 4-bit address fields ($A_0 - A_3$, $B_0 - B_3$) that cause the data to appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

New data is written into the RAM location specified by the B address when the RAM write enable (RAM $\overline{EN}$) is active and clock input is LOW. Each of the four RAM inputs is driven by a 3-input multiplexer that allows the outputs of the ALU ($F_{0,1,2,3}$) to be shifted one bit position to the left, the right, or not to be shifted. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins.

For a shift left (up) operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. For a shift right (down) operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled.

The data to be written into the RAM is applied to the D inputs of the CY7C901 and is passed (unchanged) through the ALU to the RAM location addressed by the B word address.

The outputs of the RAM A and B ports drive separate 4-bit latches that are enabled (follow the RAM data) when the clock is HIGH. The outputs of the A latches go to three multiplexers whose outputs drive the two inputs to the ALU ($R_{0,1,2,3}$) and ($S_{0,1,2,3}$) and the ($Y_{0,1,2,3}$) chip outputs.

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on two 4-bit input words, R and S. The R inputs are driven from four 2-input multiplexers whose inputs are from either the (RAM) A-port or the external data (D) inputs. The S inputs are driven from four 3-input multiplexers whose inputs are from the A-port, the B-port, or the Q register. Both multiplexers are controlled by the $I_{0,1,2}$ inputs as shown in *Table 1*. This configuration of multiplexers on the ALU R and S inputs enables the user to select eight pairs of combinations of A, B, D, Q, and "0" (unselected) inputs as 4-bit operands to the ALU. The logical and arithmetic operations performed by the ALU upon the data present at its R and S inputs are tabulated in *Table 2*. The ALU has a carry-in (C_n) input, carry-propagate ($\overline{P}$) output, carry-generate ($\overline{G}$) output, carry-out (C_{n+4}) and overflow (OVR) pins to enable the user to (1) speed up arithmetic operations by implementing carry look-ahead logic and (2) determine if an arithmetic overflow has occurred.

As shown in *Table 3*, the ALU data outputs ($F_{0,1,2,3}$) are routed to the RAM, the Q register inputs, and the Y outputs under control of the $I_{6,7,8}$ control signal inputs. In addition, the MSB of the ALU is output as F3 so that the user can examine the sign bit without enabling the three-state outputs. The F = 0 output, used for zero detection is HIGH when all bits of the F output are LOW. It is an open-drain output which may be wire ORed across multiple 7C901 processor slices.

Q Register

The Q register functions as an accumulator or temporary storage register. Physically it is a 4-bit register implemented with master-slave latches. The inputs to the Q register are driven by the outputs from four 3-input multiplexers under control of the $I_{6,7,8}$ inputs. The Q_0 and Q_3 I/O pins function in a manner similar to the RAM_0 and RAM_3 pins. The other inputs to the multiplexer enable the contents of the Q register to be shifted up or down, or the outputs of the ALU to be entered into the master latches. Data is entered into the master latches when the clock is LOW and transferred from master to slave (output) when the clock changes from LOW to HIGH.

ALU Source Operand and ALU Functions

The ALU source operands and ALU function matrix is summarized in *Table 4* and separated by logic operation or arithmetic operation in *Tables 5* and *6*, respectively. The $I_{0,1,2}$ lines select eight pairs of source operands and the $I_{3,4,5}$ lines select the operation to be performed. The carry-in (C_n) signal affects the arithmetic result and the internal flags; not the logical operations.

Conventional Addition and Pass-Increment/Decrement

When the carry-in is HIGH and either a conventional addition or a pass operation is performed, one (1) is added to the result. If the decrement operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the decrement operation so that the result is equivalent to the pass operation.

Subtraction

Recall that in two's complement integer coding − 1 is equal to all ones, and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In *Table 6* the symbol − Q represents the two's complement of Q so that the one's complement of Q is then − Q − 1.

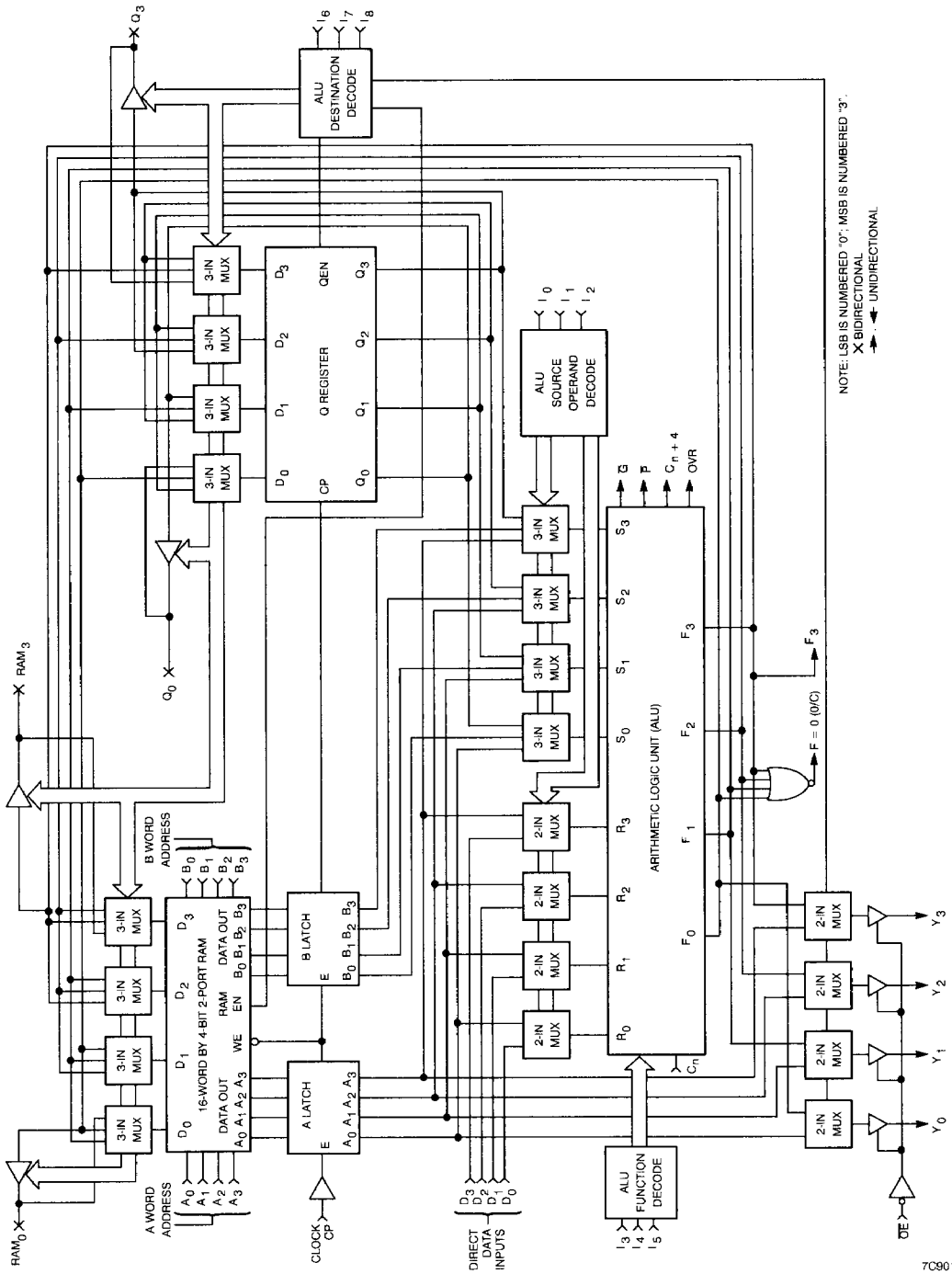


Figure 1. CY7C901 Block Diagram

Functional Tables

Table 1. ALU Source Operand Control

Mnemonic	Micro Code I_2	I_1	I_0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Table 2. ALU Function Control

Mnemonic	Micro Code I_5	I_4	I_3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
XOR	H	H	L	6	R XOR S	R ∨ S
XNOR	H	H	H	7	R XNOR S	$\overline{R \vee S}$

Table 3. ALU Destination Control

Mnemonic	Micro Code I_8	I_7	I_6	Octal Code	RAM Function Shift	Load	Q-Reg. Function Shift	Load	Y Output	RAM Shifter RAM_0	RAM_3	Q Shifter Q_0	Q_3
QREG	L	L	L	0	X	None	None	F ↓ Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F ↓ B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F ↓ B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 ↓ B	DOWN	Q/2 ↓ Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 ↓ B	X	None	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F ↓ B	UP	2Q ↓ Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F ↓ B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output that is in the high-impedance state.
A = Register addressed by A inputs.
B = Register addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Table 4. Source Operand and ALU Function Matrix

Octal I_{543}	I_{210} Octal / ALU Source / ALU Function	0 A, Q	1 A, B	2 O, Q	3 O, B	4 O, A	5 D, A	6 D, Q	7 D, O
0	C_n = L R plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R XOR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
7	R XNOR S	$\overline{A \vee Q}$	$\overline{A \vee B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \vee A}$	$\overline{D \vee Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∨ = XOR

Table 5. ALU Logic Mode Functions

Octal I_{543}, I_{210}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee Q$
60	XOR	$A \veebar Q$
61		$A \veebar B$
65		$D \veebar A$
66		$D \veebar Q$
70	XNOR	$\overline{A \veebar Q}$
71		$\overline{A \veebar B}$
75		$\overline{D \veebar A}$
76		$\overline{D \veebar Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I_{543}, I_{210}	C_n = 0 (LOW)		C_n = 1 (HIGH)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q − 1	PASS	Q
13		B − 1		B
14		A − 1		A
27		D − 1		D
22	1's Comp.	− Q − 1	2's Comp. (Negate)	− Q
23		− B − 1		− B
24		− A − 1		− A
17		− D − 1		− D
10	Subtract (1's Comp.)	Q − A − 1	Subtract (2's Comp.)	Q − A
11		B − A − 1		B − A
15		A − D − 1		A − D
16		Q − D − 1		Q − D
20		A − Q − 1		A − Q
21		A − B − 1		A − B
25		D − A − 1		D − A
26		D − Q − 1		D − Q

Logic Functions for $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the CY7C901 is in the add or subtract mode. *Table 7* indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to *Table 1*.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

Table 7. $\overline{G}$, $\overline{P}$, C_{n+n} and OVR Logic Functions

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \veebar C_4$
1	S − R	⧫ Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions ⧫			
2	R − S	⧫ Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions ⧫			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	⧫ Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions ⧫		
6	R ⊻ S	⧫ Same as $\overline{R \veebar S}$, but substitute $\overline{R_i}$ for R_i in definitions ⧫			
7	$\overline{R \veebar S}$	$G_3+G_2+G_1+G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + C_n)}$	Note 2

Notes:

2. $[P_2 + G_2P_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \veebar [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$
   + = OR

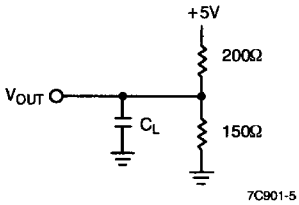
Electrical Characteristics Over Commercial and Military Operating Range[3, 4]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20 mA Commercial, 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.		− 10	10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V		− 3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V	Commercial	20		mA
			Military	16		
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = V_{SS} to V_{CC}		−40	+40	μA
I_{SC}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = 0V			− 85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial −31		70	mA
			Commercial −23		80	
			Military −27, −32		90	
I_{CC1}	Supply Current	$V_{IH} \ge V_{CC}$ − 1.2V, 10 MHz, $V_{IL} \le$ 0.4V	Commercial		26.5	mA
			Military		31	

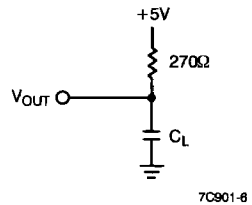
Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Output Loads used for AC Performance Characteristics[7, 8, 9]



All outputs except open drain



Open drain (F = 0)

Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V
5. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
6. Tested initially and after any design or process changes that may affect these parameters.
7. C_L = 50 pF includes scope probe, wiring and stray capacitance.
8. C_L = 5 pF for output disable tests.
9. Loads shown above are for commercial (20 mA) I_{OL} specifications only.

CY7C901–23 Commercial and CY7C901–27 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the commercial (0°C to 70°C) and military (– 55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:
CY7C901–23PC CY7C901–23DC CY7C901–23LC
CY7C901–27JC CY7C901–27DMB CY7C901–27LMB

Cycle Time and Clock Characteristics[2]

CY7C901	–23	–27
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	23 ns	27 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	43 MHz	37 MHz
Minimum Clock LOW Time	13 ns	15 ns
Minimum Clock HIGH Time	10 ns	12 ns
Minimum Clock Period	23 ns	27 ns

Combinatorial Propagation Delays (C_L = 50 pF)[3, 10]

To Output	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0		Q_0	
From Input	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_3		Q_3	
Speed (ns)	23	27	23	27	23	27	23	27	23	27	23	27	23	27	23	27
A, B Address	30	33	30	33	30	33	28	33	30	33	30	33	30	33	—	—
D	21	24	20	23	20	23	20	21	24	25	21	24	22	25	—	—
C_n	17	18	16	17	14	14	—	—	18	19	16	17	18	19	—	—
$I_{0,1,2}$	26	28	25	27	24	26	24	28	25	29	24	27	25	27	—	—
$I_{3,4,5}$	26	27	24	27	24	26	24	26	26	27	24	26	26	27	—	—
$I_{6,7,8}$	16	18	—	—	—	—	—	—	—	—	—	—	21	21	21	21
A Bypass ALU (I = 2XX)	24	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (LOW to HIGH)	24	27	23	26	23	26	23	25	24	27	24	26	24	27	19	20

Set-Up and Hold Times Relative to Clock (CP) Input[3, 10, 11]

	CP: Set-Up Time Before H ⧫ L		Hold Time After H ⧫ L		Set-Up Time Before L ⧫ H		Hold Time After L ⧫ H	
Speed (ns)	23	27	23	27	23	27	23	27
A, B Source Address	10	12	0 (Note 12)		21, 10 + t_{PWL} (Note 13)		0	
B Destination Address	10	12	⧫ Do Not Change ⧫				0	
Data	—	—	—		16		0	
C_n	—	—	—		13		0	
I_{012}	—	—	—		19		0	
I_{345}	—	—	—		19		0	
I_{678}	7	9	⧫ Do Not Change ⧫				0	
$RAM_{0,3}$, $Q_{0,3}$	—	—	—		9		0	

Output Enable/Disable Times[2]

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C901–23	$\overline{OE}$	Y	14	16
CY7C901–27	$\overline{OE}$	Y	16	18

Notes:
10. A dash indicates a propagation delay path or set-up time constraint does not exist.
11. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."
12. Source addresses must be stable prior to the clock H ⧫ L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address can be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
13. The set-up time prior to the clock L ⧫ H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L ⧫ H transition, regardless of when the clock H ⧫ L transition occurs.

CY7C901–31 Commercial and CY7C901–32 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the commercial (0°C to 70°C) and military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:
CY7C901–31PC CY7C901–31DC CY7C901–31LC
CY7C901–31JC CY7C901–32DMB CY7C901–32LMB

Cycle Time and Clock Characteristics[2]

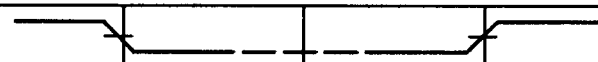
CY7C901	–31	–32
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	31 ns	32 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz	31 MHz
Minimum Clock LOW Time	16 ns	17 ns
Minimum Clock HIGH Time	15 ns	15 ns
Minimum Clock Period	31 ns	32 ns

For faster performance see CY7C901–23 specification on page 9.

Combinatorial Propagation Delays (C_L = 50 pF)[3, 10]

To Output	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0		Q_0	
From Input	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_3		Q_3	
Speed (ns)	31	32	31	32	31	32	31	32	31	32	31	32	31	32	31	32
A, B Address	40	48	40	48	40	48	37	44	40	48	40	48	40	48	—	—
D	30	37	30	37	30	37	30	34	38	40	30	37	30	37	—	—
C_n	22	25	22	25	20	21	—	—	25	28	22	25	25	28	—	—
I_{012}	35	40	35	40	35	40	37	44	37	44	35	40	35	40	—	—
I_{345}	35	40	35	40	35	40	35	40	38	40	35	40	35	40	—	—
I_{678}	25	29	—	—	—	—	—	—	—	—	—	—	26	29	26	29
A Bypass ALU (I = 2XX)	35	40	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (LOW to HIGH)	35	40	35	40	35	40	35	40	35	40	35	40	35	40	28	33

Set-Up and Hold Times Relative to Clock (CP) Input[3, 10, 11]

	CP:  Set-Up Time Before H ⧫ L	Hold Time After H ⧫ L	Set-Up Time Before L ⧫ H	Hold Time After L ⧫ H
A, B Source Address	15	0 (Note 12)	30, 15 + t_{PWL} (Note 13)	0
B Destination Address	15	⧫ Do Not Change ⧫		0
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	⧫ Do Not Change ⧫		0
$RAM_{0,3}$, $Q_{0,3}$	—	—	12	0

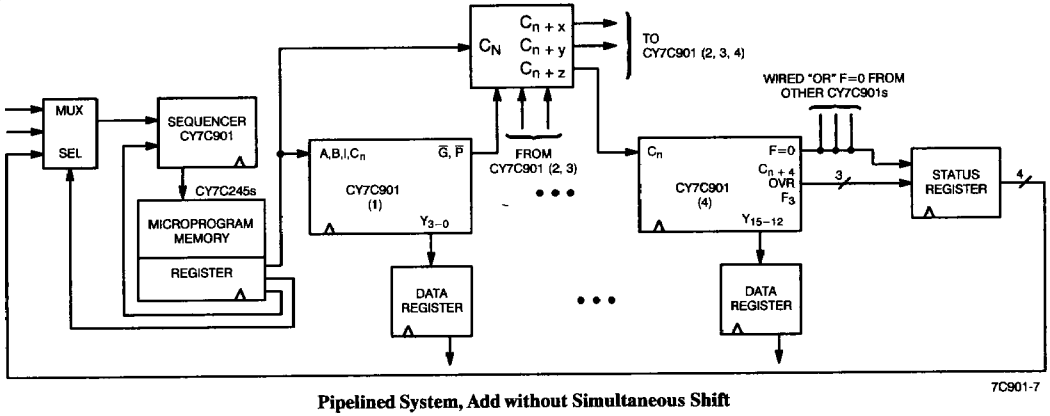
Output Enable/Disable Times[2]

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C901–31	$\overline{OE}$	Y	23	23
CY7C901–32	$\overline{OE}$	Y	25	25

Minimum Cycle Time Calculations for 16-Bit Systems

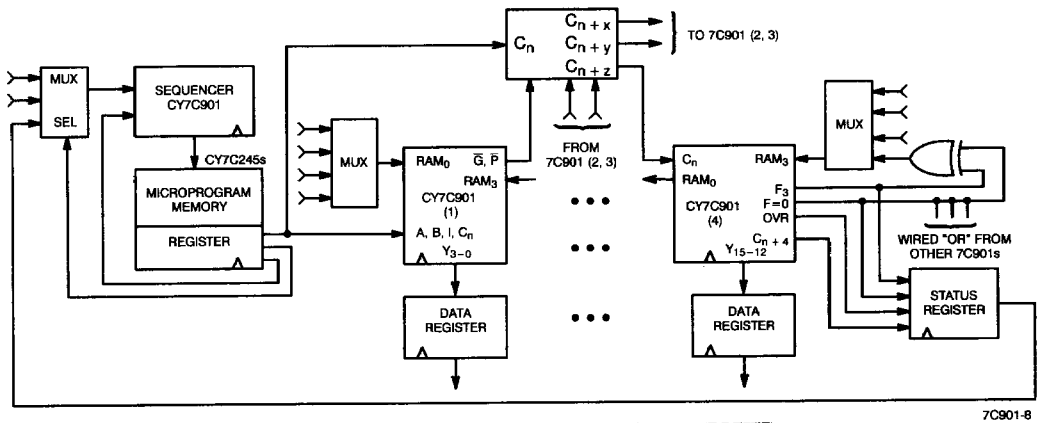
Speed used in calculations for parts other than CY7C901 are representative for MSI parts.



Pipelined System, Add without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28	MUX	Select to Output	12
Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	9	CY7C901	CC to Output	22
CY7C901	C_n to Worst Case	18	CY7C245	Access Time	20
Register	Set-Up	4			66 ns
		71 ns			

Minimum Clock Period = 71 ns



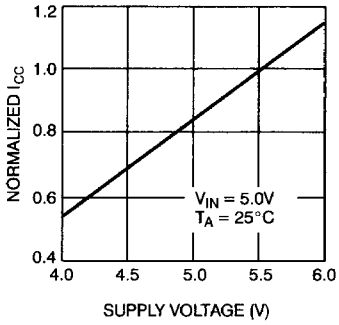
Pipelined System, Simultaneous Add and Shift Down (RIGHT)

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28	MUX	Select to Output	12
Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	9	CY7C901	CC to Output	22
CY7C901	C_n to Worst Case	18	CY7C245	Access Time	20
XOR and MUX	Prop. Delay, Select to Output	20			66 ns
CY7C901	RAM_3 Setup	9			
		96 ns			

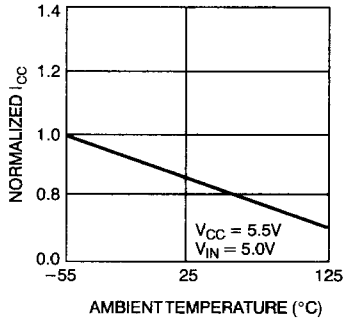
Minimum Clock Period = 96 ns

Typical DC and AC Characteristics

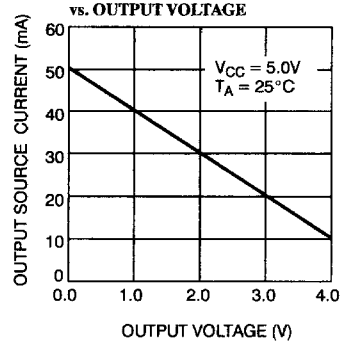
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



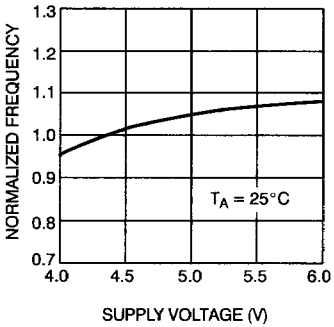
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



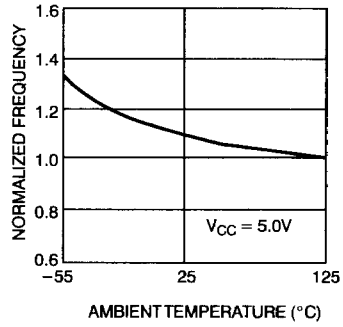
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



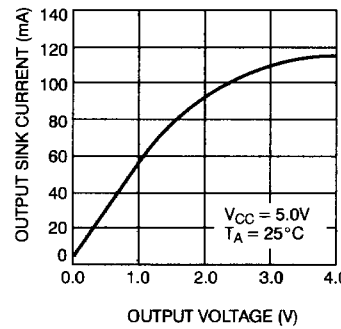
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



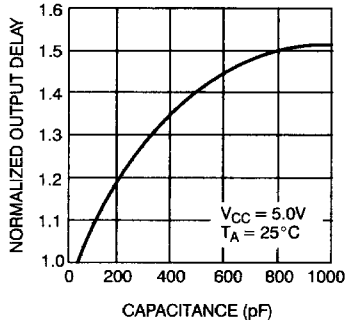
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



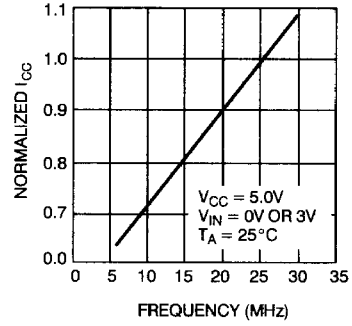
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



7C901-9

6 LOGIC

Ordering Information

Read-Modify-Write Cycle (ns)	Ordering Code	Package Type	Operating Range
23	CY7C901–23DC	D18	Commercial
	CY7C901–23JC	J67	
	CY7C901–23LC	L67	
	CY7C901–23PC	P17	
27	CY7C901–27DMB	D18	Military
	CY7C901–27LMB	L67	
31	CY7C901–31DC	D18	Commercial
	CY7C901–31JC	J67	
	CY7C901–31LC	L67	
	CY7C901–31PC	P17	
32	CY7C901–32DMB	D18	Military
	CY7C901–32LMB	L67	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CC1}	1, 2, 3

Cycle Time and Clock Characteristics

Parameters	Subgroups
Minimum Clock LOW Time	7, 8, 9, 10, 11
Minimum Clock HIGH Time	7, 8, 9, 10, 11

Combinational Propagation Delays

Parameters	Subgroups
From A, B Address to Y	7, 8, 9, 10, 11
From A, B Address to F_3	7, 8, 9, 10, 11
From A, B Address to C_{n+4}	7, 8, 9, 10, 11
From A, B Address to $\overline{G}, \overline{P}$	7, 8, 9, 10, 11
From A, B Address to F = 0	7, 8, 9, 10, 11
From A, B Address to OVR	7, 8, 9, 10, 11
From A, B Address to $RAM_{0,3}$	7, 8, 9, 10, 11
From D to Y	7, 8, 9, 10, 11
From D to F_3	7, 8, 9, 10, 11
From D to C_{n+4}	7, 8, 9, 10, 11
From D to $\overline{G}, \overline{P}$	7, 8, 9, 10, 11
From D to F = 0	7, 8, 9, 10, 11
From D to OVR	7, 8, 9, 10, 11
From D to $RAM_{0,3}$	7, 8, 9, 10, 11
From C_n to Y	7, 8, 9, 10, 11
From C_n to F_3	7, 8, 9, 10, 11
From C_n to C_{n+4}	7, 8, 9, 10, 11
From C_n to F = 0	7, 8, 9, 10, 11
From C_n to OVR	7, 8, 9, 10, 11
From C_n to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{012} to Y	7, 8, 9, 10, 11
From I_{012} to F_3	7, 8, 9, 10, 11
From I_{012} to C_{n+4}	7, 8, 9, 10, 11
From I_{012} to $\overline{G}, \overline{P}$	7, 8, 9, 10, 11
From I_{012} to F = 0	7, 8, 9, 10, 11
From I_{012} to OVR	7, 8, 9, 10, 11
From I_{012} to $RAM_{0,3}$	7, 8, 9, 10, 11

Combinational Propagation Delays (continued)

Parameters	Subgroups
From I_{345} to Y	7, 8, 9, 10, 11
From I_{345} to F_3	7, 8, 9, 10, 11
From I_{345} to C_{n+4}	7, 8, 9, 10, 11
From I_{345} to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From I_{345} to F = 0	7, 8, 9, 10, 11
From I_{345} to OVR	7, 8, 9, 10, 11
From I_{345} to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{678} to Y	7, 8, 9, 10, 11
From I_{678} to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{678} to $Q_{0,3}$	7, 8, 9, 10, 11
From A Bypass ALU to Y (I = 2XX)	7, 8, 9, 10, 11
From Clock LOW to HIGH to Y	7, 8, 9, 10, 11
From Clock LOW to HIGH to F_3	7, 8, 9, 10, 11
From Clock LOW to HIGH to C_{n+4}	7, 8, 9, 10, 11
From Clock LOW to HIGH to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to F = 0	7, 8, 9, 10, 11
From Clock LOW to HIGH to OVR	7, 8, 9, 10, 11
From Clock LOW to HIGH to $RAM_{0,3}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to $Q_{0,3}$	7, 8, 9, 10, 11

Set-Up and Hold Times Relative to Clock (CP) Input

Parameters	Subgroups
A, B Source Address Set-Up Time Before H ↓ L	7, 8, 9, 10, 11
A, B Source Address Hold Time After H ↓ L	7, 8, 9, 10, 11
A, B Source Address Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
A, B Source Address Hold Time After L ↑ H	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before H ↓ L	7, 8, 9, 10, 11
B Destination Address Hold Time After H ↓ L	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
B Destination Address Hold Time After L ↑ H	7, 8, 9, 10, 11
D Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
D Hold Time After L ↑ H	7, 8, 9, 10, 11
C_n Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
C_n Hold Time After L ↑ H	7, 8, 9, 10, 11
I_{012} Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
I_{012} Hold Time After L ↑ H	7, 8, 9, 10, 11
I_{345} Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
I_{345} Hold Time After L ↑ H	7, 8, 9, 10, 11
I_{678} Set-Up Time Before H ↓ L	7, 8, 9, 10, 11
I_{678} Hold Time After H ↓ L	7, 8, 9, 10, 11
I_{678} Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
I_{678} Hold Time After L ↑ H	7, 8, 9, 10, 11
RAM_0, RAM_3, Q_0, Q_3 Set-Up Time Before L ↑ H	7, 8, 9, 10, 11
RAM_0, RAM_3, Q_0, Q_3 Hold Time After L ↑ H	7, 8, 9, 10, 11

Document #: 38-00021-B