To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RD15LD74AP, RD15LD74ANP, RD15LD74AT

8-bit D-type Flip-Flop Driver (with Clear)

REJ03D0894-0300
Rev.3.00
Feb 29, 2008

Description

RD15LD74AP, RD15LD74ANP, RD15LD74AT have eight D-type flip-flop drivers and high voltage NMOS output (open drain output) in a 20 pin package. Each bit, there are a common clear and clock input. The input signal is output with the rising edge of clock signals. The voltage of maximum 15 V can be impressed to the drain-source voltage.

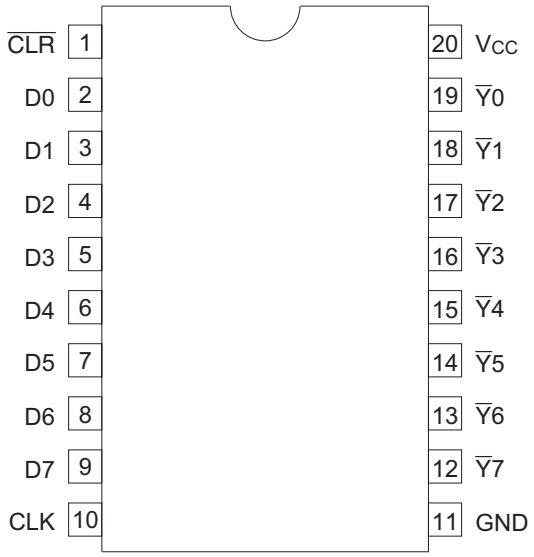
Features

- Application of amusement equipment.
- Output voltage : V_{DS} (max) = 15 V
- Output current : I_{DS} (max) = 200 mA (par pin)
- Supply voltage range : 3.0 to 5.5 V
- Operating temperature range : –20 to +85 °C
- Quiescent supply current : 5 µA max.
- Low input current : 1 µA max.
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Packing Abbreviation (Quantity)	Surface Treatment
RD15LD74APT0	SDIP-20 pin	PRDP0020BA-A (20P4B)	P	T (1,125 pcs/box)	0 (Sn-Cu)
RD15LD74ANPT0	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	T (1,000 pcs/box)	0 (Ni/Pd/Au)
RD15LD74ATH0	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	H (2,000 pcs/reel)	0 (Ni/Pd/Au)

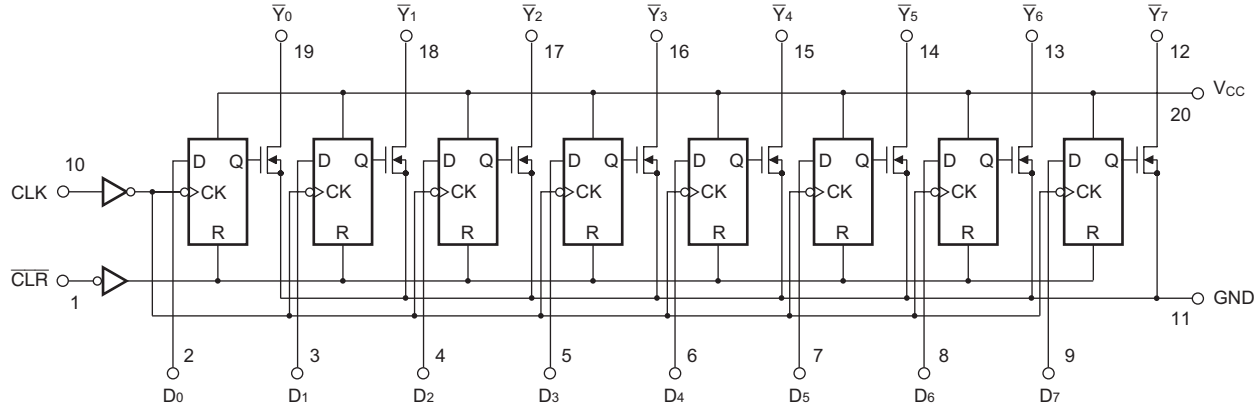
Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Logic Diagram



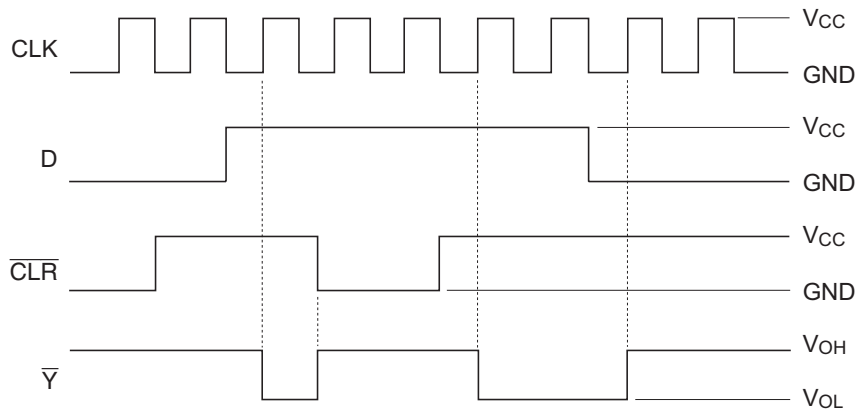
Note: Schmitt trigger circuit is added to all input. V_H = 1.5 V (TYP)

Function Table

Inputs			Output
$\overline{CLR}$	CLK	D	$\overline{Y}$
L	X	X	Z
H	↑	L	Z
H	↑	H	L
H	L	X	Y_0
H	↓	X	Y_0

H : High level
L : Low level
X : Immaterial
Z : High Impedance
↑ : Low to High transition
↓ : High to Low transition
Y_0 : Level of $\overline{Y}$ before the indicated steady input conditions were established.

Timing Figure



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions	
Supply voltage	V_{CC}	6.5	V		
Input voltage	V_I	–0.5 to V_{CC}	V		
Output voltage	V_{DS}	–0.5 to 15	V	Output : “Z” (off)	
Output current	I_{DS}	200	mA	Output : “on” , Current of one circuit	
Maximum power dissipation [*1]	P_T	1.47	W	SDIP	Ta = 25°C Base implementation
		1.38		DILP	
		0.76		TSSOP	
Storage temperature	Tstg	–55 to +125	°C		

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. The maximum package power dissipation was calculated using a junction temperature of 150°C

Recommended Operating Conditions

Item	Symbol	Ratings		Unit	Conditions	
Supply voltage	V_{CC}	3.0	5.5	V		
Input voltage	V_I	0	V_{CC}	V		
Output voltage	V_{DS}	0	15	V	Output “Z” (off)	
Output current (Current of an one circuit, when eight circuit operation)	I_{DS}	0	200	mA	SDIP	Duty cycle ≤ 60%
		0	150			Duty cycle ≤ 100%
		0	200	mA	DILP	Duty cycle ≤ 55%
		0	140			Duty cycle ≤ 100%
		0	200	mA	TSSOP	Duty cycle ≤ 25%
		0	105			Duty cycle ≤ 100%
Input rise / fall time	t_r, t_f	0	500	ns	V_{CC} = 3.0 V, 4.5 V	
Operating temperature	Ta	–20	85	°C		

Note: Unused or floating inputs must be held high or low.

Electrical Characteristics

(Ta = –20 to +85°C)

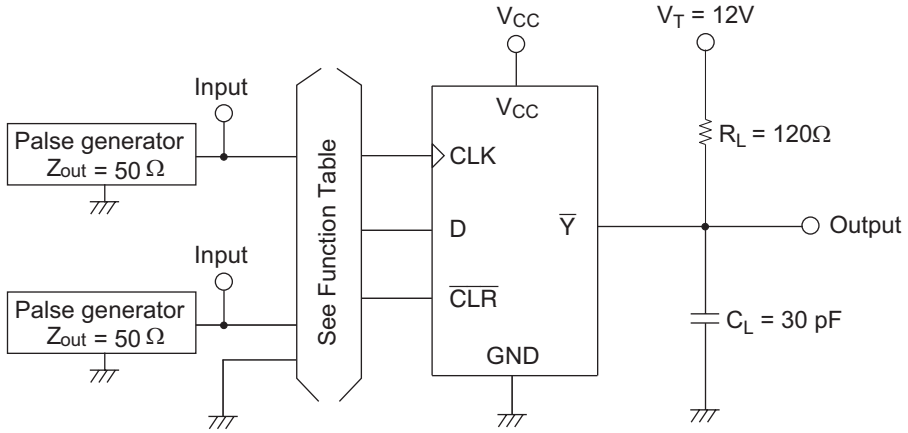
Item	Symbol	VCC (V)	Ratings			Unit	Conditions
			Min	Typ	Max		
Input voltage	V_{IH}	3.0 to 3.6	V_{CC}×0.84	—	—	V	
		4.5 to 5.5	V_{CC}×0.76	—	—		
	V_{IL}	3.0 to 3.6	—	—	V_{CC}×0.16	V	
		4.5 to 5.5	—	—	V_{CC}×0.24		
Output voltage	V_{DS}	3.0 to 3.6	—	0.30	0.45	V	I_{DS} = 100 mA
		4.5 to 5.5	—	0.25	0.38		
		3.0 to 3.6	—	0.60	0.90		I_{DS} = 200 mA
		4.5 to 5.5	—	0.51	0.77		
“H” input current	I_{IH}	3.0 to 5.5	—	0.005	1.0	µA	V_I = V_{CC}
“L” input current	I_{IL}	3.0 to 5.5	—	0.005	–1.0	µA	V_I = 0 V
Quiescent supply current	I_{CC}	5.5	—	0.005	5.0	µA	All output “Z” (off) V_I = V_{CC} or GND
		5.5	—	0.005	5.0		All output “on”, V_I = V_{CC} or GND
Output off state leak current	I_{DS}	5.0	—	0.002	5.0	µA	V_{DS} = 12 V
Output on resister	R_{DS}	4.5	—	2.5	3.8	Ω	I_{DS} = 100 mA

Switching Characteristics

(Ta = –20 to +85°C, CL = 30 pF, tr = tf =6 ns)

Item	Symbol	VCC (V)	Ratings		Unit	Conditions
			Min	Max		
Maximum clock frequency	f_{max}	3.3 ± 0.3	—	15	MHz	
		5.0 ± 0.5	—	20		
Propagation delay time	t_{PLH}	3.3 ± 0.3	1.0	65	ns	CLK, $\overline{CLR}$ to $\overline{Y}$
		5.0 ± 0.5	1.0	50		
Propagation delay time	t_{PHL}	3.3 ± 0.3	1.0	60	ns	CLK to $\overline{Y}$
		5.0 ± 0.5	1.0	45		
Setup time	t_{su}	3.3 ± 0.3	25	—	ns	D to CLK
		5.0 ± 0.5	20	—		
Hold time	t_h	3.3 ± 0.3	3	—	ns	CLK to D
		5.0 ± 0.5	3	—		
Pulse width	t_W	3.3 ± 0.3	50	—	ns	CLK, $\overline{CLR}$
		5.0 ± 0.5	40	—		
Output rise time	t_{TLH}	3.3 ± 0.3	—	30	ns	$\overline{Y}$
		5.0 ± 0.5	—	20		
Output fall time	t_{THL}	3.3 ± 0.3	—	10	ns	$\overline{Y}$
		5.0 ± 0.5	—	5		

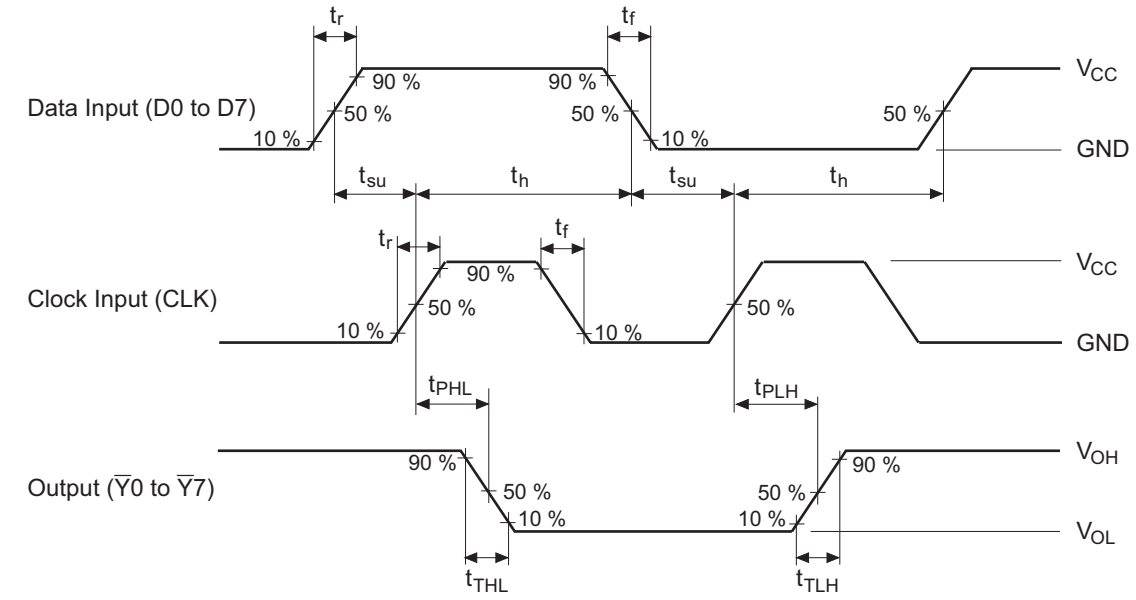
Test Circuit



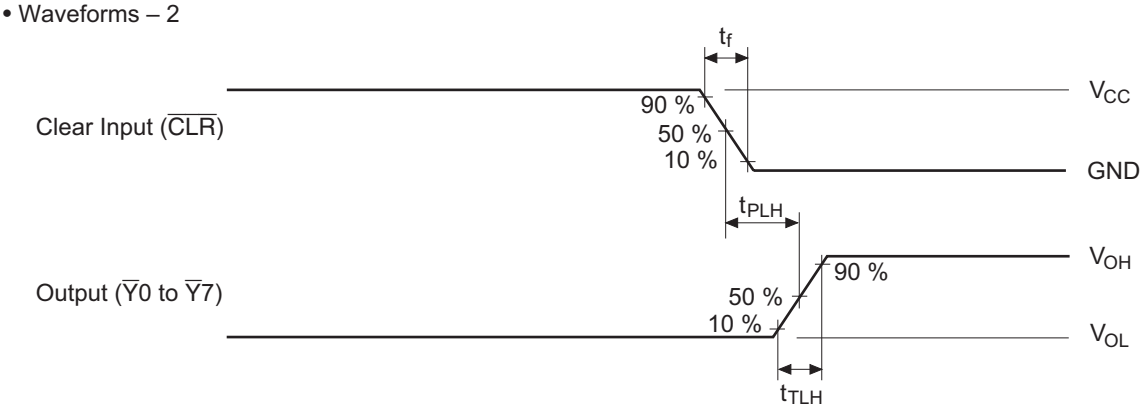
Note: 1. Input waveform : PRR = 1MHz, Duty Cycle = 50%, tr = 6ns, tf = 6ns
2. C_L includes probe and jig capacitance.

Waveforms

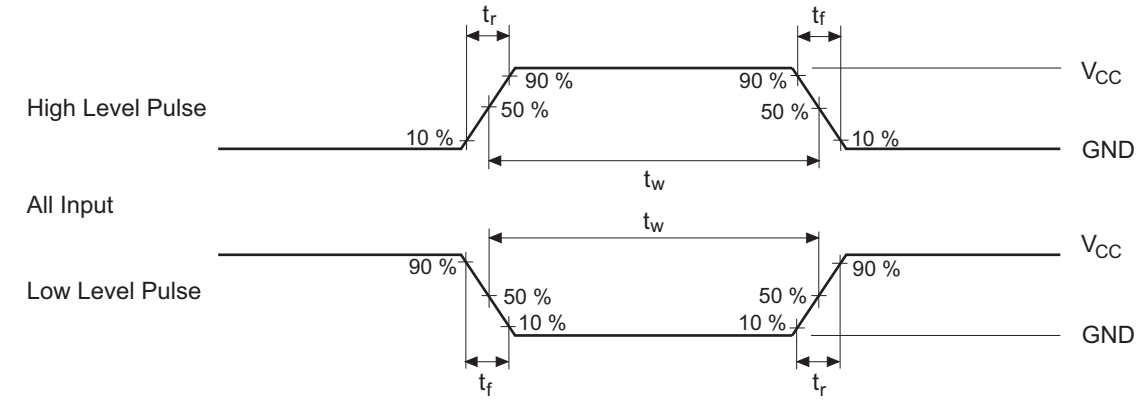
• Waveforms – 1



• Waveforms – 2



• Waveforms – 3

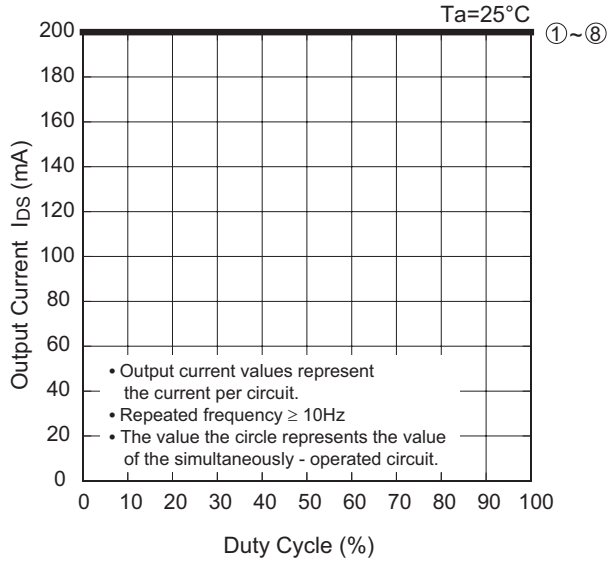


Notes: 1. Input waveform : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
2. The input and output is measured one at a time with one transition per measurement.

Application Data

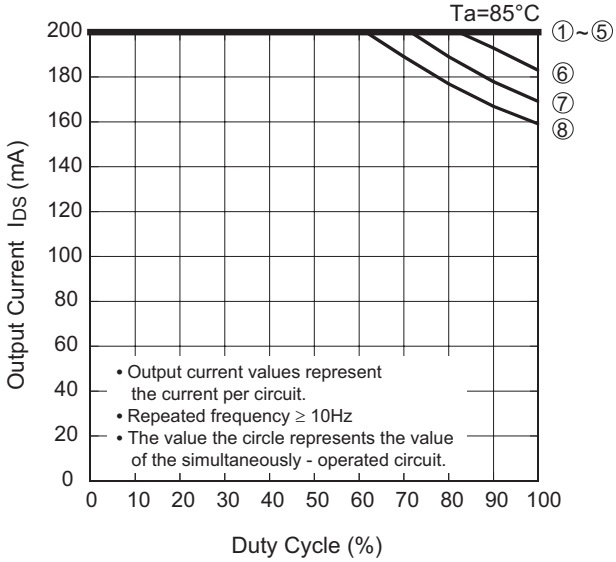
Duty Cycle – Output Current Characteristics

• RD15LD74AP



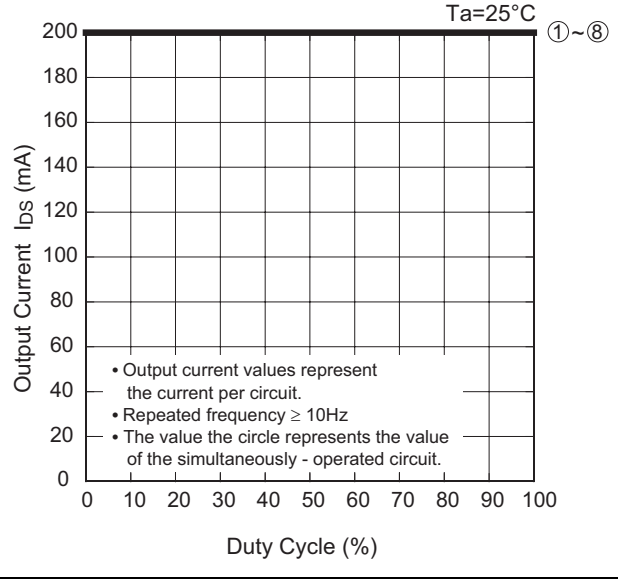
Duty Cycle – Output Current Characteristics

• RD15LD74AP



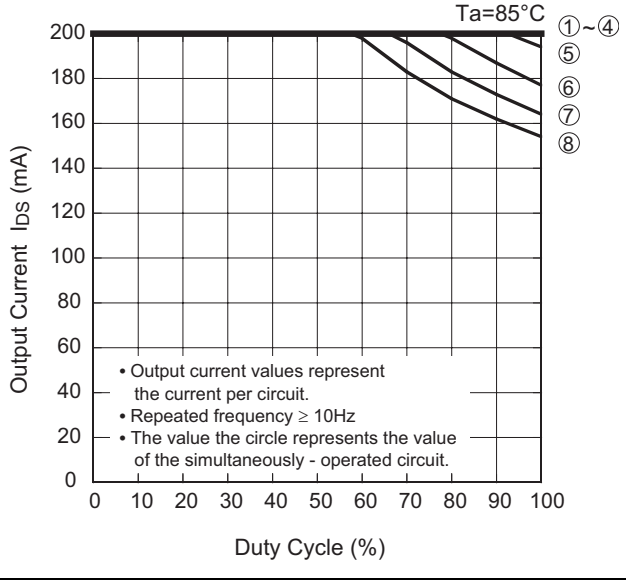
Duty Cycle – Output Current Characteristics

• RD15LD74ANP



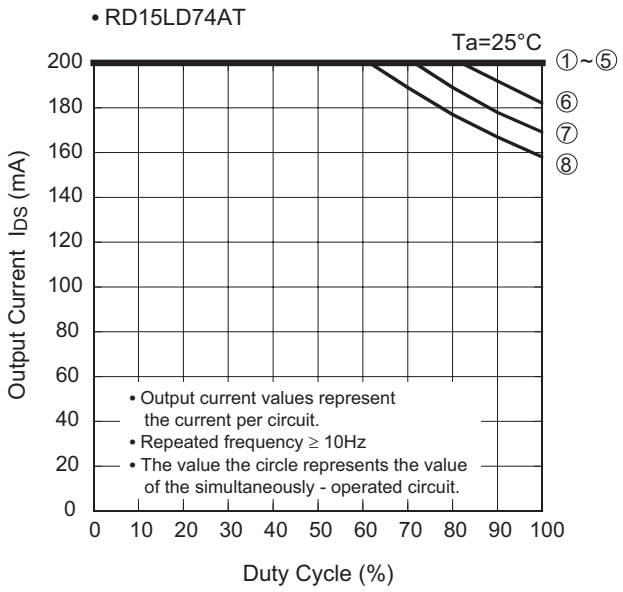
Duty Cycle – Output Current Characteristics

• RD15LD74ANP

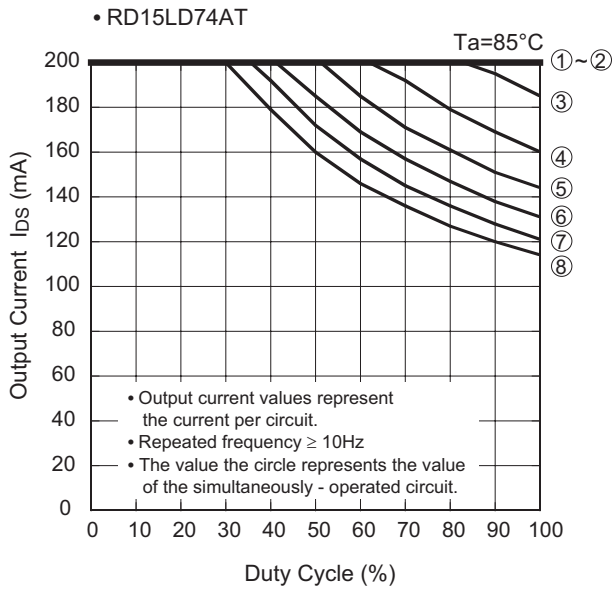


Application Data

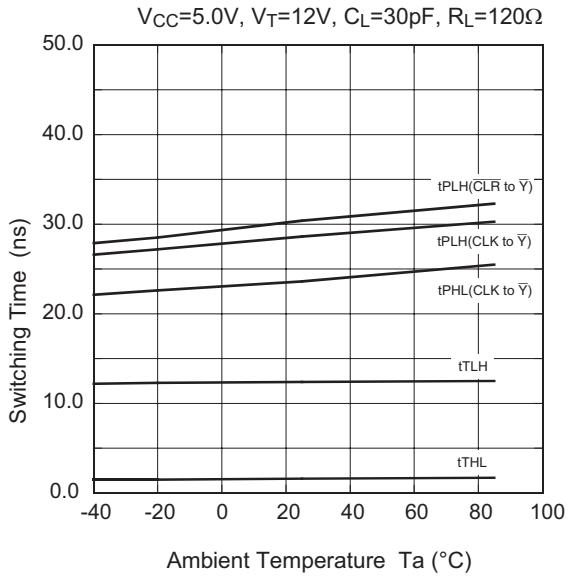
Duty Cycle – Output Current Characteristics



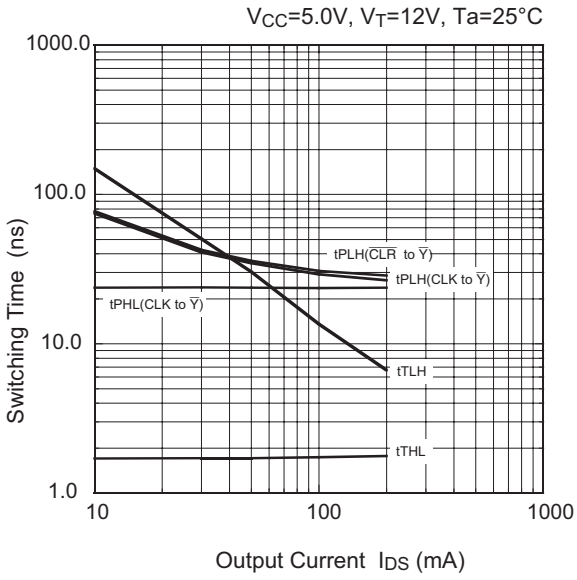
Duty Cycle – Output Current Characteristics



Switching Time – Ambient Temperature Characteristics

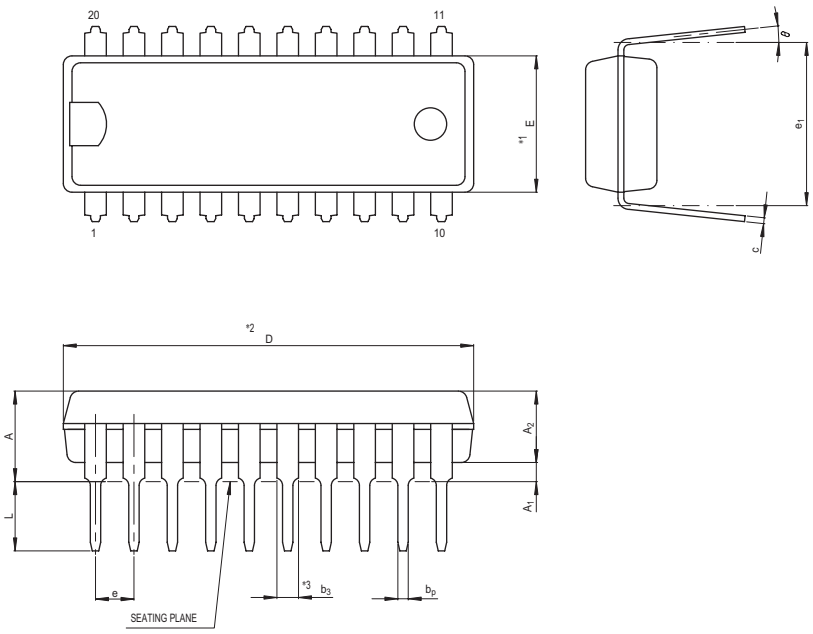


Switching Time – Output Current Characteristics



Package Dimensions

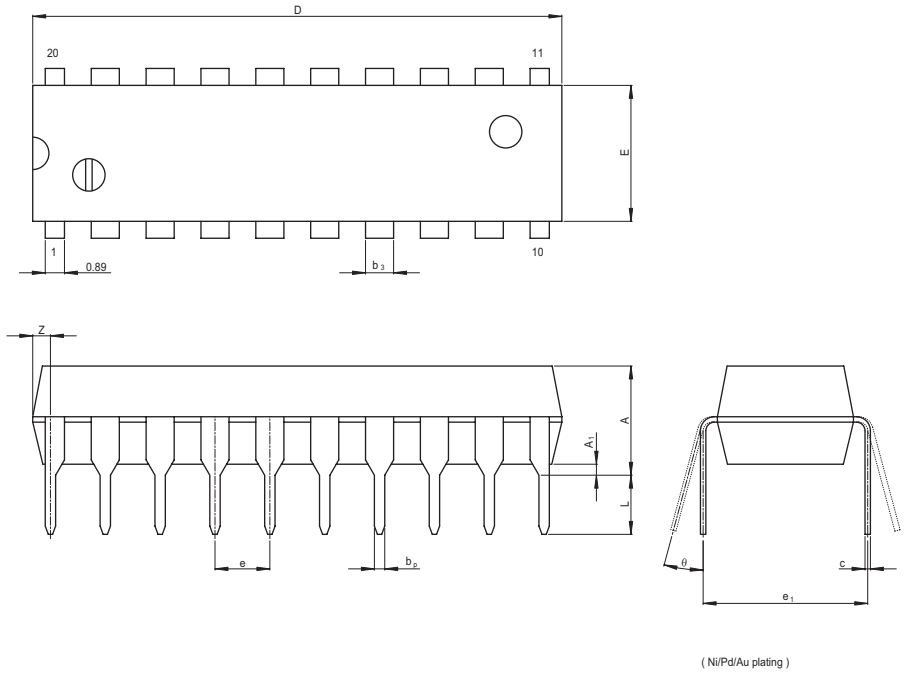
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP20-6.3x19-1.78	PRDP0020BA-A	20P4B	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

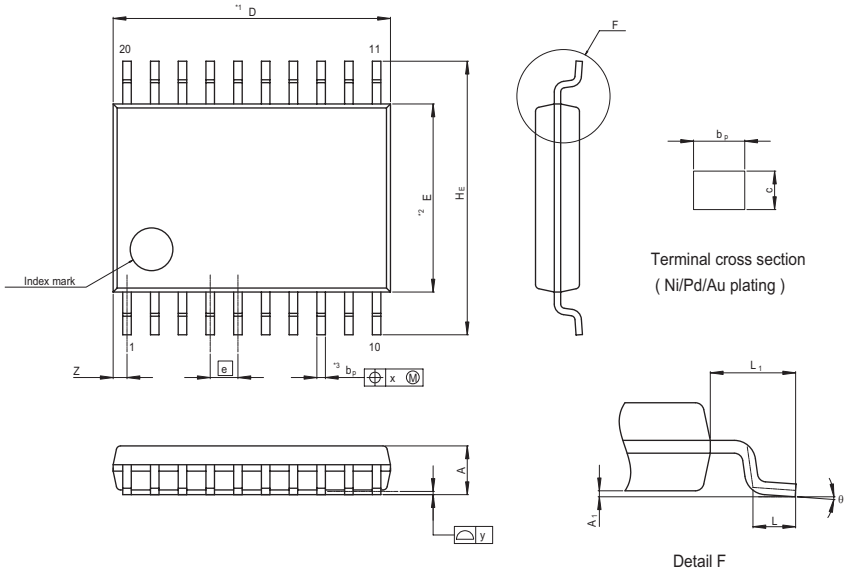
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.38	0.48	0.58
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.3x24.5-2.54	PRDP0020AC-B	DP-20NEV	1.26g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	24.50	25.40
E	—	6.30	7.00
A	—	—	5.08
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.27
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP20-4.4x6.5-0.65	PTSP0020JB-A	TTP-20DAV	0.07g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L_1	—	1.0	—

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