CDP1859/3, CDP1859C/3

High-Reliability 4-Bit Latch and Decoder Memory Interface

Features:

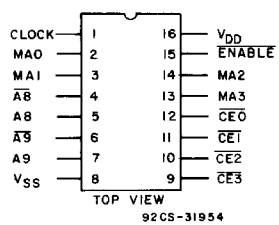
- *Provides easy connection of memory devices to CDP1802 microprocessor*
- *Non-inverting fully buffered data transfer*

The RCA-CDP1859/3 and CDP1859C/3 are CMOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the 1800-series microprocessor multiplexed address bus at maximum clock frequency.

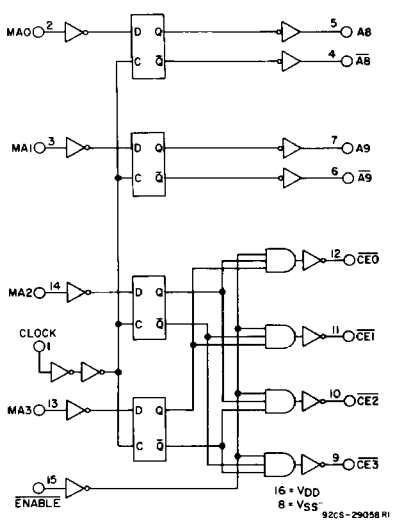
The CDP1859/3 is functionally identical to the CDP1859C/3. The CDP1859/3 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1859C/3 has a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1859/3 interfaces the 1800-series microprocessor address bus and up to 32 CDP1821 1024 x 1 RAMs to provide a 4K byte RAM system. The CDP1859/3 generates the chip selects required by the CDP1821 RAM. The chip select outputs are a function of the address bits connected to inputs MA2 and MA3. The address bits connected to inputs MA0 and MA1 are latched by the trailing edge of TPA (generated by the 1800-series microprocessor) to provide the two additional address lines required by the CDP1821 when used in a CDP1800 series microprocessor-based system. When $\overline{ENABLE}$ = 1, the CE outputs are 1's; when $\overline{ENABLE}$ = 0, the CE outputs are enabled and correspond to the binary decode of the MA2 and MA3 inputs. $\overline{ENABLE}$ does not affect the latching or state of outputs A8, $\overline{A8}$, A9 or $\overline{A9}$.

The CDP1859/3 and CDP1859C/3 are supplied in 16-lead, dual-in-line side-brazed ceramic packages (D suffix) that conform to the requirements and dimensions specified in MIL-38510 Case Outline D-2. Other package styles may be available on a special order basis.

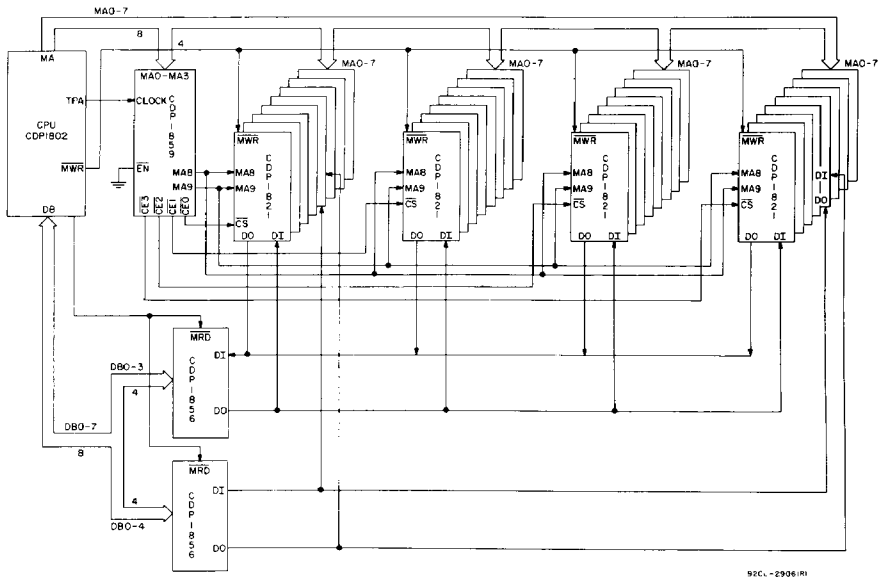


TERMINAL ASSIGNMENT



Functional diagram.

CDP1859/3, CDP1859C/3



4K byte RAM system using the CDP1859, CDP1856, and CDP1821.

STATIC ELECTRICAL CHARACTERISTICS
5-V Data Apply to the CDP1859 and the CDP1859C.
10-V Data Apply to the CDP1859 only.

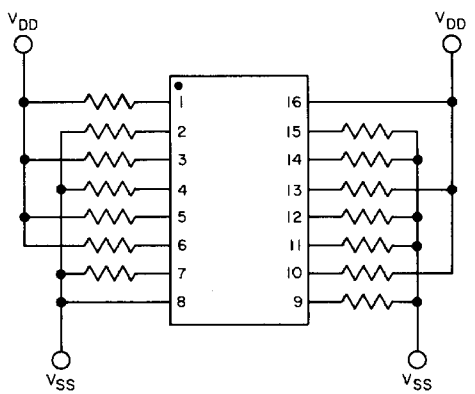
CHARACTERISTIC		TEST CONDITIONS			LIMITS CDP1859 CDP1859C				UNITS
					+25/-55° C		+125° C		
		V_{DD} (V)	V_I (V)	V_O (V)	Min.	Max.	Min.	Max.	
Quiescent Device Current,	I_L	5	0, 5	—	—	500	—	1000	μA
		10	0, 10	—	—	500	—	1000	
Output Low Drive (Sink) Current	I_{OL}	5	0, 5	0.4	1.6	—	1	—	mA
		10	0, 10	0.5	3.6	—	2.2	—	
Output High Drive (Source) Current,	I_{OH}	5	0, 5	4.6	-1.6	—	-1	—	
		10	0, 10	9.5	-3.6	—	-2.2	—	
Input Leakage Current,	I_{IN}	5	0, 5	—	—	±1	—	±5	μA
		10	0, 10	—	—	±1	—	±5	

CDP1859/3, CDP1859C/3

DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		A8	A9	$\overline{\text{A8}}$	$\overline{\text{A9}}$	$\overline{\text{CE0}}$	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{CE3}}$
	MA0	MA1								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY $\overline{\text{ENABLE}}$				1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE



ALL RESISTORS 47 kΩ (± 20%)

92CS-39696

TYPE NO.	V_{DD}	TEMP.	TIME
CDP1859/3	11 V ± 0.5 V	+125°C	160 HRS MIN
CDP1859C/3	7 V ± 0.5 V	+125°C	160 HRS MIN

Static burn-in circuit.