CMOS 4-Bit Arithmetic Logic Unit

High-Voltage Types (20-Volt Rating)

The RCA-CD40181B is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive–OR and–NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181B operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181B contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the CD40181B. Use of the CD40182B look-ahead carry generator in conjunction with multiple CD40181B'S permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance.

Also included in the CD40181B is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in Table III.

The CD40181B types are supplied in 24-lead hermetic ceramic dual-in-line packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40181 is similar to industry types MC14581 and 74181.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

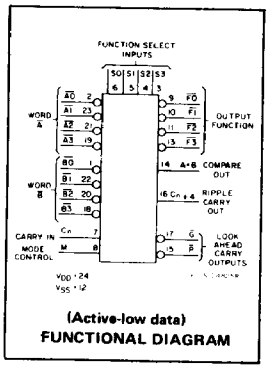
CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

Features:

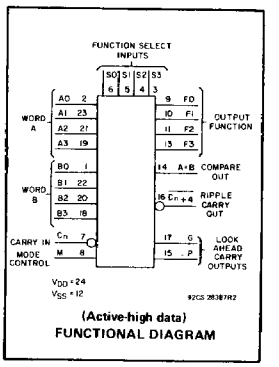
- Full look-ahead carry for speed operations on long words
- Generates 16 logic functions of two Boolean variables
- Generates 16 arithmetic functions of two 4-bit binary words
- A = B comparator output available
- Ripple-carry input and output available
- Typical addition time 200 ns @ V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
  = 1 V at V_{DD} = 5 V
  = 2 V at V_{DD} = 10 V
  = 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Parallel arithmetic units
- Process controllers
- Low-power minicomputers



(Active-low data)
FUNCTIONAL DIAGRAM



(Active-high data)
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

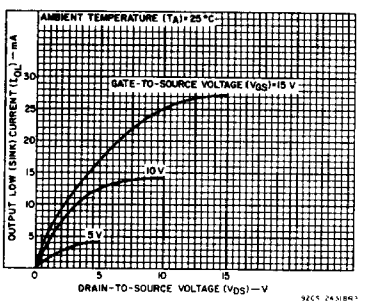


Fig. 1 – Typical output low (sink) current characteristics.

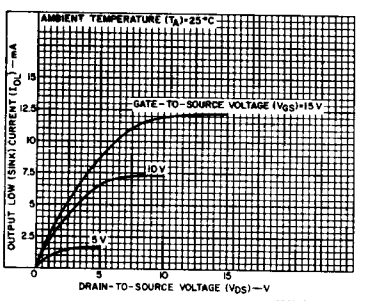


Fig. 2 – Minimum output low (sink) current characteristics.

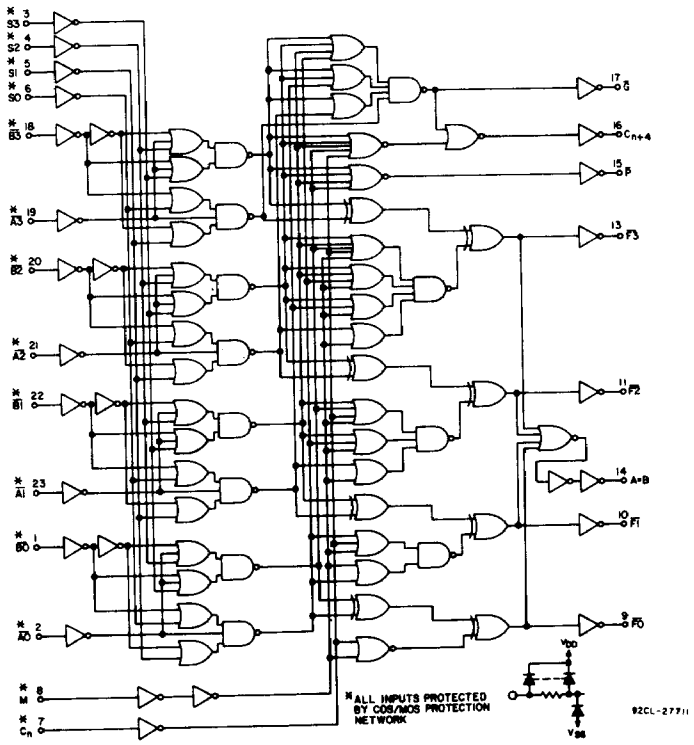


Fig. 3 – CD40181B logic diagram (active-low data).

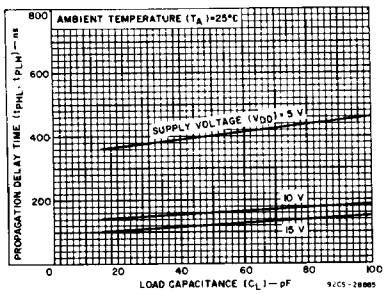


Fig. 6 – Typical propagation delay time as a function of load capacitance (for A or B to F, logic mode).

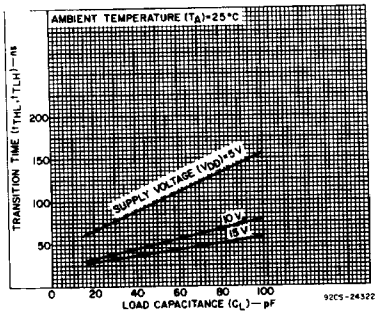


Fig. 7 – Typical transition time as a function of load capacitance.

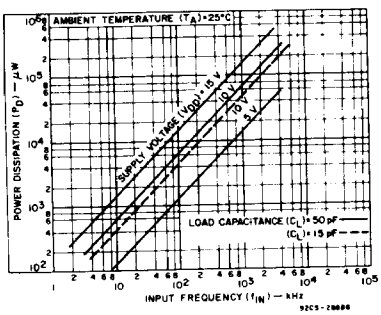


Fig. 8 – Typical dynamic dissipation as a function of input frequency (see Fig. 11 – dynamic power dissipation test circuit).

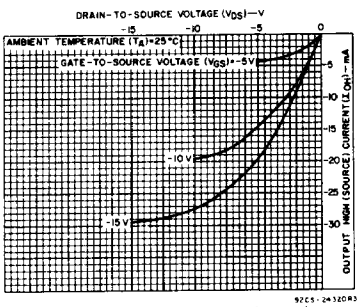


Fig. 4 – Typical output high (source) current characteristics.

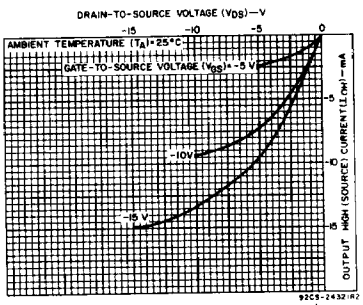


Fig. 5 – Minimum output high (source) current characteristics.

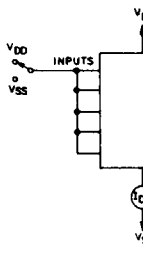


Fig. 9 – Quiescent-device-current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at -40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

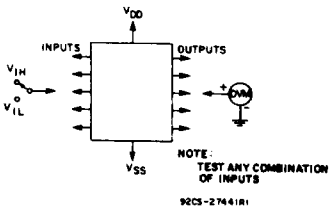


Fig. 10 – Input-voltage test circuit.

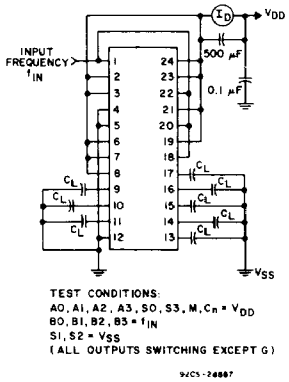


Fig. 11 – Dynamic power dissipation test circuit.

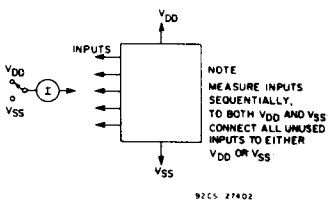
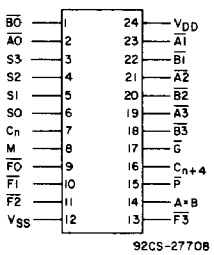


Fig. 12 – Input current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} A or B to F (logic mode), A or B to G or P,	5	400	800	ns
	10	160	320	
	15	120	240	
A or B to F, C_{n+4}, or A = B,	5	500	1000	ns
	10	200	400	
	15	140	280	
C_n to F	5	320	640	ns
	10	135	270	
	15	100	200	
C_n to C_{n+4}	5	200	400	ns
	10	100	200	
	15	70	140	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN} (Any Input)	–	5	7.5	pF



Top View

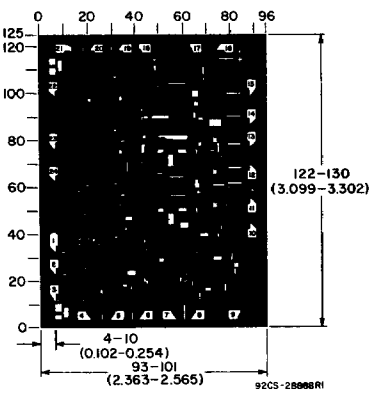
Terminal Assignment (Active-low Data)

TABLE I
TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUT ACTIVE LOW		
				LOGIC FUNCTION	ARITHMETIC* FUNCTION M = L	
S3	S2	S1	S0	M = H	C_n = L	C_n = H
0	0	0	0	$\overline{A}$	A minus 1	A
0	0	0	1	$\overline{AB}$	AB minus 1	AB
0	0	1	0	$\overline{A}$ + B	$\overline{AB}$ minus 1	$A\overline{B}$
0	0	1	1	Logic 1	minus 1	Zero
0	1	0	0	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
0	1	0	1	$\overline{B}$	AB plus (A + $\overline{B}$)	AB plus (A + $\overline{B}$) plus 1
0	1	1	0	$\overline{A \oplus B}$	A minus B minus 1	A minus B
0	1	1	1	A + $\overline{B}$	A + $\overline{B}$	(A + $\overline{B}$) plus 1
1	0	0	0	$\overline{AB}$	A plus (A + B)	A plus (A + B) plus 1
1	0	0	1	A $\oplus$ B	A plus B	A plus B plus 1
1	0	1	0	B	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
1	0	1	1	A + B	A + B	A + B plus 1
1	1	0	0	Logic 0	A plus A	A plus A plus 1
1	1	0	1	$A\overline{B}$	$A\overline{B}$ plus A	$A\overline{B}$ plus A plus 1
1	1	1	0	AB	$A\overline{B}$ plus A	$A\overline{B}$ plus A plus 1
1	1	1	1	A	A	A plus 1

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE HIGH		
				LOGIC FUNCTION	ARITHMETIC* FUNCTION M = L	
S3	S2	S1	S0	M = H	C_n = H	C_n = L
0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{A + B}$	A + B	(A + $\overline{B}$) plus 1
0	0	1	0	$\overline{AB}$	A + $\overline{B}$	(A + $\overline{B}$) plus 1
0	0	1	1	Logic 0	minus 1	Zero
0	1	0	0	$\overline{AB}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
0	1	0	1	$\overline{B}$	(A + B) plus $A\overline{B}$	(A + B) plus $A\overline{B}$ plus 1
0	1	1	0	A $\oplus$ B	A minus B minus 1	A minus B
0	1	1	1	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
1	0	0	0	$\overline{A}$ + B	A plus AB	A plus AB plus 1
1	0	0	1	$\overline{A \oplus B}$	A plus B	A plus B plus 1
1	0	1	0	B	(A + $\overline{B}$) plus AB	(A + $\overline{B}$) plus AB plus 1
1	0	1	1	AB	AB minus 1	AB
1	1	0	0	Logic 1	A plus A	A plus A plus 1
1	1	0	1	A + $\overline{B}$	(A + B) plus A	(A + B) plus A plus 1
1	1	1	0	A + B	(A + $\overline{B}$) plus A	(A + $\overline{B}$) plus A plus 1
1	1	1	1	A	A minus 1	A

* Expressed as two's complement. 1 = HIGH LEVEL 0 = LOW LEVEL



Dimensions and pad layout for CD40181BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

TABLE II

AC TEST SETUP REFERENCE (ACTIVE-LOW DATA)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE*
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}	
SUM_{IN} to SUM_{OUT}	$\overline{BO}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN} to $\overline{P}$	$\overline{AO}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN} to $\overline{G}$	$\overline{BO}$	$\overline{G}$	All $\overline{A}$'s M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN} to C_{n+4}	$\overline{BO}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN} to A = B	$\overline{BO}$	A = B	All A's, B1, B2, B3, M	C_n	SUBTRACT
SUM_{IN} to SUM_{OUT} (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All $\overline{A}$'s, C_n	M	EXCLUSIVE OR

* ADD Mode: SO, S3 = V_{DD}; S1, S2 = V_{SS}. SUBTRACT Mode: SO, S3 = V_{SS}; S1, S2 = V_{DD}.

TABLE III

MAGNITUDE COMPARISON

ACTIVE – HIGH DATA				ACTIVE – LOW DATA		
INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE		INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
1	1	$A \leqslant B$		0	0	$A \leqslant B$
0	1	$A < B$		1	0	$A < B$
1	0	$A > B$		0	1	$A > B$
0	0	$A \geqslant B$		1	1	$A \geqslant B$

1 = HIGH LEVEL
0 = LOW LEVEL