

DATA SHEET

74LVT08

3.3V Quad 2-input AND gate

Product specification

1996 May 29

IC24 Data Handbook

3.3V Quad 2-input AND gate

74LVT08

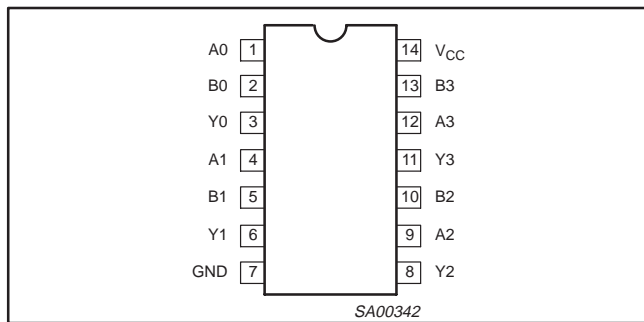
QUICK REFERENCE DATA

SYMBOL	PARAMETER	TEST CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn	$C_L = 50\text{pF};$ $V_{CC} = 3.3\text{V}$	3.0 3.4	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or 3.0V	4	pF
I_{CCL}	Total supply current	Outputs Low; $V_{CC} = 3.6\text{V}$	1	mA

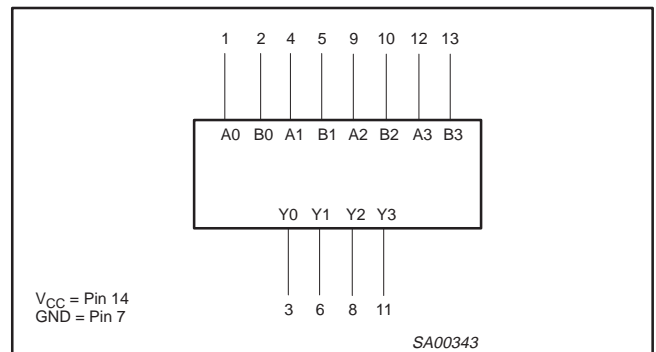
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic SO	-40°C to $+85^{\circ}\text{C}$	74LVT08 D	74LVT08 D	SOT108-1
14-Pin Plastic SSOP	-40°C to $+85^{\circ}\text{C}$	74LVT08 DB	74LVT08 DB	SOT337-1
14-Pin Plastic TSSOP	-40°C to $+85^{\circ}\text{C}$	74LVT08 PW	74LVT08PW DH	SOT402-1

PIN CONFIGURATION



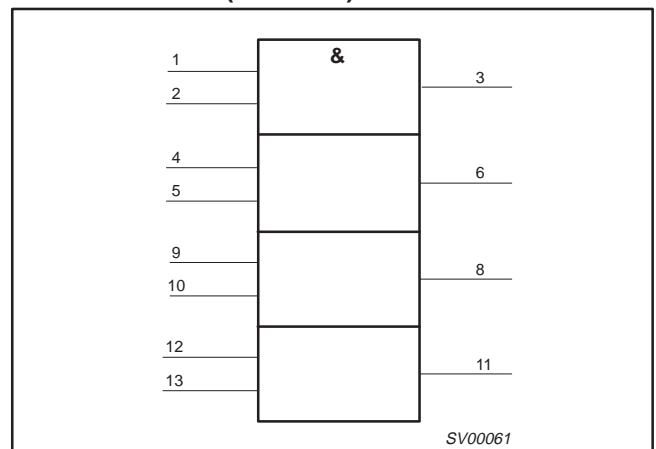
LOGIC DIAGRAM



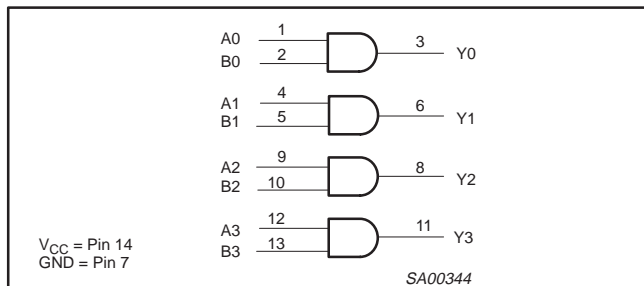
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



3.3V Quad 2-input AND gate

74LVT08

FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:

H = High voltage level

L = Low voltage level

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in High state	-32	mA
		Output in Low state	64	
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	2.7	3.6	V
V _I	Input voltage	0	5.5	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		-20	mA
I _{OL}	Low-level output current		32	mA
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

3.3V Quad 2-input AND gate

74LVT08

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = -18mA			-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2			V
		V _{CC} = 2.7V; I _{OH} = -6mA	2.4			
		V _{CC} = 3.0V; I _{OH} = -20mA	2.0			
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA				V
		V _{CC} = 2.7V; I _{OL} = 24mA	0.5			
		V _{CC} = 3.0V; I _{OL} = 32mA	0.5			
I _I	Input leakage current	V _{CC} = 0 or 3.6V; V _I = 5.5V				μA
		V _{CC} = 3.6V; V _I = V _{CC} or GND	±1			
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V				±100
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0	0.02			mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0	1	2		
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND	0.2			μA
C _I	Input capacitance	V _I = 3V or 0	4			pF
C _O	Output capacitance	V _O = 3V or 0	10			pF

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = -40°C to +85°C.

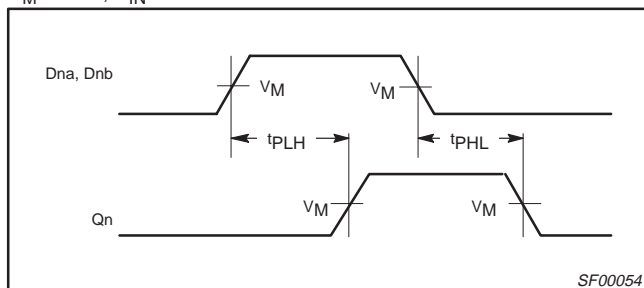
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V	
			MIN	TYP ¹	MAX	MAX	
t _{PLH} t _{PHL}	Propagation delay An or Bn to Yn	1	1.0 1.0	3.0 3.4	3.9 4.6	4.7 4.8	ns

NOTE:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

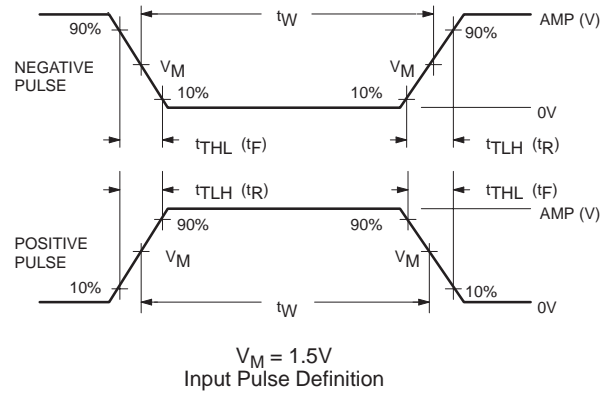
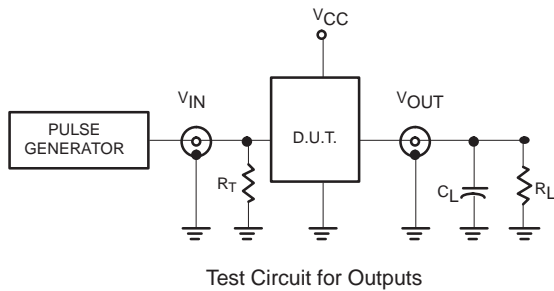


Waveform 1. Propagation Delay for Non-Inverting Outputs

3.3V Quad 2-input AND gate

74LVT08

TEST CIRCUIT AND WAVEFORMS



DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_r	t_f
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

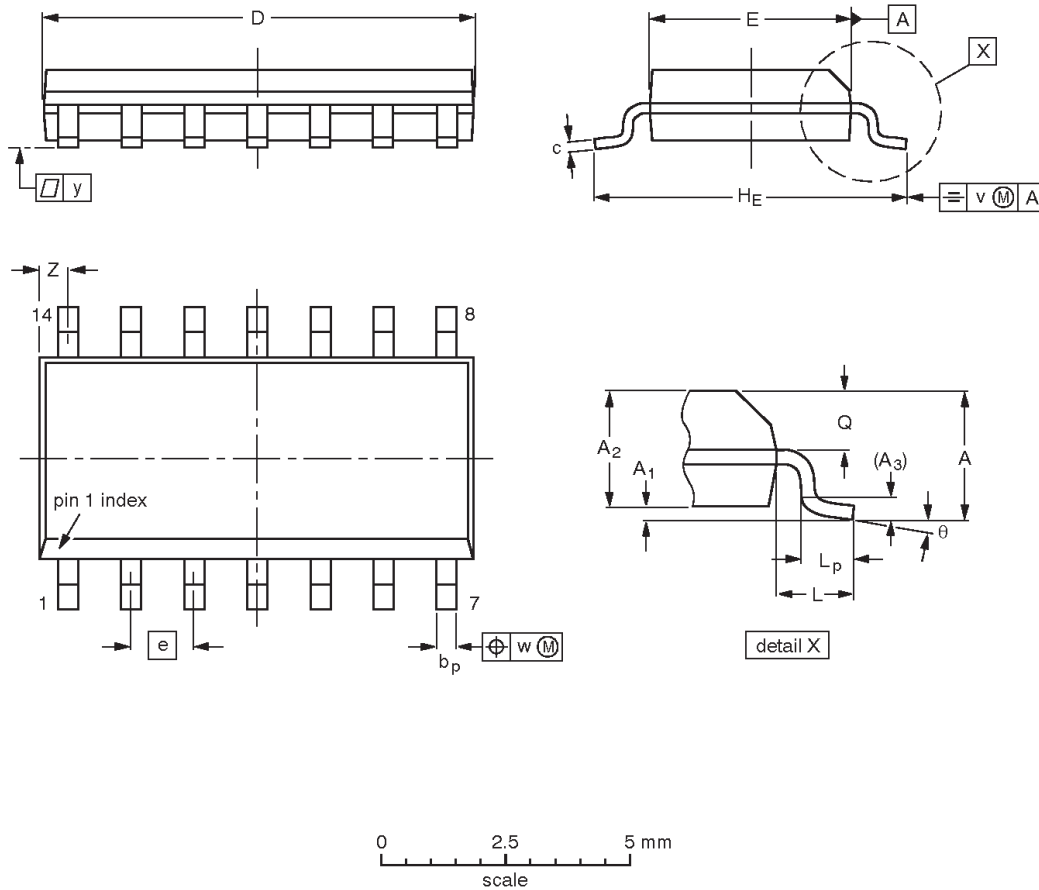
SV00022

3.3V Quad 2-input AND gate

74LVT08

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			95-01-29 97-05-22

3.3V Quad 2-input AND gate

74LVT08

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

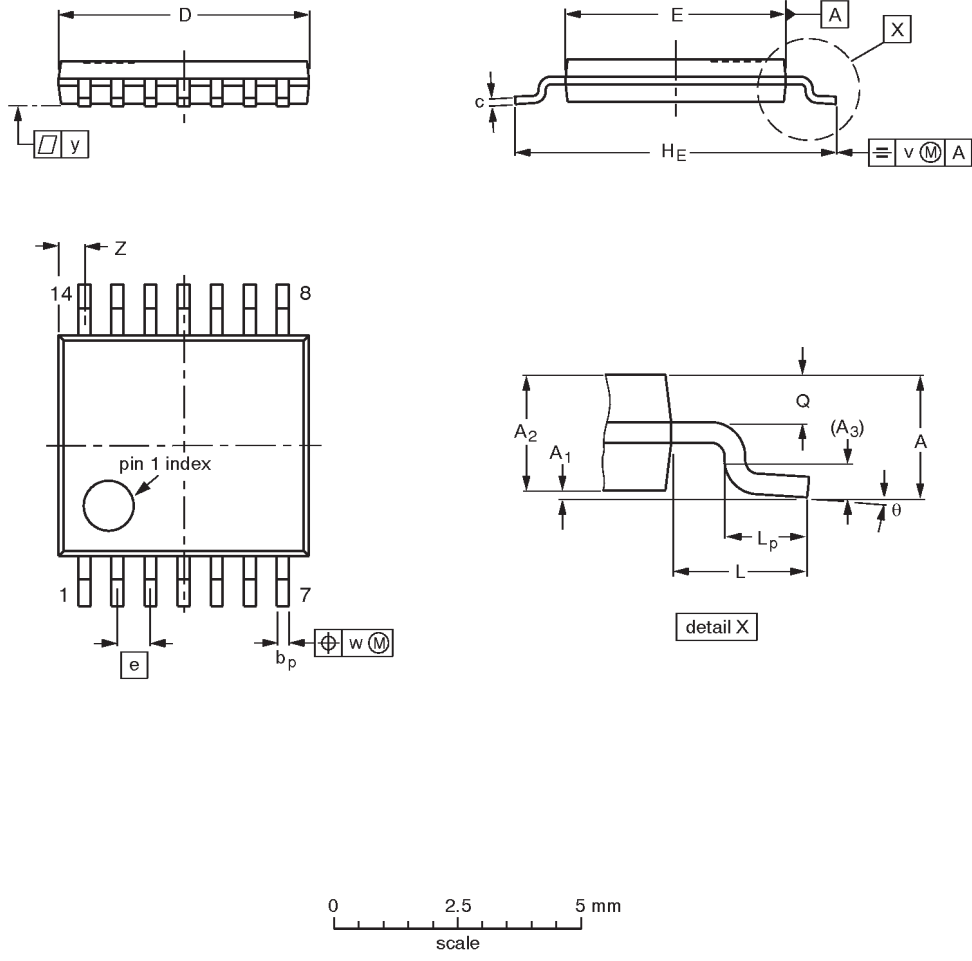
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				95-02-04 96-01-18

3.3V Quad 2-input AND gate

74LVT08

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12- 95-04-04

3.3V Quad 2-input AND gate

74LVT08

NOTES

3.3V Quad 2-input AND gate

74LVT08

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

Philips Semiconductors and Philips Electronics North America Corporation
register eligible circuits under the Semiconductor Chip Protection Act.
© Copyright Philips Electronics North America Corporation 1996
All rights reserved. Printed in U.S.A.

(print code)

Date of release: July 1994

Document order number:

9397-750-04845

74LVT08; 3.3 V Quad 2-input AND gate

Information as of 2003-04-22

My.Semiconductors.COM.
Your personal service from Philips Semiconductors.
Please register now !
Stay informed

Use right mouse button to download datasheet
Download datasheet

[Products](#)

[MultiMarket Semiconductors](#)

[Product Selector](#)

[Catalog by Function](#)

[Catalog by System](#)

[Cross-reference](#)

[Packages](#)

[End of Life information](#)

[Distributors Go Here!](#)

[Models](#)

[SoC solutions](#)

General description	Features	Applications	Datasheet
Block diagram	Buy online	Support & tools	Email/translate
Products & packages	Parametrics	Similar products	

Applications

- [AN2022: The Behavior Of Integrated Bus Hold Circuits](#) (date 01-Mar-96)
- [AN203 2: Test Fixtures for High Speed Logic](#) (date 02-Apr-98)
- [AN2301: Simulation Support for Philips' Advanced BiCMOS Products](#)
- [AN243: LVT \(Low Voltage Technology\) and ALVT \(Advanced LVT\)](#) (date 01-Jan-98)
- [AN246: Transmission Lines and Terminations with Philips Advanced Logic Families](#)

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74LVT08	3.3 V Quad 2-input AND gate	5/29/1996	Product specification	10	87	Download

Blockdiagram(s)

Block diagram of 74LVT08D

▣ Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74LVT08D	SOT108-1 (SO14)	3.3V Quad 2-Input AND Gate	4~6	Low	14	None	TTL	Medium
74LVT08DB	SOT337-1 (SSOP14)	3.3V Quad 2-Input AND Gate	4~6	Low	14	None	TTL	Medium
74LVT08PW	SOT402-1 (TSSOP14)	3.3V Quad 2-Input AND Gate	4~6	Low	14	None	TTL	Medium

▣ Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u> DigiKey IC packing info	<u>Package</u>	<u>Device status</u>	<u>Buy online</u>
74LVT08D	74LVT08D	9352 090 20112	Standard Marking * Tube	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
	74LVT08D-T	9352 090 20118	Standard Marking * Reel Pack, SMD, 13"	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
74LVT08DB	74LVT08DB	9352 090 30112	Standard Marking * Tube	SOT337-1 (SSOP14)	Full production	order this <input type="checkbox"/>
	74LVT08DB-T	9352 090 30118	Standard Marking * Reel Pack, SMD, 13"	SOT337-1 (SSOP14)	Full production	order this <input type="checkbox"/>
74LVT08PW	74LVT08PW	9352 090 40112	Standard Marking * Tube	SOT402-1 (TSSOP14)	Full production	order this <input type="checkbox"/>
	74LVT08PW-T	9352 090 40118	Standard Marking * Reel Pack, SMD, 13"	SOT402-1 (TSSOP14)	Full production	order this <input type="checkbox"/>

Products in the above table are all in production. Some variants are discontinued; [click here](#) for information on these variants.

▣ Similar products

[DigiKey](#) [74LVT08](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

[Innovative Low Voltage Logic Solutions](#)(date 01-Aug-00)

[Introduction to Advanced BiCMOS Logic Products](#)(date 01-Mar-98)

[Family specifications LVT, family characteristics](#)(date 01-Mar-98)

[Advanced BiCMOS features](#)(date 01-Jan-98)

Email/translate this product information

- [Email this product information.](#)
- Translate this product information page from English to:

The English language is the official language used at the semiconductors.philips.com website and webpages. All translations on this website are created through the use of [Google Language Tools](#) and are provided for convenience purposes only. No rights can be derived from any translation on this website.

[About this Web Site](#)

| Copyright © 2003 Koninklijke Philips N.V. All rights reserved. | [Privacy Policy](#) |

| Koninklijke Philips N.V. | Access to and use of this Web Site is subject to the following [Terms of Use](#). |