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T-43-15

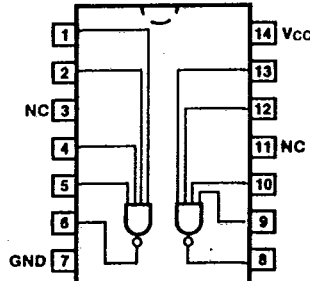
54S/74S140

DUAL 4-INPUT NAND LINE DRIVER

CONNECTION DIAGRAM
PINOUT A

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C to } +70^\circ \text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ \text{C to } +125^\circ \text{C}$	
Plastic DIP (P)	A	74S140PC		9A
Ceramic DIP (D)	A	74S140DC	54S140DM	6A
Flatpak (F)	A	74S140FC	54S140FM	3I



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	2.5/2.5
Outputs	75/37.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S		UNITS	CONDITIONS
		Min	Max		
V_{OH}	Output HIGH Voltage	2.0		V	$V_{CC} = \text{Min}$, $V_{IN} = 0.5 \text{ V}$, $R_0 = 50 \Omega \text{ to Gnd}$
V_{OL}	Output LOW Voltage		0.5	V	$V_{CC} = \text{Min}$, $I_{OL} = 60 \text{ mA}$, $V_{IN} = 2.0 \text{ V}$
I_{OS}	Output Short Circuit Current	-50	-225	mA	$V_{CC} = \text{Max}$, $V_{OUT} = 0 \text{ V}$
I_{CCH} I_{CCL}	Power Supply Current		18 44	mA	$V_{IN} = \text{Gnd}$ $V_{IN} = \text{Open}$ $V_{CC} = \text{Max}$
t_{PLH} t_{PHL}	Propagation Delay		6.5 6.5	ns	Figs. 3-1, 3-4

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ \text{C}$ and $V_{CC} = +5.0 \text{ V}$.