CGS2534V Commercial/CGS2534TV Industrial Quad 1 to 4 Clock Drivers

General Description

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds,

CGS2534 is a 4 to 16 inverting driver with TTL compatible I/Os. This device has skew specifications of 350 ps pin-to-pin as well as a 650 ps specification for part-to-part propagation delay variation.

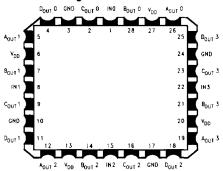
Features

- Guaranteed and tested: 350 ps pin-to-pin skew (t_{OSHL} and t_{OSLH})
- 650 ps part-to-part variation on positive or negative transition
- Implemented on National's ABT family process
- Symmetric output current drive: -36/36 mA I_{OH/IOL}
- Industrial temperature of -40°C to +85°C
- 28-pin PLCC for optimum skew performance
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection

Ordering Code: See Section 10

Connection Diagrams

Pin Assignment for 28-Pin PLCC

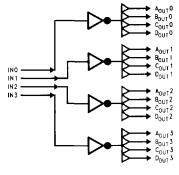


TL/F/11921-5

Truth Table

Input	Output
In(0-3)	ABCD Out (0-3)

CGS2534



TL/F/11921-1

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) 7.0V input Voltage (V_I) 7.0V -30 mA Input Current Current Applied to Output (High/Low) twice the rated IOH/IOL MA

Operating Temperature Industrial Grade

-40°C to +85°C Commercial Grade 0°C to +70°C Storage Temperature Range -65°C to +150°C

Airflow Typical θ_{JA} 0 LFM 62°C/W 43°C/W 225 LFM 500 LFM 34°C/W 900 LFM 27°C/W

Recommended Operating **Conditions**

Supply Voltage (V_{CC}) 4.5V to 5.5V Maximum Input Rise/Fall Time (0.8V to 2.0V)

Free Air Operating Temperature (TA)

-40°C to +85°C Industrial Commercial 0°C to +70°C

5 ns

Note: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics

Over recommended operating conditions unless otherwise specified. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL}	Input Low Level Voltage				0.8	>
VIH	Input High Level Voltage		2.0			V
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{I} = -18 \text{ mA}$			-1.2	٧
V _{OH}	High Level Output Voltage (Note 5)	$I_{OH} = -3 \text{ mA, } V_{CC} = 4.5 \text{V}$	2.4			V
		$I_{OH} = -36 \text{ mA}, V_{CC} = 4.5 \text{V}$	2.0			
V _{OL}	Low Level Output Voltage (Note 5)	V _{CC} = 4.5V, I _{OL} = 36 mA		0.4	0.5	٧
		$V_{CC} \approx 4.5V$, $I_{OL} = 50 \mu A$		0.1	0.1	
lį	Input Current @ Max Input Voltage	V _{CC} = 5.5V, V _{IH} = 7V			7	μΑ
l _{IH}	High Level Input Current	$V_{CC} = 5.5V, V_{IH} = 2.7V$			5	μΑ
I _{IL}	Low Level Input Current	$V_{CC} = 5.5V, V_{IL} = 0.4V$	-5			μА
los	Output Drive Current	$V_{CC} = 5.5V, V_{O} = 0V$	-100		275	mA
lord	Minimum Dynamic Output Current (Note 1)	$V_{CC} = 5.5V, V_{OLD} = 0.8V$	70		·	mA
Гонр	Minimum Dynamic Output Current (Note 1)	$V_{CC} = 5.5V, V_{OHD} = 2.0V$	- 90			mA
ССТ	Maximum I _{CC} /Input	V _{CC} = 5.5V			3.6	mA
lcc	Supply Current '2534 (Quiescent)	V _{CC} = 5.5V			235	μΑ
C _{IN}	Input Capacitance	V _{CC} = 5V		5		pF

Note 1: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Over recommended operating conditions unless otherwise specified. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol		CGS2534						Unit
	Parameter	$T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ $R_L = 500\Omega$			$T_A = -40^{\circ}\text{C to} + 85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$ $R_L = 500\Omega$			
		Min	Тур	Max	Min	Тур	Max]
f _{MAX}	Frequency Maximum					125		MHz
t _{PLH}	Low-to-High Propagation Delay IN _n to OUT _n			3.5			3.5	ns
t _{PHL}	High-to-Low Propagation Delay INn to OUTn			3.5			3.5	ns
^t OSHL	Maximum Skew Common Edge Output-to-Output Variation (Note 2)		150	350		300	350	ps
toslh	Maximum Skew Common Edge Output-to-Output Variation (Note 2)		150	350		300	350	ps
t _{RISE} , t _{FALL}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)			1.5			1.5	ns
t _{HIGH}	Pulse Width Duration High Pulse Width Duration Low (Note 4)	4			4 4			ns
t _{PVLH}	Part-to-Part Variation of Low-to-High Transitions (Note 3)			650			650	ps
t _{PVHL}	Part-to-Part Variation of High-to-Low Transitions (Note 3)			650			650	ps

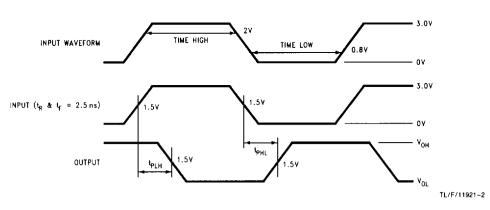
Note 2: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Limits are guaranteed by design.

Note 3: Part to Part transition variation is defined as the absolute difference between the propagation delay of any output on one device to any output on another device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{PVHL}) or LOW to HIGH (t_{PVLH}). Limits are guaranteed by design.

Note 4: Time high is measured at 2.0V, time low is measured at 0.8V.

Note 5: For increased drive, output pins may be connected together when the corresponding input pins are connected together.

Timing Information



CGS2534/35/36/37

Memory Array Driving

In order to minimize the total load on the address bus, quite often memory arrays are being driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large buswidth designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

CGS2534/35/36/37 Quad 1 to 4 Clock Drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

These drivers are optimized to driver large loads, with 3.5 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together (see the diagram below, point A). This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 350 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory sub-system by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problem which are associated with driving high capacitive loads (Point B).

The diagram below depicts a "2534/35/36/37" a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These drivers can operate beyond 125 MHz, and are also available in 3V-5V TTL/CMOS versions with large current drive.

