T-51-10-10

National Semiconductor

ADC1031/ADC1034/ADC1038 10-Bit Serial I/O A/D Converters with Analog Multiplexer and Track/Hold Function

General Description

The ADC1031, ADC1034 and ADC1038 are 10-bit successive approximation A/D converters with serial I/O. The serial input, for the ADC1034 and ADC1038, controls a single-ended analog multiplexer that selects one of 4 input channels (ADC1034) or one of 8 input channels (ADC1038). The ADC1034 and ADC1038 serial output data can be configured into a left- or right-justified format.

An input track/hold is implemented by a capacitive reference ladder and sampled-data comparator. This allows the analog input to vary during the A/D conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Applications

- Engine control
- Process control
- Instrumentation
- Test equipment

Features

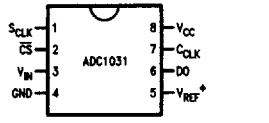
- Serial I/O (MICROWIRE™ compatible)
- Separate asynchronous converter clock and serial data I/O clock
- Analog input track/hold function
- Ratiometric or absolute voltage referencing
- No zero or full scale adjustment required
- 0V to 5V analog input range with single 5V power supply
- TTL/MOS input/output compatible
- No missing codes

Key Specifications

■ Resolution	10 bits
■ Total unadjusted error	±½ LSB and ±1 LSB (max)
■ Single supply	5V ±5%
■ Power dissipation	20 mW (max)
■ Max. conversion time (f_C = 3 MHz)	13.7 μs (max)
■ Serial data exchange time (f_S = 1 MHz)	10 μs (max)

Connection Diagrams

Dual-In-Line and SO Packages



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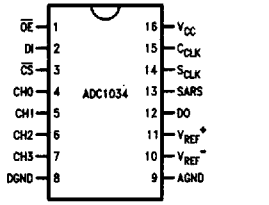
Top View

ADC1031 In NS Package N08E



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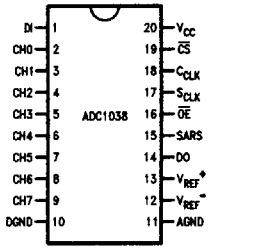
Top View

ADC1034 In NS Packages J16A, M16B or N16E



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Top View

ADC1038 In NS Packages J20A, M20B or N20A

Ordering Information

Industrial $-40°C \le T_A \le +85°C$	Package
ADC1031BIN, ADC1031CIN	N08E
ADC1034BIJ, ADC1034CIJ	J16A
ADC1034BIN, ADC1034CIN	N16E
ADC1034BIWM, ADC1034CIWM	M16B
ADC1038BIJ, ADC1038CIJ	J20A
ADC1038BIN, ADC1038CIN	N20A
ADC1038BIWM, ADC1038CIWM	M20B
Military $-55°C \le T_A \le +125°C$	**Package**
ADC1034CMJ	J16A
ADC1038CMJ	J20A

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Package Dissipation at T_A = 25°C (Note 5)	500 mW
ESD Susceptability (Note 6)	2000V
Soldering Information	
N Package (10 sec.)	260°C
J Package (10 sec.)	300°C
SO Package (Note 7):	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1031BIN, ADC1031CIN, ADC1034BIJ, ADC1034CIJ, ADC1034BIN, ADC1034CIN, ADC1034BIWM, ADC1034CIWM, ADC1038BIJ, ADC1038CIJ, ADC1038BIN, ADC1038CIN, ADC1038BIWM, ADC1038CIWM	$-40°C \le T_A \le +85°C$
ADC1034CMJ, ADC1038CMJ	$-55°C \le T_A \le +125°C$
Supply Voltage (V_{CC})	4.75 V_{DC} to 5.25 V_{DC}
Reference Voltage ($V_{REF} = V_{REF}^+ - V_{REF}^-$)	2.0 V_{DC} to V_{CC} + 0.05V

Electrical Characteristics

The following specifications apply for V_{CC} = +5.0V, V_{REF} = +4.6V, f_S = 700 kHz, and f_C = 3 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter		Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
CONVERTER AND MULTIPLEXER CHARACTERISTICS						
	Total Unadjusted Error	BIJ, BIN, BIWM	(Note 10)		**±1/2**	LSB (max)
		CIJ, CIN, CIWM, CMJ			**±1**	LSB (max)
	Differential Linearity				**10**	Bits (min)
R_{REF}	Reference Input Resistance			8	 **5** **11**	kΩ kΩ (min) kΩ (max)
V_{REF}	Reference Voltage				**(V_{CC} + 0.05)**	V (max)
V_{IN}	Analog Input Voltage		(Note 11)		**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
	On Channel Leakage Current		On Channel = 5 V_{DC}, Off Channel = 0 V_{DC}	5.0	200 **500**	nA (max) nA (max)
	(Note 12)		On Channel = 0 V_{DC}, Off Channel = 5 V_{DC}	5.0	−200 **−500**	nA (max) nA (max)
	Off Channel Leakage Current		On Channel = 5 V_{DC}, Off Channel = 0 V_{DC}	5.0	−200 **−500**	nA (max) nA (max)
	(Note 12)		On Channel = 0 V_{DC}, Off Channel = 5 V_{DC}	5.0	200 **500**	nA (max) nA (max)
	Power Supply Sensitivity	Zero Error	4.75 $V_{DC} \le V_{CC} \le$ 5.25 V_{DC}		**±1/4**	LSB (max)
		Full Scale Error			**±1/4**	LSB (max)

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5.0V, V_{REF} = +4.6V, f_S = 700 kHz, and f_C = 3 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.25 V_{DC}		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75 V_{DC}		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.0 V_{DC}	0.005	**2.5**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0 V_{DC}	−0.005	**−2.5**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75 V_{DC} I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.5**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75 V_{DC} I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V	−0.01	**−3**	μA (max)
		V_{OUT} = 5V	0.01	**3**	μA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V	−14	**−6.5**	mA (min)
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}	16	**8.0**	mA (min)
I_{CC}	Supply Current	$\overline{CS}$ = HIGH, V_{REF} Open	1.5	**3**	mA (max)
AC CHARACTERISTICS					
f_C	Conversion Clock (C_{CLK}) Frequency		0.7 4.0	 **3.0**	MHz (min) MHz (max)
f_S	Serial Data Clock (S_{CLK}) Frequency (Note 13)	f_C = 3 MHz, R/$\overline{L}$ = "0"	183		kHz (min)
		f_C = 3 MHz, R/$\overline{L}$ = "1"	622		kHz (min)
		f_C = 3 MHz, R/$\overline{L}$ = "0" or R/$\overline{L}$ = "1"	2	**1.0**	MHz (max)
T_C	Conversion Time	Not Including MUX Addressing and Analog Input Sampling Times		**41 (1/f_C) + 200 ns**	(max)
t_{CA}	Analog Sampling Time	After Address is Latched, $\overline{CS}$ = Low		**4.5 (1/f_S) + 200 ns**	(max)
t_{ACC}	Access Time Delay from $\overline{CS}$ or $\overline{OE}$ Falling Edge to DO Data Valid	$\overline{OE}$ = "0"	100	**200**	ns (max)
t_{SET-UP}	Set-up Time of $\overline{CS}$ Falling Edge to S_{CLK} Rising Edge		75	**150**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{OE}$ or $\overline{CS}$ Rising Edge to DO TRI-STATE	R_L = 3 kΩ, C_L = 100 pF	100	**120**	ns (max)
t_{HDI}	DI Hold Time from S_{CLK} Rising Edge		0	**50**	ns (min)
t_{SDI}	DI Set-up Time to S_{CLK} Rising Edge		50	**100**	ns (min)

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5.0V, V_{REF} = +4.6V, f_S = 700 kHz, and f_C = 3 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter		Conditions		Typical (Note 8)	Limit (Note 9)	Units (Limits)
AC CHARACTERISTICS (Continued)							
t_{HDO}	DO Hold Time from S_{CLK} Falling Edge		R_L = 30 kΩ, C_L = 100 pF		70	**10**	ns (min)
t_{DDO}	Delay from S_{CLK} Falling Edge to DO Data Valid		R_L = 30 kΩ, C_L = 100 pF		150	**250**	ns (max)
t_{RDO}	DO Rise Time		R_L = 30 kΩ, C_L = 100 pF	TRI-STATE to High	35	**75**	ns (max)
				Low to High	75	**150**	ns (max)
t_{FDO}	DO Fall Time		R_L = 30 kΩ, C_L = 100 pF	TRI-STATE to Low	35	**75**	ns (max)
				High to Low	75	**150**	ns (max)
C_{IN}	Input Capacitance		Analog Inputs (CH0–CH7)		50		pF
			All Other Inputs		7.5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < DGND, or V_{IN} > V_{CC}) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 125°C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: ADC1031 with BIN and CIN suffixes 71°C/W, ADC1034 with BIJ, CIJ, and CMJ suffixes 52°C/W, ADC1034 with BIN and CIN suffixes 54°C/W, ADC1034 with BIWM and CIWM suffixes 70°C/W, ADC1038 with BIJ, CIJ, and CMJ suffixes 53°C/W, ADC1038 with BIN and CIN suffixes 46°C/W, ADC1038 with BIWM and CIWM suffixes 64°C/W.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or *Linear Databook* section "Surface Mount" for other methods of soldering surface mount devices.

Note 8: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 11: Two on-chip diodes are tied to each analog input. They will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

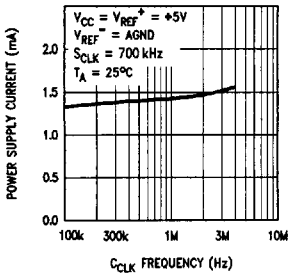
Note 12: Channel leakage current is measured after the channel selection.

Note 13: In order to synchronize the serial data exchange properly, SARS needs to go low after completion of the serial I/O data exchange. If this does not occur the output shift register will be reset and the correct output data lost. The minimum limit for S_{CLK} will depend on C_{CLK} frequency and whether right-justified or left-justified, and can be determined by the following equations:

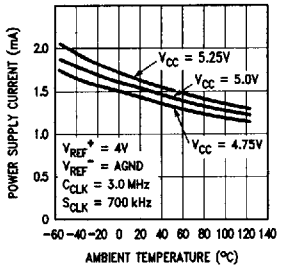
$f_S > (8.5/41)\ (f_C)$ with right-justification (R/$\overline{L}$ = "1") and $f_S > (2.5/41)\ (f_C)$ with left-justification (R/$\overline{L}$ = "0").

Typical Performance Characteristics

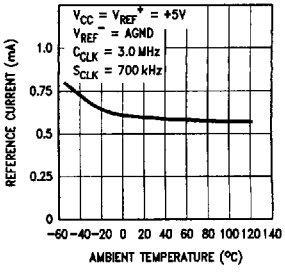
Power Supply Current (I_{CC}) vs C_{CLK}



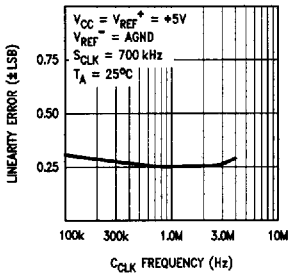
Power Supply Current (I_{CC}) vs Ambient Temperature



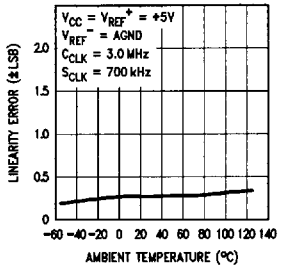
Reference Current (I_{REF}) vs Ambient Temperature



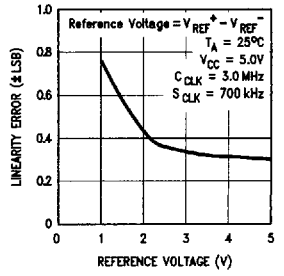
Linearity Error vs C_{CLK} Frequency



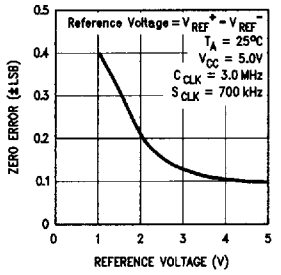
Linearity Error vs Ambient Temperature



Linearity Error vs Reference Voltage



Zero Error vs Reference Voltage



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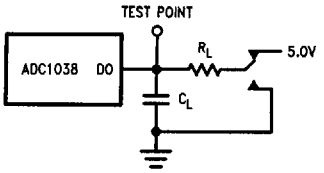
Test Circuits

t_{1H}, t_{0H}



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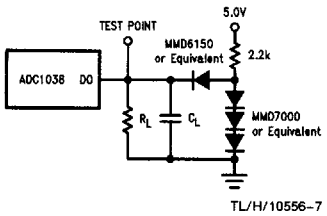
DO except "TRI-STATE"



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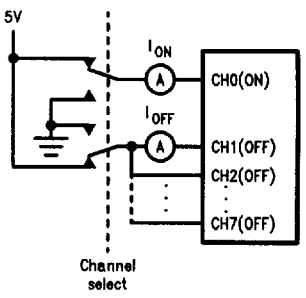
Leakage Current



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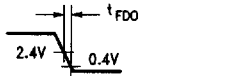
Timing Diagrams

DO High to Low State



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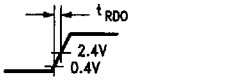
DO Low to High State



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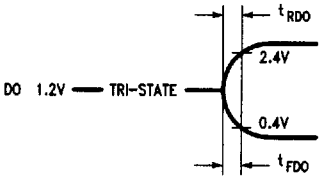
DO "TRI-STATE" Rise and Fall Times



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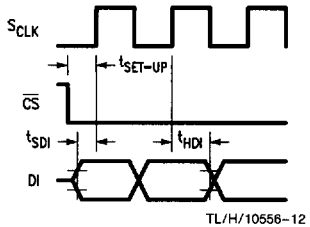
DI Data Input Timing



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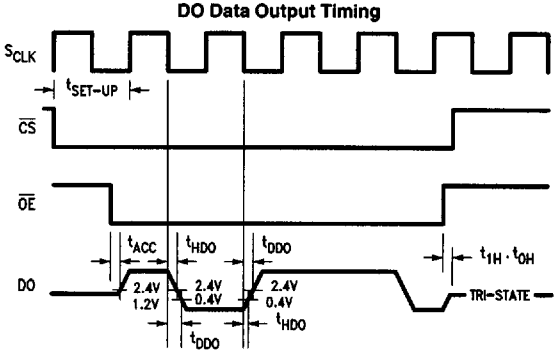
DO Data Output Timing



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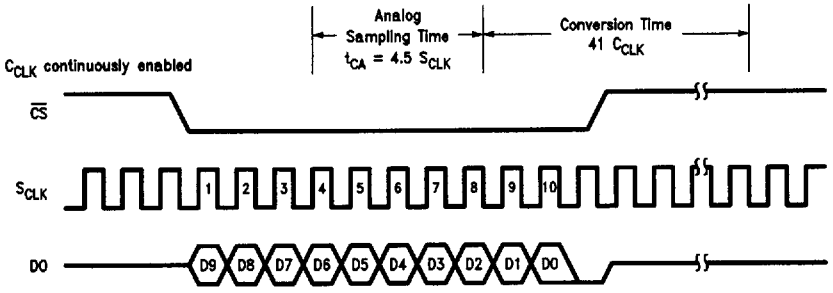
Timing Diagrams (Continued)

ADC1031 $\overline{CS}$ High during Conversion



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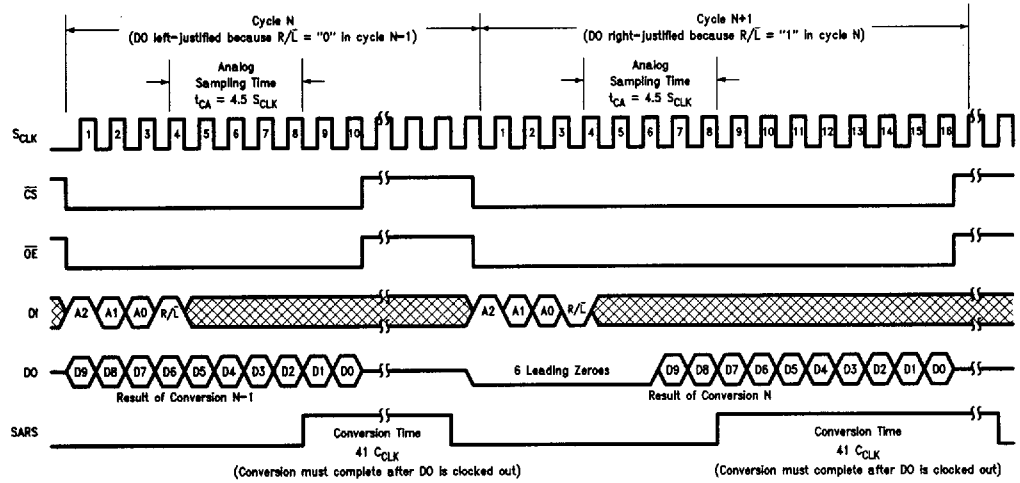
ADC1038/ADC1034 $\overline{CS}$ High during Conversion



C_{CLK} continuously enabled

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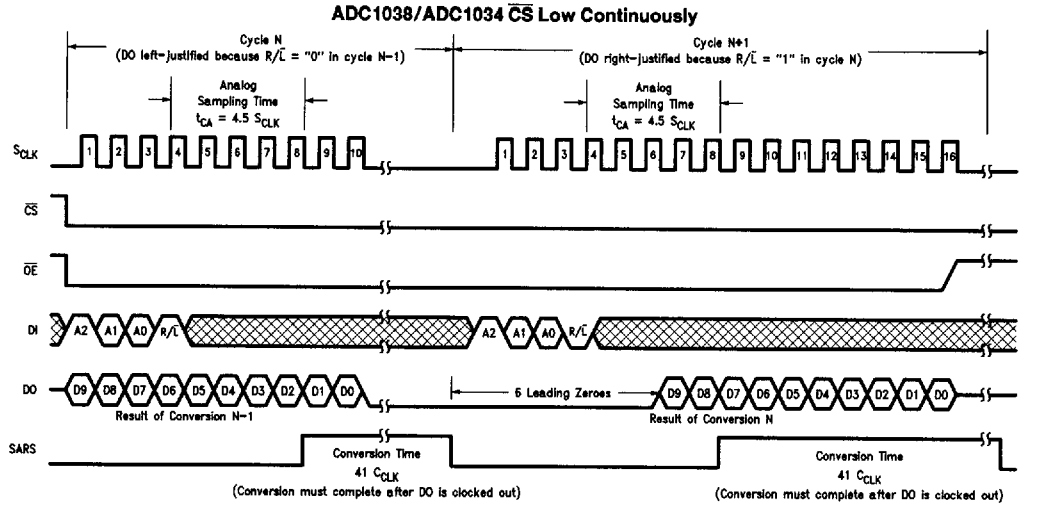
Timing Diagrams (Continued)



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C_{CLK} continuously enabled

Multiplexer Address/Channel Assignment Tables

ADC1038

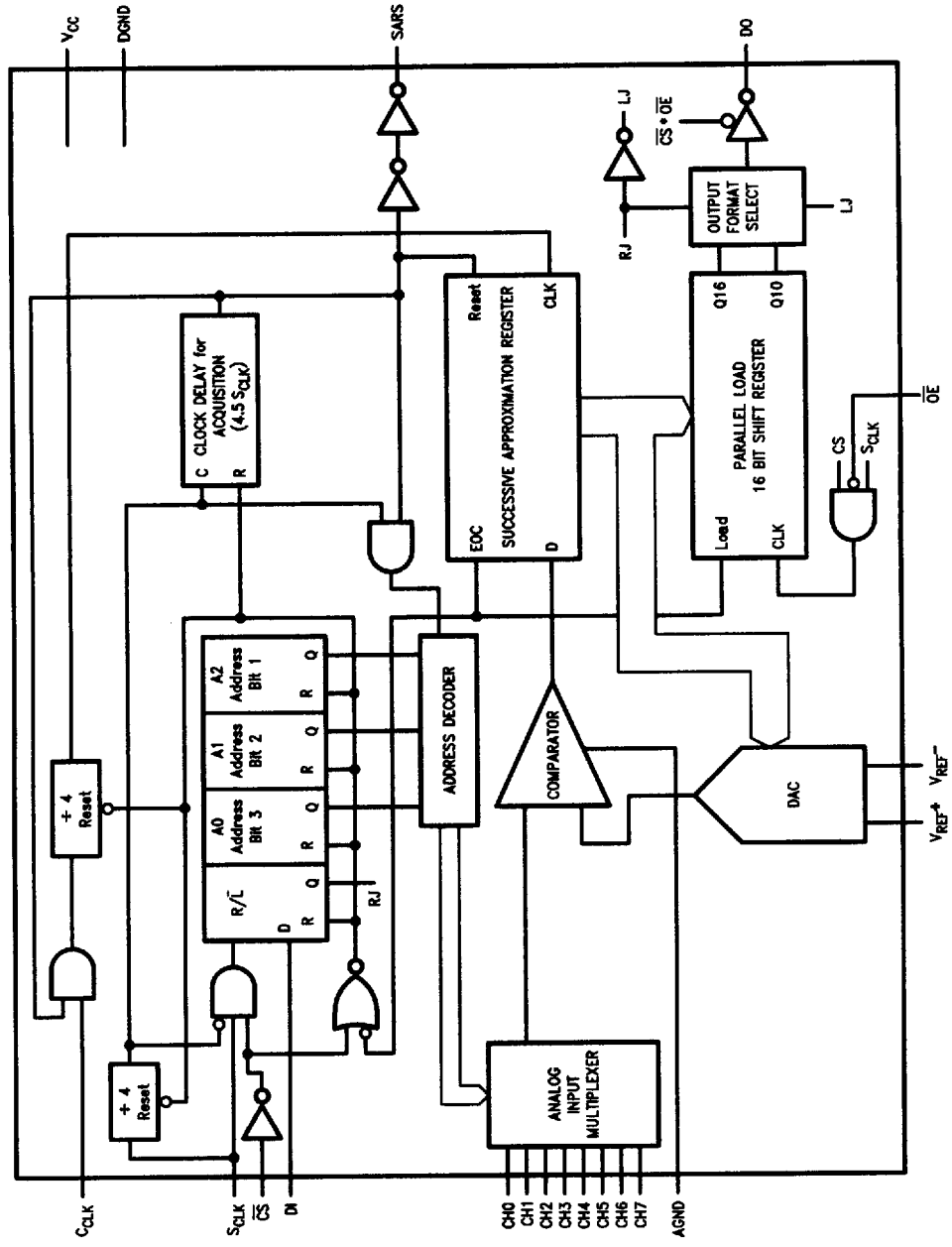
MUX Address			Analog Channel Selected
A2	A1	A0	
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

ADC1034

MUX Address			Analog Channel Selected
A2	A1	A0	
X	0	0	CH0
X	0	1	CH1
X	1	0	CH2
X	1	1	CH3

Note: "X" = don't care

ADC1038 Functional Block Diagram



1.0 Pin Descriptions

C_{CLK} The clock applied to this input controls the successive approximation conversion time interval. The clock frequency applied to this input can be between 700 kHz and 4 MHz.

S_{CLK} The serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs and the analog sampling time available to acquire an analog input voltage. The rising edge loads the information on the DI pin into the multiplexer address shift register (address register). This address controls which channel of the analog input multiplexer (MUX) is selected.

The falling edge shifts the data resulting from the previous A/D conversion out on DO. $\overline{CS}$ and $\overline{OE}$ enable or disable the above functions.

DI The serial data input pin. The data applied to this pin is shifted by S_{CLK} into the multiplexer address register. The first 3 bits of data (A0–A2) are the MUX channel address (see the Multiplexer Address/Channel Assignment tables). The fourth bit (R/$\overline{L}$) determines the data format of the conversion result in the conversion to be started. When R/$\overline{L}$ is low the output data format is left-justified; when high it is right-justified. When right-justified, six leading "0"s are output on DO before the MSB information; thus the complete conversion result is shifted out in 16 clock periods.

DO The data output pin. The A/D conversion result (D0–D9) is output on this pin. This result can be left- or right-justified depending on the value of R/$\overline{L}$ bit shifted in on DI.

SARS This pin is an output and indicates the status of the internal successive approximation register (SAR). When high, it signals that the A/D conversion is in progress. This pin is set high after the analog input sampling time (t_{CA}) and remains high for 41 C_{CLK} periods. When SARS goes low, the output shift register has been loaded with the conversion result and another A/D conversion sequence can be started.

$\overline{CS}$ The chip select pin. When a low is applied to this pin, the rising edge of S_{CLK} shifts the data on DI into the address register.

$\overline{OE}$ The output enable pin. When $\overline{OE}$ and $\overline{CS}$ are both low the falling edge of S_{CLK} shifts out the previous A/D conversion data on the DO pin.

CH0–CH7 The analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of S_{CLK} into the address register.

Source impedances (R_S) driving these inputs should be kept below 1 kΩ. If R_S is greater than 1 kΩ, the sampled data comparator will not have enough time to acquire the correct value of the applied input voltage.

The voltage applied to these inputs should not exceed V_{CC} or go below DGND or AGND by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

V_{REF}^+ The positive analog voltage reference for the analog inputs. In order to maintain accuracy the voltage range of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) is 2.5 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF}^+ cannot exceed V_{CC} + 50 mV.

V_{REF}^- The negative voltage reference for the analog inputs. In order to maintain accuracy the voltage at this pin must not go below DGND and AGND by more than 50 mV or exceed 40% of V_{CC} (for V_{CC} = 5V, V_{REF}^- (max) = 2V).

V_{CC} The power supply pin. The operating voltage range of V_{CC} is 4.75 V_{DC} to 5.25 V_{DC}. V_{CC} should be bypassed with 10 μF and 0.1 μF capacitors to digital ground for proper operation of the A/D converter.

DGND, AGND The digital and analog ground pins. In order to maintain accuracy the voltage difference between these two pins must not exceed 300 mV.

2.0 Functional Description

2.1 DIGITAL INTERFACE

The ADC1034 and ADC1038 implement their serial interface via seven digital control lines. There are two clock inputs for the ADC1034/ADC1038. The S_{CLK} controls the rate at which the serial data exchange occurs and the duration of the analog sampling time window. The C_{CLK} controls the conversion time and must be continuously enabled. A low on $\overline{CS}$ enables the rising edge of S_{CLK} to shift in the serial multiplexer addressing data on the DI pin. The first three bits of this data select the analog input channel for the ADC1038 and the ADC1034 (see the Channel Addressing Tables). The following bit, R/$\overline{L}$, selects the output data format (right-justified or left-justified) for the conversion to be started. With $\overline{CS}$ and $\overline{OE}$ low the DO pin is active (out of TRI-STATE) and the falling edge of S_{CLK} shifts out the data from the previous analog conversion. When the first conversion is started the data shifted out on DO is erroneous as it depends on the state of the Parallel Load 16-Bit Shift Register on power up, which is unpredictable.

The ADC1031 implements its serial interface with only four control pins since it has only one analog input and comes in an eight pin mini-dip package. The S_{CLK}, C_{CLK}, $\overline{CS}$ and $\overline{DO}$ pins are available for the serial interface. The output data format cannot be selected and defaults to a left-justified format. The state of DO is controlled by $\overline{CS}$ only.

2.2 OUTPUT DATA FORMAT

When R/$\overline{L}$ is low the output data format is left-justified; when high it is right-justified. When right-justified, six leading "0"s are output on DO before the MSB, and the complete conversion result is shifted out in 16 clock periods.

2.3 $\overline{CS}$ HIGH DURING CONVERSION

With a continuous S_{CLK} input, $\overline{CS}$ must be used to synchronize the serial data exchange. A valid $\overline{CS}$ is recognized if it occurs at least 100 ns (t_{SET-UP}) before the rising edge of S_{CLK}, thus causing data to be input on DI. If this does not

2.0 Functional Description (Continued)

occur there will be an uncertainty as to which S_{CLK} rising edge will clock in the first bit of data. $\overline{CS}$ must remain low during the complete I/O exchange. Also, $\overline{OE}$ needs to be low if data from the previous conversion needs to be accessed.

2.3 $\overline{CS}$ LOW CONTINUOUSLY

Another way to accomplish synchronous serial communication is to tie $\overline{CS}$ low continuously and use SARS and S_{CLK} to synchronize the serial data exchange. S_{CLK} can be disabled low during the conversion time and enabled after SARS goes low. With $\overline{CS}$ low during the conversion time a zero will remain on DO until the conversion is completed. Once the conversion is complete, the falling edge of SARS will shift out on DO the MSB before S_{CLK} is enabled. This MSB would be a leading zero if right-justified or D9 if left-justified. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously. If $\overline{CS}$ goes high during the conversion sequence DO is put into TRI-STATE, and the conversion result is not affected so long as $\overline{CS}$ remains high until the end of the conversion.

2.4 TYING S_{CLK} and C_{CLK} TOGETHER

S_{CLK} and C_{CLK} can be tied together. The total conversion time will increase because the maximum clock frequency is now 1 MHz. The timing diagrams and the serial I/O exchange time (10 S_{CLK} cycles) remain the same, but the conversion time (T_C = 41 C_{CLK} cycles) lengthens from a minimum of 14 μs to a minimum of 41 μs. In the case where $\overline{CS}$ is low continuously, since the applied clock cannot be disabled, SARS must be used to synchronize the data output on DO and initiate a new conversion. The falling edge of SARS sends the MSB information out on DO. The next rising edge of the clock shifts in MUX address bit A2 on DI. The following clock falling edge will clock the next data bit of information out on DO. A conversion will be started after MUX addressing information has been loaded in (3 more clocks) and the analog sampling time (4.5 clocks) has elapsed. The ADC1031 does not have SARS. Therefore, $\overline{CS}$ cannot be left low continuously on the ADC1031.

3.0 Analog Considerations

3.1 THE INPUT SAMPLE AND HOLD

The ADC1031/4/8's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for 4.5 S_{CLK} cycles after the multiplexer addressing information is loaded in. For the ADC1031/4/8, the sampling of the analog input starts on S_{CLK}'s 4th rising edge.

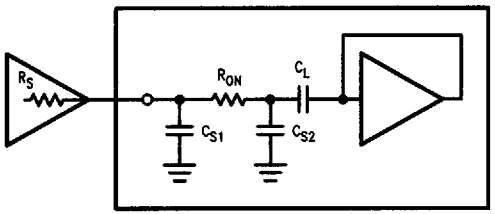


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FIGURE 1. Analog Input Model

An acquisition window of 4.5 S_{CLK} cycles is available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (9 kΩ) of the multiplexer switches, the C_{S1} (3.5 pF) and the total ladder (C_L) and stray (C_{S2}) capacitance (48 pF). For large source resistance the analog input can be modeled as an RC network as shown in *Figure 1*. The values shown yield an acquisition time of about 3 μs for 10 bit accuracy with a zero to a full scale change in the reading. External source resistance and capacitance will lengthen the acquisition time and should be accounted for.

The curve "Signal to Noise Ratio vs Output Frequency" *(Figure 2)* gives an indication of the usable bandwidth of the ADC1031/ADC1034/ADC1038. The signal to noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the A/D. An ideal 10 bit A/D converter with a total unadjusted error of 0 LSB would have a signal to noise ratio of about 62 dB, which can be derived from the equation:

$$S/N = 6.02(N) + 1.8$$

where S/N is in dB and N is the number of bits. *Figure 2* shows the signal to noise ratio vs. input frequency of a typical ADC1031/4/8 with ½ LSB total unadjusted error. The dotted lines show signal-to-noise ratios for an ideal (noiseless) 10 bit A/D with 0 LSB error and an A/D with a 1 LSB error.

The sample-and-hold error specifications are included in the error and timing specifications of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC1031/4/8's total unadjusted error specification, while the hold settling time is included in the A/D's maximum conversion time specification. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

3.2 INPUT FILTERING

Due to the sampling nature of the analog input, transients will appear on the input pins. They are caused by the ladder capacitance and internal stray capacitance charging current flowing into V_{IN}. These transients will not degrade the A/D's performance if they settle out within the sampling window. This will occur if external source resistance is kept to a minimum.

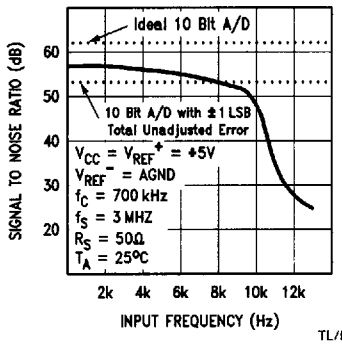

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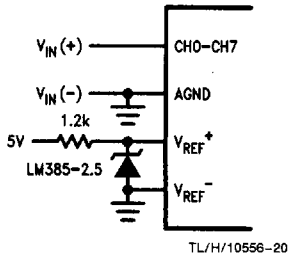
FIGURE 2. ADC1031/4/8 Signal to Noise Ratio vs Input Frequency

3.0 Analog Considerations (Continued)

External Reference 2.5V Full Scale



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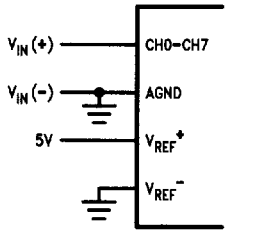
Power Supply as Reference



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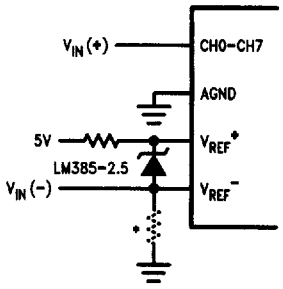
Input Not Referred to GND



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*Current path must still exist from $V_{IN}(-)$ to ground

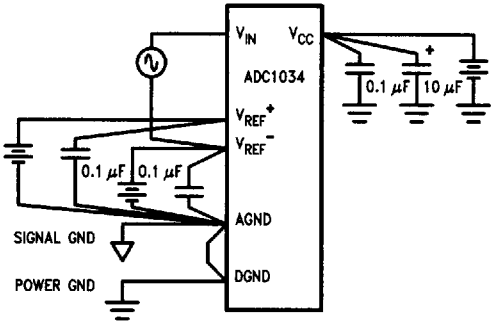
FIGURE 3. Analog Input Options

3.3 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC1031/4/8 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{REF}+$ and $V_{REF}-$. By reducing V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF} = 2V then 1 LSB = 1.95 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}-$ sets the input level which produces a digital output of all zeros. Though V_{IN} is not itself differential, the reference design allows nearly differential-input capability for many measurement applications. *Figure 3* shows some of the configurations that are possible.

Power Supply Bypassing



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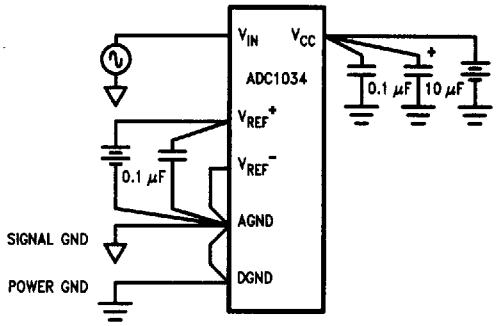

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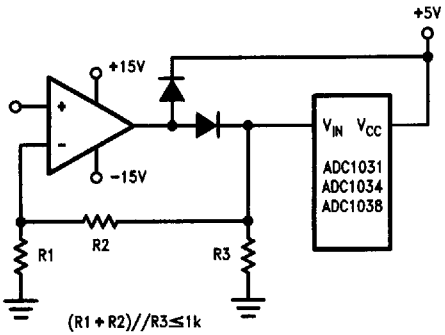
2

Protecting the Analog Inputs



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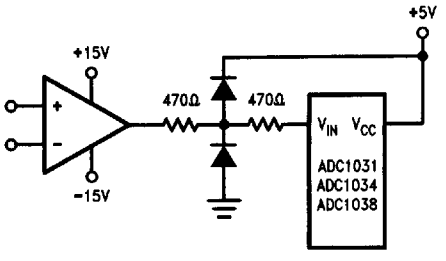

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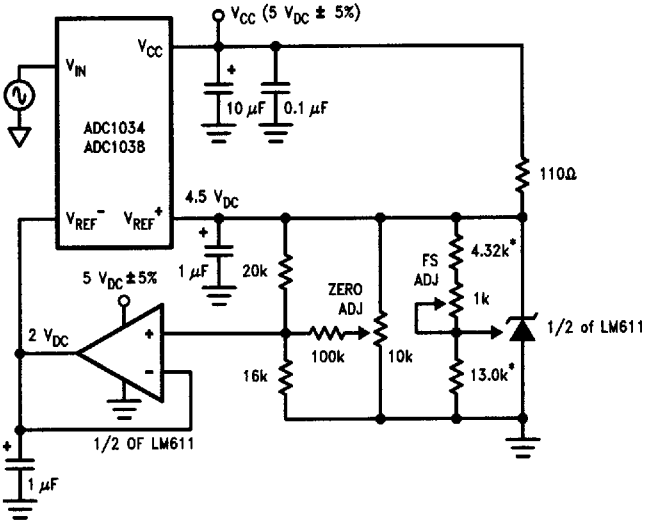
Diodes are IN914

Zero-Shift and Span-Adjust (2V ≤ V_{IN} ≤ 4.5V)



*1% resistors

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