

June 1989

2K x 8 CMOS RAM

### Features

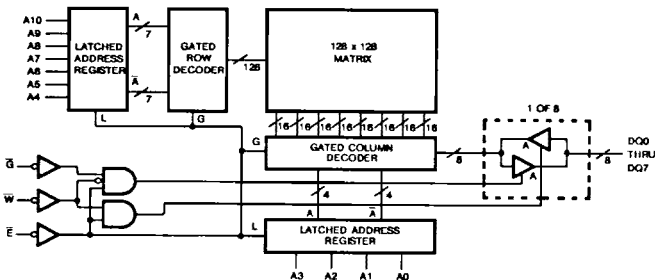
- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 275 $\mu$ W Max.
- Low Power Operation ..... 55mW/MHz Max.
- Fast Access ..... 120/200ns Max.
- Industry Standard Pinout
- Single Supply ..... 5.0 Volt VCC
- TTL Compatible
- Static Memory Cells
- High Output Drive
- On-Chip Address Latches
- Easy Microprocessor Interfacing

### Description

The HM-6516/883 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, which also gives fast access times. The pinout of the HM-6516/883 is the popular 24 pin, 8-bit wide JEDEC standard which allows easy memory board layouts, flexible enough to accommodate a variety of PROMs, RAMS, EPROMs, and ROMs.

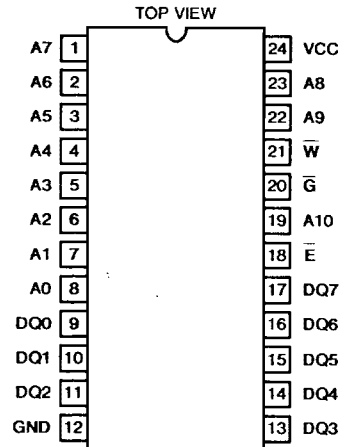
The HM-6516/883 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

### Functional Diagram

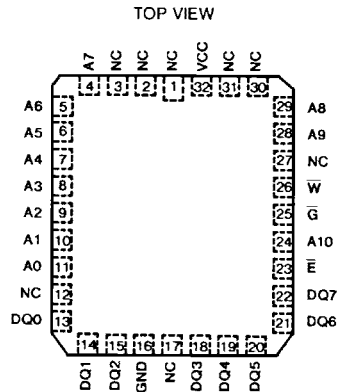


### Pinouts

HM1-6516/883 (CERAMIC DIP)



HM4-6516/883 (CERAMIC LCC)



PIN	DESCRIPTION
NC	No Connect
A <sub>0</sub> - A <sub>10</sub>	Address Inputs
E	Chip Enable/Power Down
V <sub>SS</sub> /GND	Ground
DQ <sub>0</sub> - DQ <sub>7</sub>	Data In/Data Out
VCC	Power (+5V)
W	Write Enable
G	Output Enable

# Specifications HM-6516/883

## Absolute Maximum Ratings

Supply Voltage .....	+7.0V
Input or Output Voltage Applied for all grades .....	GND-0.3V to VCC+0.3V
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+175°C
Lead Temperature (Soldering 10 sec).....	+300°C
ESD Classification .....	Class 1

## Reliability Information

Thermal Resistance	$\theta_{ja}$	$\theta_{jc}$
Ceramic DIP Package .....	48°C/W	8°C/W
Ceramic LCC Package .....	86°C/W	12°C/W
Maximum Package Power Dissipation at +125°C		
Ceramic DIP Package .....	1W	
Ceramic LCC Package .....	0.75W	
Gate Count .....	25953 Gates	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Operating Conditions

Operating Temperature Range .....	-55°C to +125°C	Input High Voltage .....	+2.4V to VCC
Operating Supply Voltage .....	4.5V to 5.5V	Data Retention Supply Voltage .....	2.0V to 4.5V
Input Low Voltage .....	0 to +0.8V	Input Rise and Fall Time .....	40ns Max

**TABLE 1. HM-6516/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Guaranteed and 100% Tested. VCC = 5.0V ± 10% Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH	VCC = 4.5V, IO = -1.0mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 3.2mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = $\bar{G}$ = 5.5V, VIO = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	1.0	μA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	1.0	μA
Operating Supply Current	ICCOP	VCC = $\bar{G}$ = 5.5V, (Note 2), f = 1MHz, VI = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	10	mA
Standby Supply Current	ICCSB1	VCC = 5.5V, HM-6516/883 $\bar{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	100	μA
		VCC = 5.5V, HM-6516B/883 $\bar{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	50	μA
Data Retention Supply Current	ICCDR	VCC = 2.0V, HM-6516/883 $\bar{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	50	μA
		VCC = 2.0V, HM-6516B/883 $\bar{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	25	μA
Functional Test	FT	VCC = 4.5V (Note 4)	7, 8A, 8B	-55°C ≤ TA ≤ +125°C	-	-	

**CAUTION:** These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

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## Specifications HM-6516/883

**TABLE 2. HM-6516/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Devices Guaranteed and 100% Tested. VCC = 5.0V ± 10% Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	(NOTES 1, 5) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Read/Write/ Cycle Time	TELEL	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	280	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	170	-	ns
Address Access Time	TAVQV (Note 6)	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	200	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	120	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	200	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	120	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	120	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	120	-	ns
Data Set-Up Time	TDVWH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	80	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883			50	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	10	-	ns
Write Enable Pulse Set-up Time	TWLEH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883			120	-	ns
Address Set-Up Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	0	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	50	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883			30	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	80	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	50	-	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	-55°C ≤ T <sub>A</sub> ≤ +125°C	120	-	ns

NOTES: 1. All voltages referenced to Device Ground.

2. Typical derating = 5mA/MHz increase in ICCOP.

3. Shall be tested initially, and after any design changes.

4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

5. AC measurements assume transition time ≤ 5ns; input levels = 0V to 3V; timing reference levels = 1.5V; output load = CL ≥ 50pF and 1 TTL equivalent load; and for CL > 50pF, CL < 300pF, access time are derated by 0.15ns/pF.

6. TAVQV = TELQV + TAVEL.

# Specifications HM-6516/883

**TABLE 3. HM-6516/883 ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open T <sub>A</sub> = +25°C, f = 1MHz, All Measurements Referenced to Device GND	1, 2	T <sub>A</sub> = +25°C	-	8	pF
		VCC = Open T <sub>A</sub> = +25°C, f = 1MHz, All Measurements Referenced to Device GND	1, 3	T <sub>A</sub> = +25°C	-	12	pF
Input/Output Capacitance	CI/O	VCC = Open T <sub>A</sub> = +25°C, f = 1MHz, All Measurements Referenced to Device GND	1, 2	T <sub>A</sub> = +25°C	-	10	pF
		VCC = Open T <sub>A</sub> = +25°C, f = 1MHz All Measurements Referenced to Device GND	1, 3	T <sub>A</sub> = +25°C	-	14	pF
Output Enable To Output Valid Time	TGLQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	10	-	ns
Chip Enable To Output Valid Time	TELQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	10	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V HM-6516/883	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	80	ns
		VCC = 4.5V and 5.5V HM-6516B/883	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	50	ns
Output Disable Time	TGHQZ	VCC = 4.5V and 5.5V HM-6516/883	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	80	ns
		VCC = 4.5V and 5.5V HM-6516B/883	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	50	ns
Write Enable Output Disable Time	TWLQZ	VCC = 4.5V and 5.5V HM-6516/883	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	80	ns
		VCC = 4.5V and 5.5V HM-6516B/883	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	50	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	1	-55°C ≤ T <sub>A</sub> ≤ +125°C	-	80	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

- 2. Applies to LCC device types only.
- 3. Applies to DIP device types only.

**TABLE 4. APPLICABLE SUBGROUPS**

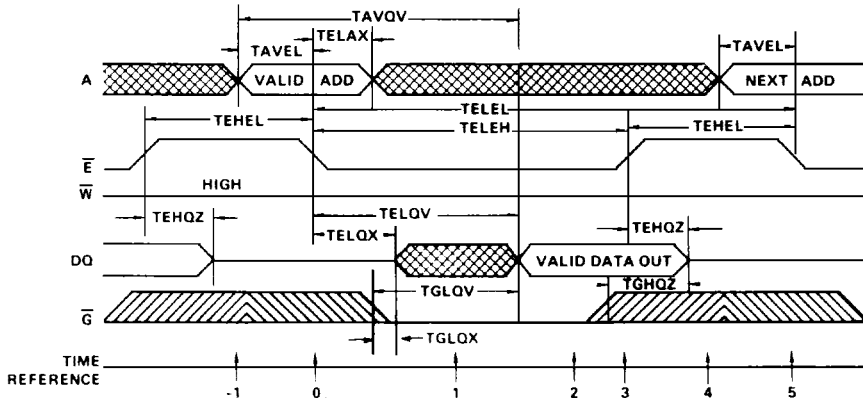
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

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**Timing Waveforms**

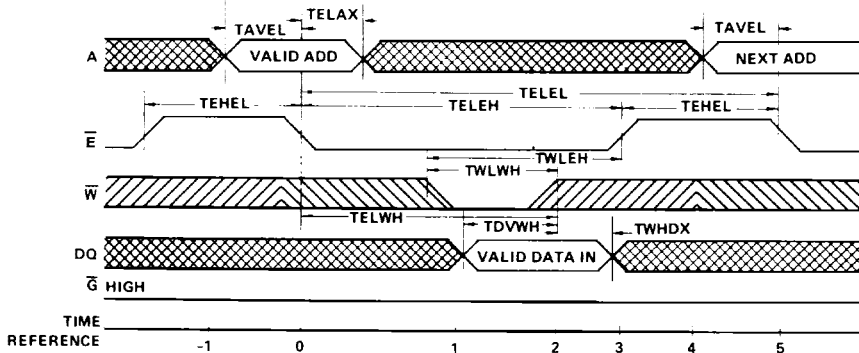
**READ CYCLE** HM-6516/883 and HM-6516B/883



The address information is latched in the on chip registers on the falling edge of  $\bar{E}$  ( $T = 0$ ), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time ( $T = 1$ ), the outputs become enabled but data is not valid until time ( $T = 2$ ),  $\bar{W}$  must re-

main high throughout the read cycle. After the data has been read,  $\bar{E}$  may return high ( $T = 3$ ). This will force the output buffers into a high impedance mode at time ( $T = 4$ ).  $\bar{G}$  is used to disable the output buffers when in a logical "1" state ( $T = -1, 0, 3, 4, 5$ ). After ( $T = 4$ ) time, the memory is ready for the next cycle.

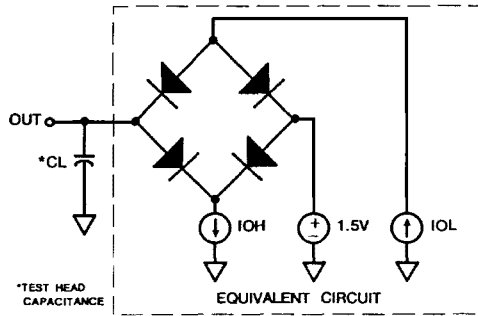
**WRITE CYCLE** HM-6516/883 and HM-6516B/883



The write cycle is initiated on the falling edge of  $\bar{E}$  ( $T = 0$ ), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active,  $\bar{G}$  can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of  $\bar{G}$ . If  $\bar{E}$  and  $\bar{G}$  fall before  $\bar{W}$  falls (read mode), a possible bus conflict may exist. If  $\bar{E}$  rises before  $\bar{W}$  rises, reference data setup and hold times to the  $\bar{E}$  rising edge. The

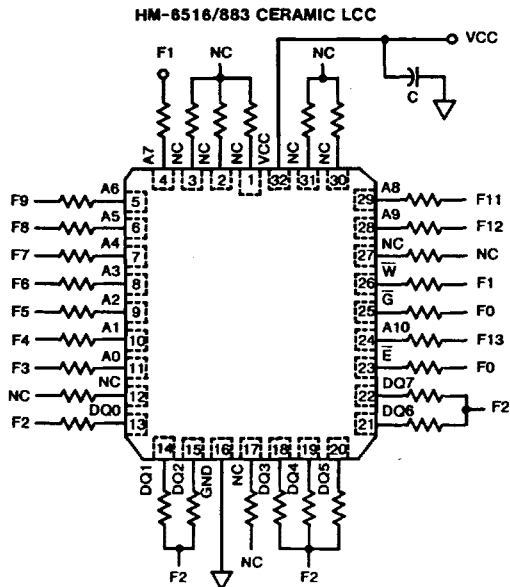
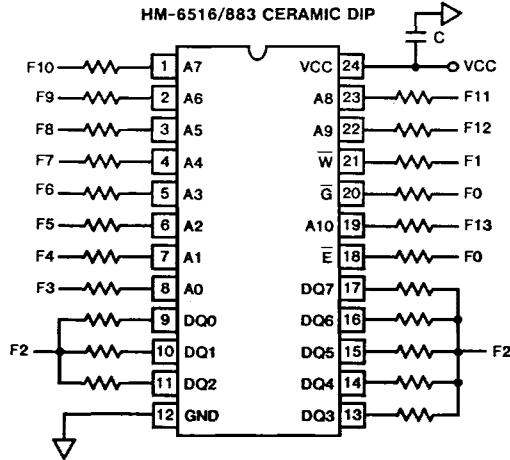
write operation is terminated by the first rising edge of  $\bar{W}$  ( $T = 2$ ) or  $\bar{E}$  ( $T = 3$ ). After the minimum  $\bar{E}$  high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the  $\bar{W}$  line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of  $\bar{E}$ .

Test Load Circuit



\*TEST HEAD CAPACITANCE

Burn-In Circuits



NOTES:

- All resistors 47kΩ 5%
- F0 = 100kHz ± 10%
- VCC = 5.5V ± .5V
- VIH = 4.5V ± 10%
- VIL = -0.2V - +0.4V
- C = 0.01μF min

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**Metallization Topology**

**DIE DIMENSIONS:**

186.6 x 199.6 x 19 ± 1mils

**METALLIZATION:**

Type: Si - Al  
 Thickness: 9kÅ - 13kÅ

**GLASSIVATION:**

Type: SiO<sub>2</sub>  
 Thickness: 7kÅ - 9kÅ

**DIE ATTACH:**

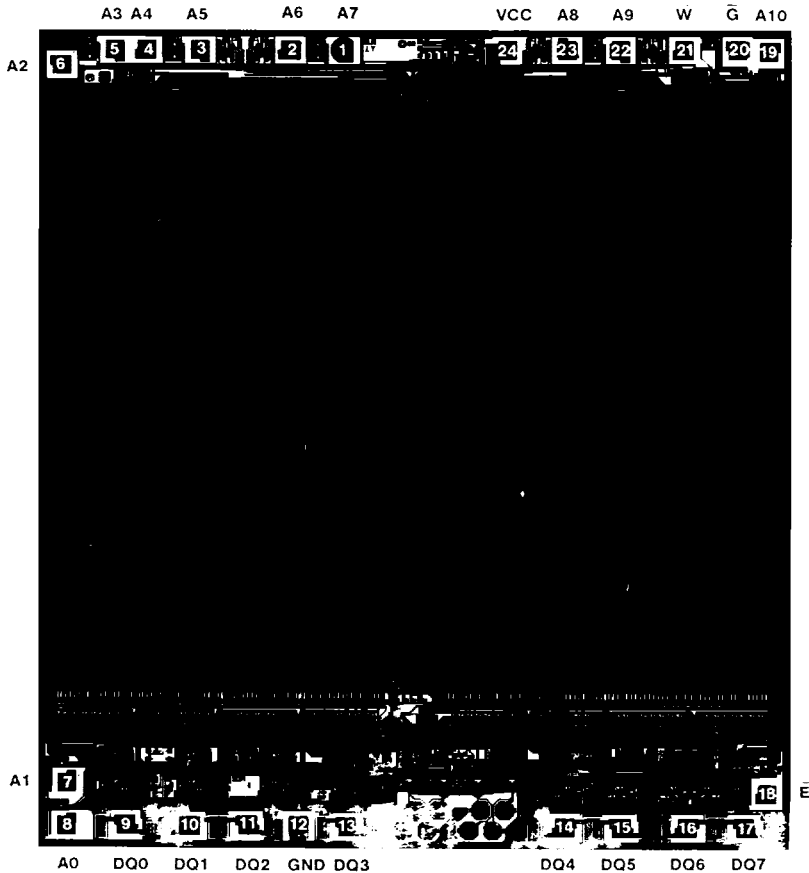
Material: Gold/Silicon Eutectic Alloy  
 Temperature: Ceramic DIP — 460°C (Max)  
 Ceramic LCC — 420°C (Max)

**WORST CASE CURRENT DENSITY:**

0.5 x 10<sup>5</sup> A/cm<sup>2</sup>

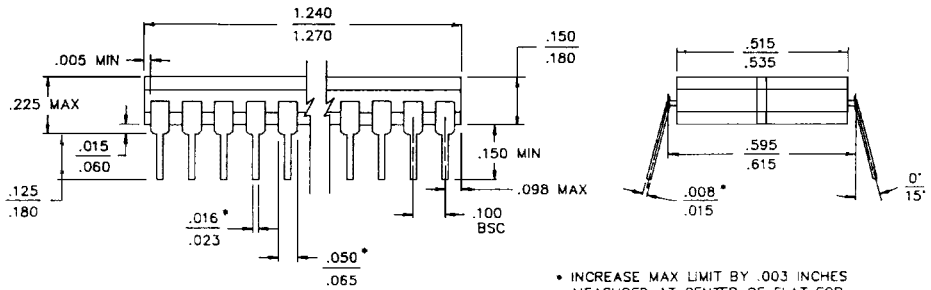
**Metallization Mask Layout**

HM-6516/883



**Packaging†**

**24 PIN CERAMIC DIP**

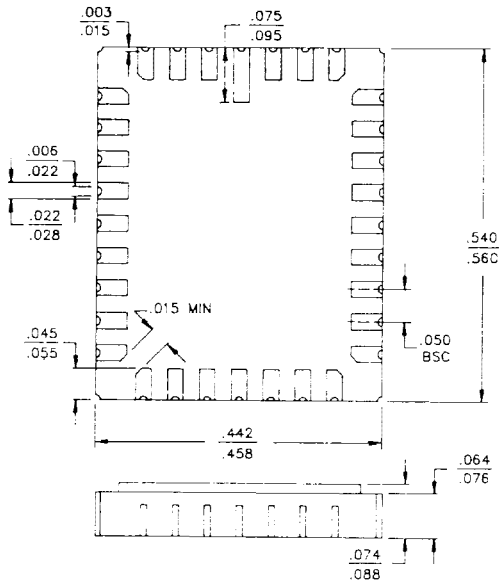


• INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

**LEAD MATERIAL:** Type B  
**LEAD FINISH:** Type A  
**PACKAGE MATERIAL:** Ceramic, 90% Alumina  
**PACKAGE SEAL:**  
 Material: Glass Frit  
 Temperature: 450°C ± 10°C  
 Method: Furnace Seal

**INTERNAL LEAD WIRE:**  
 Material: Aluminum  
 Diameter: 1.25 Mil  
 Bonding Method: Ultrasonic  
**COMPLIANT OUTLINE:** 38510 D-3

**32 PAD CERAMIC LCC**



**PAD MATERIAL:** Type C  
**PAD FINISH:** Type A  
**FINISH DIMENSION:** Type A  
**PACKAGE MATERIAL:** Multilayer Ceramic, 90% Alumina  
**PACKAGE SEAL:**  
 Material: Gold/Tin (80%/20%)  
 Temperature: 320°C ± 10°C  
 Method: Furnace Braze

**INTERNAL LEAD WIRE:**  
 Material: Aluminum  
 Diameter: 1.25 Mil  
 Bonding Method: Ultrasonic  
**COMPLIANT OUTLINE:** 38510 C-12

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NOTE: All Dimensions are  $\frac{\text{Min}}{\text{Max}}$ . Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.



## DESIGN INFORMATION

### 2K x 8 CMOS RAM

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

