November 2001

# IRF830B/IRFS830B

# FAIRCHILD SEMICONDUCTOR

# IRF830B/IRFS830B **500V N-Channel MOSFET**

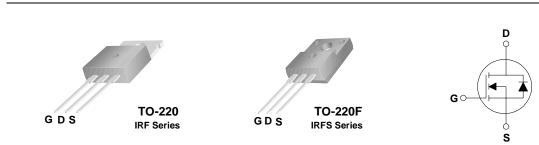
#### **General Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

#### Features

- + 4.5A, 500V,  $R_{DS(on)}$  = 1.5 $\Omega$  @V\_{GS} = 10 V + Low gate charge ( typical 27 nC)
- Low Crss (typical 17 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



# Absolute Maximum Ratings T<sub>c</sub> = 25°C unless otherwise noted

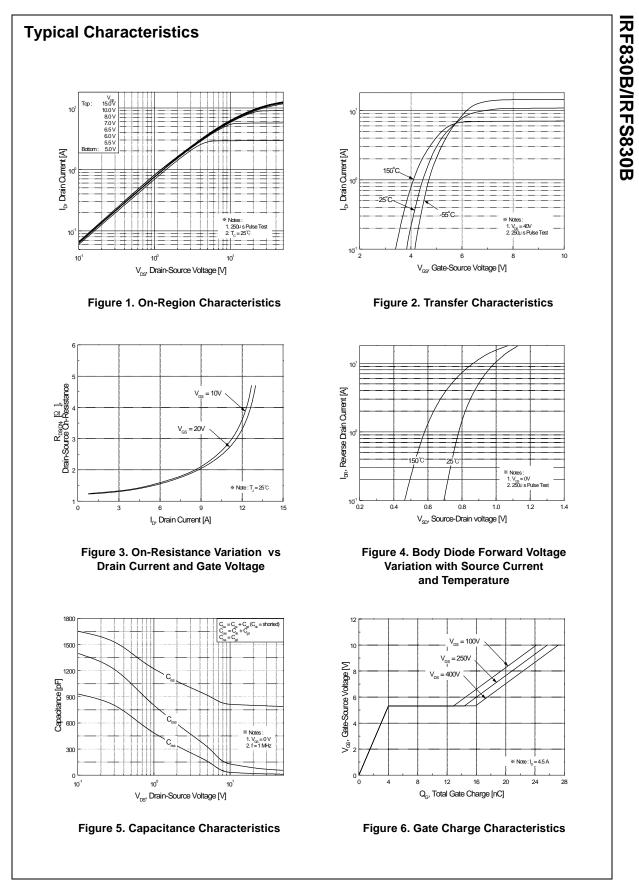
Symbol	Parameter	IRF830B	IRFS830	Units	
V <sub>DSS</sub>	Drain-Source Voltage		500		V
I <sub>D</sub>	Drain Current - Continuous ( $T_C = 25^{\circ}C$ )		4.5	4.5 *	А
	- Continuous (T <sub>C</sub> = 100°C)		2.9	2.9 *	A
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	18	18 *	А
V <sub>GSS</sub>	Gate-Source Voltage	± 30		V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	270		mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	4.5		Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	7.3		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.5		V/ns
PD	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C		73	38	W
			0.58	0.3	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C
ΤL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		30	00	°C

\* Drain current limited by maximum junction temperature

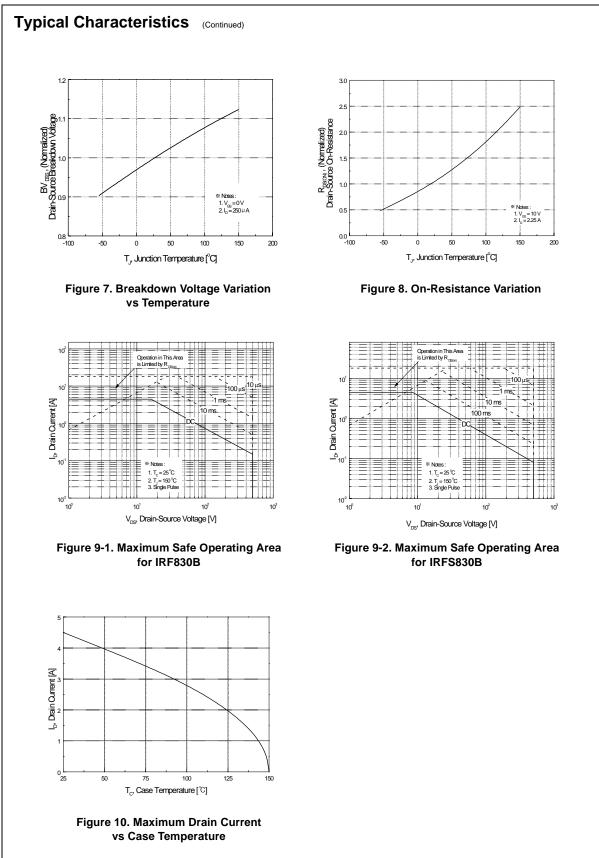
# **Thermal Characteristics**

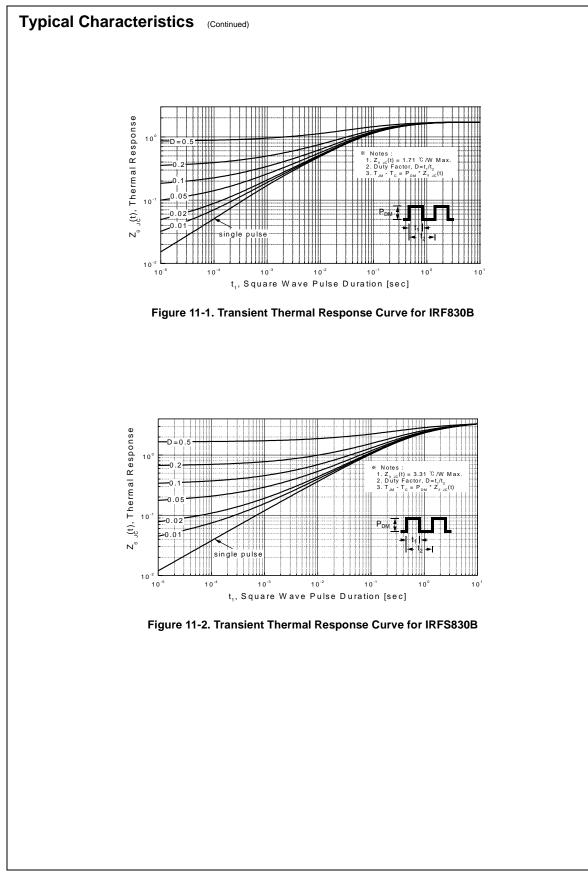
Symbol	Parameter	IRF830B	IRFS830B	Units
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction-to-Case Max.	1.71	3.31	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5		°C/W
$R_{\thetaJA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	°C/W

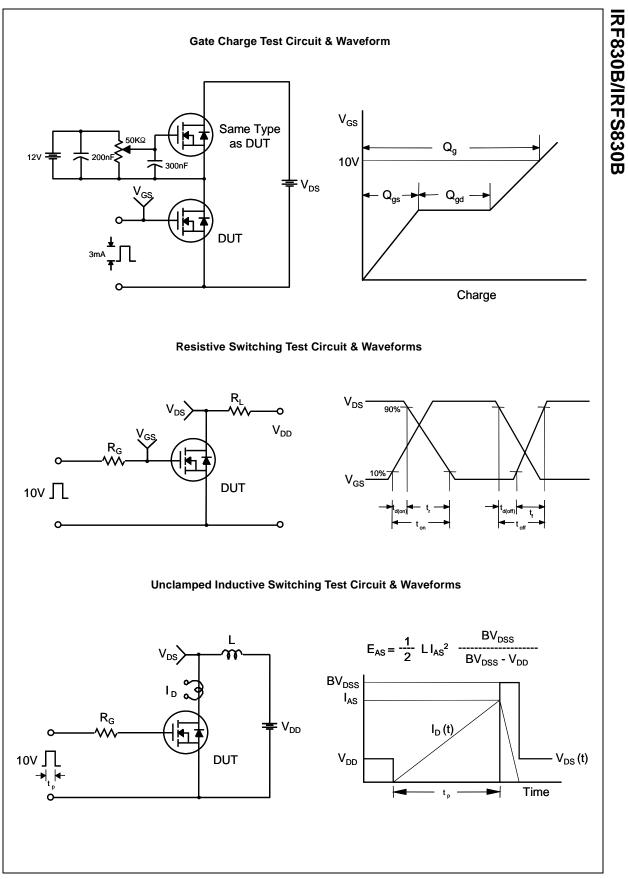
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, Referenced to 25°C		0.54		V/°C
DSS		$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$			10	μΑ
	Zero Gate Voltage Drain Current	$V_{DS} = 400 \text{ V}, \text{ T}_{C} = 125^{\circ}\text{C}$			100	μΑ
GSSF	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
GSSR	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 2.25 \text{ A}$		1.16	1.5	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40 \text{ V}, \text{ I}_{D} = 2.25 \text{ A}$ (Note 4)		4.2		S
Dvnam	ic Characteristics		1		1	
C <sub>iss</sub>	Input Capacitance			800	1050	pF
C <sub>OSS</sub>	Output Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		76	100	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			17	22	pF
d(on)	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 4.5 A,		15	40	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 250 \text{ V}, \text{ I}_{D} = 4.5 \text{ A},$ R <sub>G</sub> = 25 Ω		40	90	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			85	180	ns
<sup>t</sup> f	Turn-Off Fall Time	(Note 4, 5)		45	100	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 4.5 A,		27	35	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		4.0		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4, 5)		12		nC
Drain-S	ource Diode Characteristics ar	nd Maximum Ratings				
s	Maximum Continuous Drain-Source Dic				4.5	А
ISM	Maximum Pulsed Drain-Source Diode F	Forward Current			18	А
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_{S} = 4.5 A$			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 V, I_{S} = 4.5 A,$		305		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_{F} / dt = 100 \text{ A}/\mu \text{s} $ (Note 4)		2.6		μC
L = 24mH, I, I <sub>SD</sub> $\leq$ 4.5A, Pulse Test :	ating : Pulse width limited by maximum junction temper $A_S = 4.5A$ , $V_{DD} = 50V$ , $R_G = 25 \Omega$ , Starting $T_J = 25^{\circ}C$ d/dt $\leq 300A/\mu$ s, $V_{DD} \leq BV_{DSS}$ , Starting $T_J = 25^{\circ}C$ Pulse width $\leq 300 \mu$ s, Duty cycle $\leq 2\%$ ordenendent of concrition temperature	rature				
Essentially i	ndependent of operating temperature					



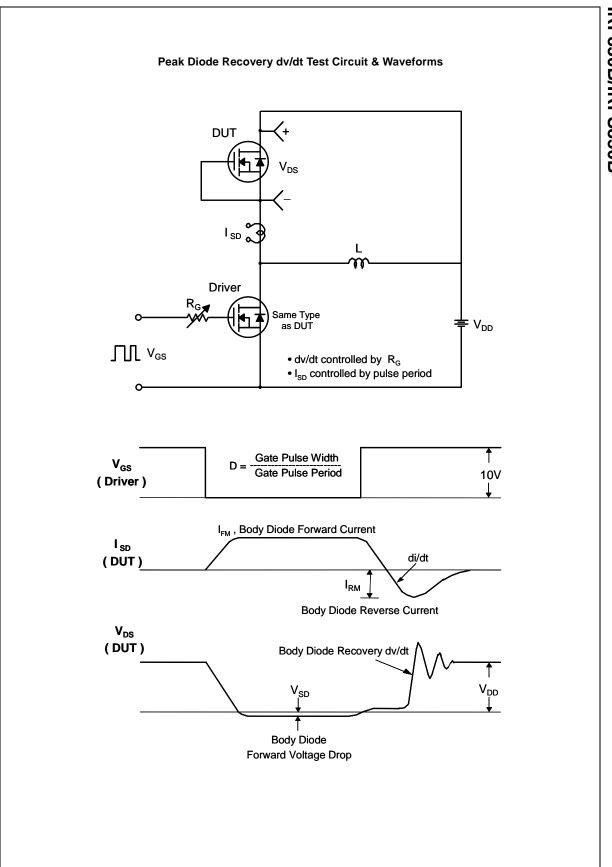
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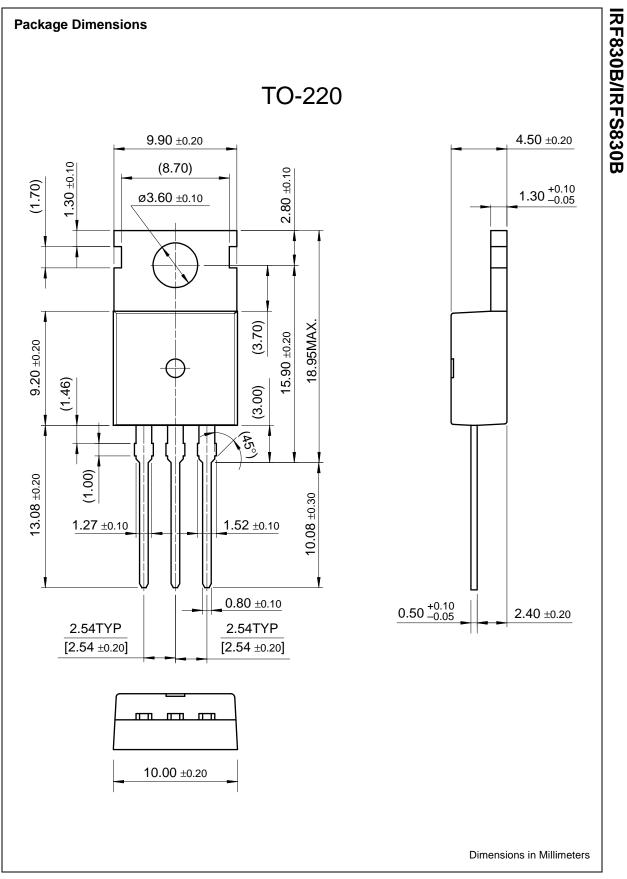




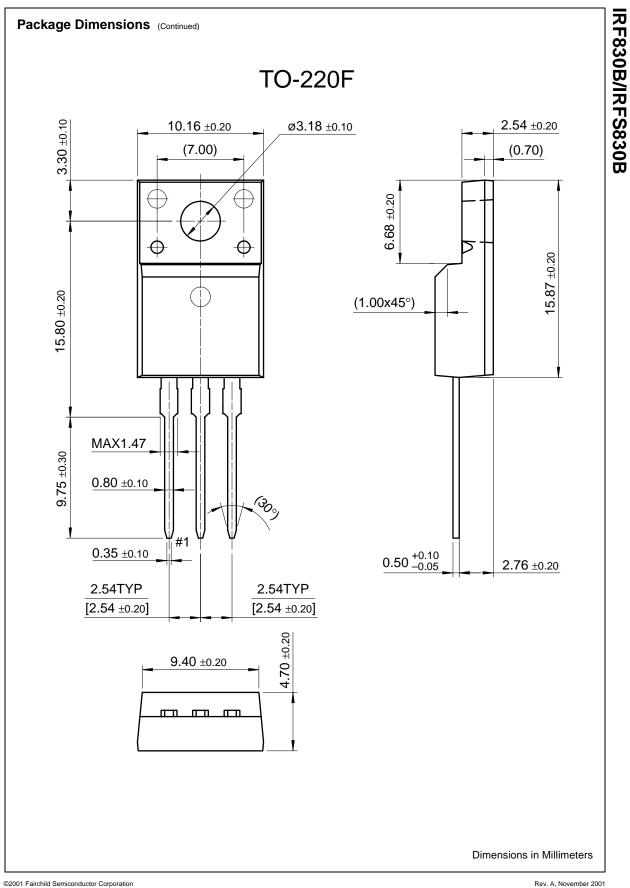


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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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<u>Memory</u> Optoelectronics <u>Markets and</u> applications	General description These N-Channel enhancement mode power	e-mail this datasheet	Support Dotted line Distributor and field sales representatives Dotted line Quality and reliability
<u>New products</u> <u>Product selection and</u> <u>parametric search</u> <u>Crosse reference</u>	field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.	This page Print version	Dotted line Design tools
Cross-reference search technical information	This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and		
buy products	<ul> <li>withstand high energy pulse in the avalanche and commutation mode. These devices are well</li> <li>suited for high efficiency switch mode power</li> </ul>		
technical support	supplies, power factor correction and electronic- lamp ballasts based on half bridge.	-	
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Features

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Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Packing method
			,	,	

IRFS830B	Full Production	\$0.66	<u>TO-220F</u>	3	RAIL
IRFS830BT	Full Production	\$0.66	<u>TO-220F</u>	3	RAIL

\* 1,000 piece Budgetary Pricing

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Application notes

AN-4121: AN-4121 Design of Power Factor Correction Circuit Using FAN7527B (124 K) Jul 19, 2002

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