19-5669; Rev 2; 12/11

73S8014BN
Smart Card Interface

ISO/IEC 7816-3

DS_8014BN_057

DESCRIPTION

The 73S8014BN is a single smart card (ICC) interface circuit designed to provide full electrical compliance with ISO 7816-3, EMV® 4.2, and NDS specifications. It is derived from the 73S8024RN industry-standard electrical interface, but adds support for 1.8V smart card applications. The 73S8014BN has been optimized to match set-top box/A/V conditional access applications. The optimization adds functionality while creating a device with a smaller pin count. For NDS applications requiring an on-chip adjustable POR, see the Maxim 73S8024RN series of interface ICs.

The 73S8014BN interfaces with the host processor through the same bus (digital I/Os) as the 73S8024RN and most other 8024 type devices. **As a result, the 73S8014BN is a very attractive cost-reduction path from traditional 8024 ICs.**

Interfacing with the system controller is done through a control bus, composed of digital inputs to control the 73S8014BN, and one interrupt output to inform the system controller of the card presence, device readiness and faults.

The card clock can be generated by an on-chip oscillator using an external crystal or by connection to an externally supplied clock signal. In addition, the clock divider provides divisor values of divide by 1, 2, 4, and 8 that are controlled through a single pin.

The 73S8014BN incorporates an ISO 7816-3 activation/deactivation sequencer that controls the card signals. Level-shifters drive the card signals with the selected card voltage (1.8V, 3V, or 5V), coming from an internal low dropout (LDO) voltage regulator. This LDO regulator is powered by a dedicated power-supply input, V_{PC}. Digital circuitry is powered separately by a digital power supply, V_{DD}. With its embedded LDO regulator, the 73S8014BN is a cost-effective solution for any application where a 5V (typically -5% +10%) power supply is available.

Emergency card deactivation is initiated upon card extraction or upon any fault detected by the protection circuitry. The fault can be a card overcurrent, V_{CC} undervoltage, or power-supply fault (V_{DD}). The card overcurrent circuitry is a true current-detection function, as opposed to V_{CC} voltage drop detection, as usually implemented in non-Maxim 8024 interface ICs.

The 73S8014BN contains a power-down mode with typical power consumption of 1µA on each of the V_{DD} and V_{PC} supplies. The power-down mode is controlled through existing control pins without the need for a dedicated control pin.

APPLICATIONS

- **Set-Top Box Conditional Access and Pay-per-View**
- **General-Purpose Smart Card Readers**

ADVANTAGES

- **NDS Compliant**
- **Same Advantages as the Maxim 73S80xxR Family:**
  - Card V_{CC} Generated by an LDO Regulator
  - Very Low Power Dissipation (Saves Up to 1/2W)
  - Fewer External Components Are Required
  - Better Noise Performance
- **True Card Overcurrent Detection**
- **Firmware Compatibility with 8024 ICs**
- **Small-Format 20-Pin SO Package Capable of Fully Supporting NDS Applications**
- **Power-Down Mode**

FEATURES

- **Card Interface**
  - Complies with ISO 7816-3, EMV 4.2, and NDS
  - Supports 3V/5V Cards Up to 65mA and 1.8V Cards Up to 40mA
  - ISO 7816-3 Activation/Deactivation Sequencer
  - Automated Deactivation Upon Hardware Fault (i.e., Upon Drop on V_{DD} Power Supply or Card Overcurrent)
  - Overcurrent Detection 145mA max
  - Card CLK Clock Frequency Up to 20MHz
- **System Controller Interface**
  - Three Digital Inputs Control the Card Activation/Deactivation, Card Reset, Power-Down, and Card Voltage
  - One Digital Input Controls the Card Clock Frequency
  - One Digital Output, Interrupt to the System Controller, Reports to the Host the Card Presence, Device Readiness, and Faults
  - Crystal Oscillator or Host Clock, Up to 27MHz
- **Regulator Power Supply**
  - 4.75V to 5.5V (EMV 4.2)
  - 4.85V to 5.5V (NDS)
- **Digital Interfacing: 2.7V to 3.6V**
- **±6kV ESD Protection on the Card Interface**
- **20-Pin SO Package**
- **RoHS-Compliant (6/6)/Lead(Pb)-Free Package**

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FUNCTIONAL DIAGRAM

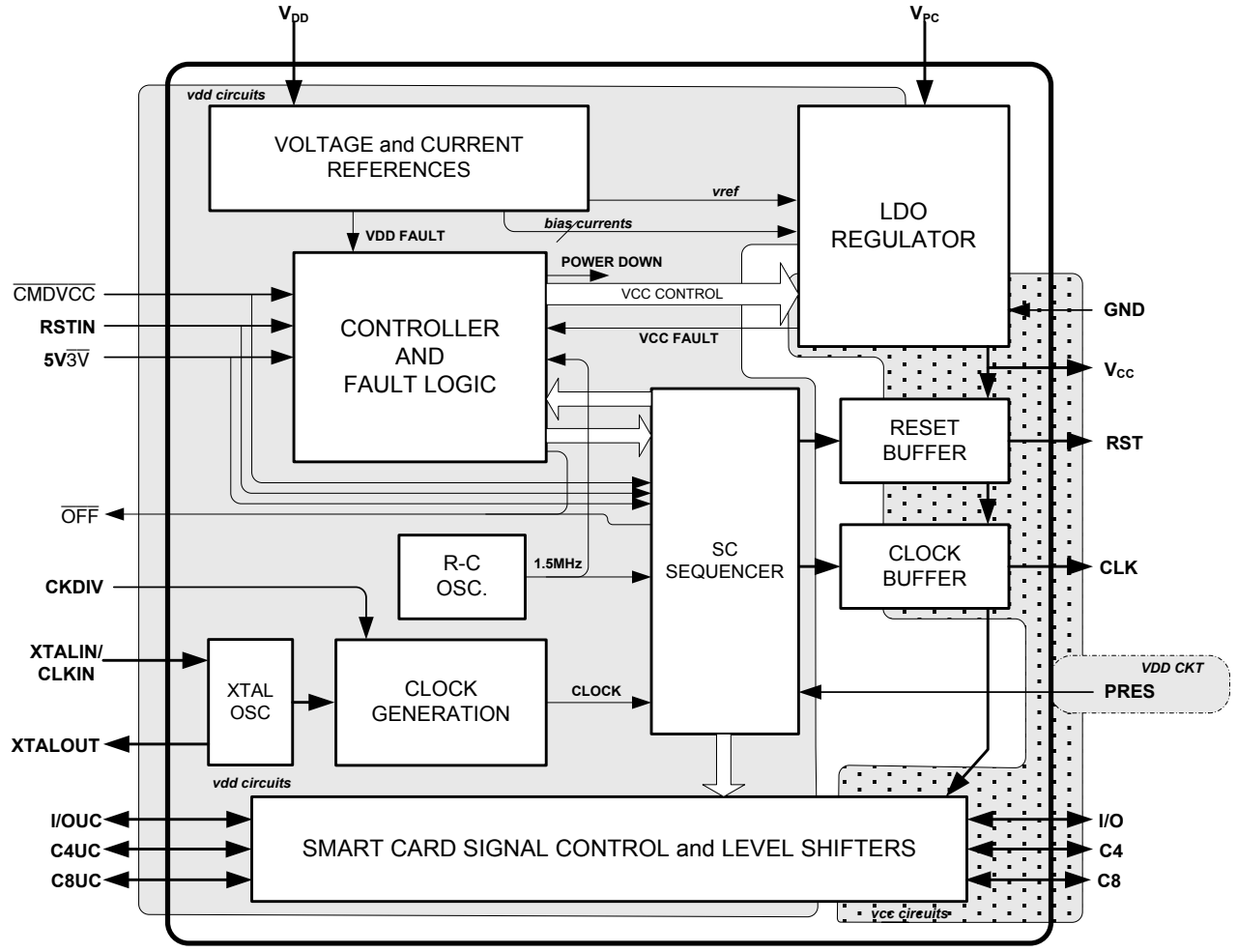

Figure 1: 73S8014BN Block Diagram

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1 Pinout

The 73S8014BN is offered in a 20-pin SO package.

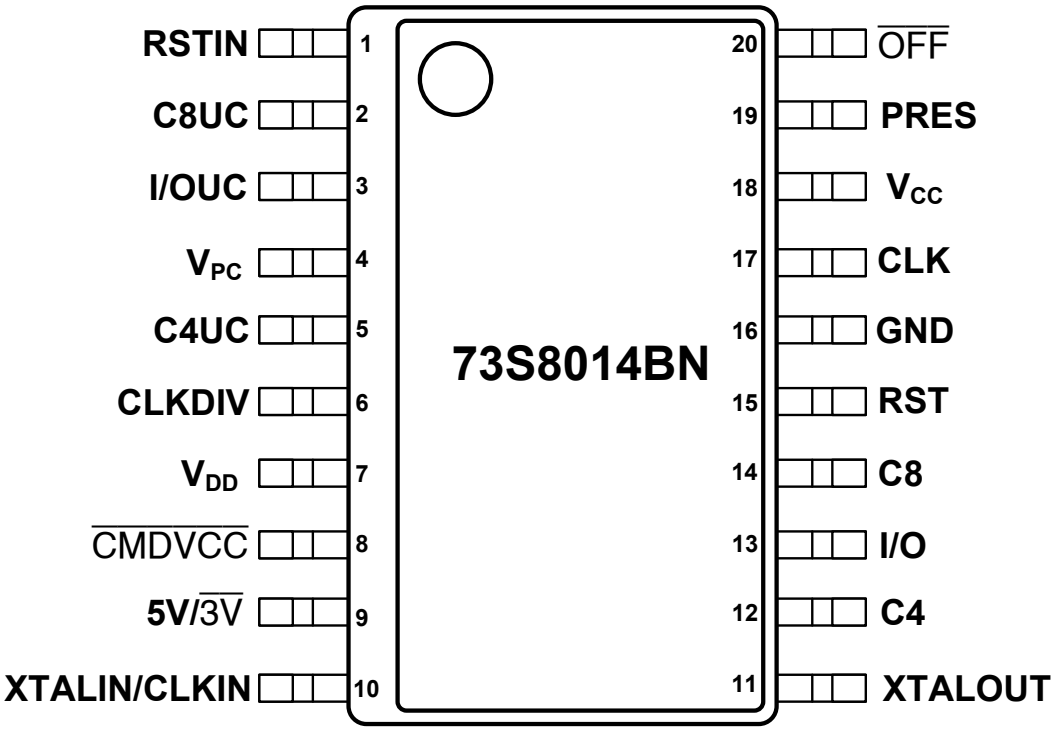


Figure 2: 73S8014BN 20-SO Pinout

Table 1 provides the 73S8014BN pin names, pin numbers, type, equivalent circuits, and descriptions.

Table 1: 73S8014BN 20-Pin SO Pin Definitions

NAME	PIN	TYPE	EQUIVALENT CIRCUIT FIGURE #	DESCRIPTION
CARD INTERFACE				
I/O	13	IO	Figure 16	Card I/O: Data Signal to/from Card. Includes an 11kΩ pullup resistor to V_{CC}.
C4	12	IO	Figure 16	Card C4: Data Signal to/from Card. Includes an 11kΩ pullup resistor to V_{CC}.
C8	14	IO	Figure 16	Card C8: Data Signal to/from Card. Includes an 11kΩ pullup resistor to V_{CC}.
RST	15	O	Figure 15	Card Reset. Provides reset (RST) signal to card.
CLK	17	O	Figure 14	Card Clock: Provides clock signal (CLK) to card. The rate of this clock is determined by the external crystal frequency or frequency of the external clock signal applied on XTALIN and CLKDIV selections.
PRES	19	I	Figure 18	Card Presence Switch. Active high indicates the card is present. Includes a high-impedance pulldown current source. The PRES input includes a 5ms debounce for card insertion.
V_{CC}	18	PSO	Figure 13	Card Power Supply. Logically controlled by sequencer, output of LDO regulator. Requires an external filter capacitor to the card GND.
GND	16	GND	—	Card and Digital Ground
HOST PROCESSOR INTERFACE				
$\overline{\text{CMDVCC}}$	8	I	Figure 18	Command V_{CC} (Negative Assertion). Logic-low on this pin causes the LDO regulator to ramp the V_{CC} supply to the card and initiates a card activation sequence, only when a card is present.
5V/$\overline{\text{3V}}$	9	I	Figure 18	5V/3V/1.8V Card Selection. Logic-high selects 5V for V_{CC} and card interface. Logic-low selects 3V operation. Logic going from high to low within ±400ns of $\overline{\text{CMDVCC}}$ falling selects 1.8V. When the device is to be used with a single card voltage (3V or 5V only), this pin should be connected to either GND or V_{DD}. However, it includes a high-impedance pullup resistor to default this pin high (selection of 5V card) when not connected. Do not change the level of this pin when $\overline{\text{CMDVCC}}$ is low.
CLKDIV	6	I	Figure 20	Sets the Divide Ratio from the XTAL Oscillator (or External Clock Input) to Card Clock. This is a multilevel input that uses a ratio of the V_{DD} voltage to select the clock divider as shown: CLKDIV — CLOCK RATE GND — XTALIN/4 V_{DD}/3 — XTALIN V_{DD} x 2/3 — XTALIN/8 V_{DD} — XTALIN/2 **Note:** This input has no internal pullup or pulldown so it must not be left unconnected.
$\overline{\text{OFF}}$	20	O	Figure 12	Active-Low Interrupt Signal to the Processor. Active-low multifunction indicating fault conditions, device readiness, and card presence. Open-drain output configuration. It includes an internal 20kΩ pullup to V_{DD}.

NAME	PIN	TYPE	EQUIVALENT CIRCUIT FIGURE #	DESCRIPTION
RSTIN	1	I	Figure 18	Reset Input. Within a card session, this signal is the reset command to the card. Outside a card session, this signal is used to place the device in power-down.
C8UC	2	IO	Figure 17	System Controller Data C8 to/from the Card. Includes an 11kΩ pullup resistor to $V_{DD.}$
I/OUC	3	IO	Figure 17	System Controller Data I/O to/from the Card. Includes an 11kΩ pullup resistor to $V_{DD.}$
C4UC	5	IO	Figure 17	System Controller Data C4 to/from the Card. Includes an 11kΩ pullup resistor to $V_{DD.}$
MISCELLANEOUS INPUTS AND OUTPUTS				
XTALIN/ CLKIN	10	I	Figure 19	Crystal Oscillator Input. This pin can either be connected to crystal or driven as a source for the card clock.
XTALOUT	11	O	Figure 19	Crystal Oscillator Output. Connected to crystal. This pin can be left open if XTALIN is being used as external clock input.
POWER SUPPLY AND GROUND				
V_{DD}	7	PSO	Figure 13	System Interface Supply Voltage and Supply Voltage for Internal Circuitry
V_{PC}	4	PSO	Figure 13	LDO Regulator Power Supply Source

2 Electrical Specifications

This section provides the following:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Smart Card Interface Requirements
- Digital Signals Characteristics
- DC Characteristics
- Voltage Fault-Detection Circuits

2.1 Absolute Maximum Ratings

Table 2 lists the maximum operating conditions for the 73S8014BN. Permanent device damage can occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability. The smart card interface pins are protected against short circuits to V_{CC}, ground, and each other.

Table 2: Absolute Maximum Device Ratings

PARAMETER	RATING
Supply Voltage Range, V_{DD}	-0.5V to 4.0V DC
Supply Voltage Range, V_{PC}	-0.5V to 6.0V DC
Input Voltage for Digital Inputs	-0.3V to (V_{DD} + 0.5V) DC
Storage Temperature Range	-60°C to +150°C
Pin Voltage Range (except Card Interface)	-0.3V to (V_{DD} + 0.5V) DC
Pin Voltage Range (Card Interface)	-0.3V to (V_{CC} + 0.5V) DC
ESD Tolerance (Card Interface Pins)*	±6kV
ESD Tolerance (Other Pins)	±2kV

**ESD testing on smart card pins is Human Body Model (HBM) condition, three pulses, each polarity referenced to ground.*

Note: Smart card pins are protected against shorts between any combinations of smart card pins.

2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 3.

Table 3: Recommended Operating Conditions

PARAMETER	RATING
Supply Voltage Range, V_{DD}	2.7V to 3.6V DC
Supply Voltage Range, V_{PC}	4.75V to 5.5V DC
Ambient Operating Temperature Range	-40°C to +85°C
Input Voltage for Digital Inputs	0 to (V_{DD} + 0.3V)

2.3 Smart Card Interface Requirements

Table 4 lists the 73S8014BN smart card interface requirements.

Table 4: DC Smart Card Interface Requirements

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CARD POWER SUPPLY (V_{CC}) REGULATOR (General conditions: 4.75V < V_{PC} < 5.5V, 2.7V < V_{DD} < 5.5V; -40°C < T_A < +85°C, unless otherwise noted.) (NDS conditions: 4.85V < V_{PC} < 5.5V, unless otherwise noted.)						
Card Supply Voltage Including Ripple and Noise	V_{CC}	Inactive mode	-0.1		+0.1	V
		Inactive mode, I_{CC} = 1mA	-0.1		+0.4	
		Active mode; I_{CC} < 65mA; 5V	4.65		5.25	
		Active mode; I_{CC} < 65mA; 5V, NDS condition	4.75		5.25	
		Active mode; I_{CC} < 65mA; 3V	2.85		3.15	
		Active mode; single pulse of 100mA for 2μs; 5V, fixed load = 25mA (Note 1)	4.6		5.25	
		Active mode; I_{CC} < 40mA; 1.8V	1.68		1.92	
		Active mode; single pulse of 100mA for 2μs; 3V, fixed load = 25mA (Note 1)	2.76		3.15	
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ < 200mA, t < 400ns; 5V (Note 1)	4.6		5.25	
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t < 400ns; 5V, NDS condition (Note 1)	4.65		5.25	
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t < 400ns; 3V (Note 1)	2.7		3.15	
		Active mode; current pulses of 20nAs with peak $\|I_{CC}\|$ <100mA, t < 400ns; 1.8V (Note 1)	1.62		1.92	
V_{CC} Ripple	V_{CCRIP}	f_{RIPPLE} = 20kHz – 200MHz (Note 1)			350	mV
Card Supply Output Current	I_{CCMAX}	Static load current, V_{CC} > 4.6V or 2.7V as selected			65	mA
		Static load current, V_{CC}>1.65			40	
I_{CC} Fault Current	I_{CCF}	V_{CC} = 3V or 5V	70		145	mA
		V_{CC} = 1.8V	50		110	mA
V_{CC} Slew Rate, Rise	V_{SR}	C_F = 1.0μF on V_{CC}	0.06	0.150	0.30	V/μs
V_{CC} Slew Rate, Fall	V_{SF}	C_F = 1.0μF on V_{CC}	0.075	0.150	0.60	V/μs
External Filter Cap (V_{CC} to GND)	C_{FNDS}	NDS applications, C_F should be ceramic with low ESR (< 100mΩ) (Note 1)	0.5	1.0	1.5	μF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERFACE REQUIREMENTS **DATA SIGNALS: I/O, C4, C8** **HOST INTERFACES: I/OUC, C4UC, C8UC** (I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC, C4UC, and C8UC.)						
Output Level High (I/OUC, C4UC, C8UC)	V_{OH}	I_{OH} = -40µA	0.9 x V_{DD}		V_{DD} + 0.1	V
		I_{OH} = 0mA	0.75 x V_{DD}		V_{DD} + 0.1	
Output Level High (I/O, C4, C8)		I_{OH} = -40µA (V_{CC} = 3V/5V), -20µA (V_{CC} = 1.8V)	0.9 x V_{CC}		V_{CC} + 0.1	
		I_{OL} = 1mA	0.75 V_{CC}		V_{CC}+0.1	
Output Level Low (I/OUC, C4UC, C8UC)	V_{OL}	I_{OL} = 1mA			0.15 x V_{DD}	V
Output Level Low (I/O, C4, C8)					0.15 x V_{CC}	
Input Level High (I/OUC, C4UC, C8UC)	V_{IH}		0.6 x V_{DD}		V_{DD} + 0.30	V
Input Level High (I/O, C4, C8)			0.6 x V_{CC}		V_{CC} + 0.30	
Input Level Low (I/OUC, C4UC, C8UC)	V_{IL}		-0.15		0.20 x V_{DD}	V
Input Level Low (I/O, C4, C8)		I_{OL} = 0mA	-0.15		0.20 x V_{CC}	
Output Voltage When Outside of Session	V_{INACT}	I_{OL} = 1mA			0.1	V
		V_{IH} = V_{CC}			0.3	
Input Leakage	I_{LEAK}	V_{IL} = 0V			10	µA
Input Current Low	I_{IL}	For output low, shorted to V_{CC} through 33Ω			0.65	mA
Short-Circuit Output Current	I_{SHORTL}	For output high, shorted to ground through 33Ω			15	mA
Short-Circuit Output Current	I_{SHORTH}	C_L = 80pF, 10% to 90%			15	mA
Output Rise Time, Fall Times	t_R, t_F				100	ns
Input Rise, Fall Times	t_{IR}, t_{IF}	Output stable for > 400ns (Note 1)			1	µs
Internal Pullup Resistor	R_{PU}		8	11	15	kΩ
Maximum Data Rate	FD_{MAX}	Edge from master to slave, measured at 50%			1	MHz
Delay, I/O to I/OUC, I/OUC to I/O, C4 to C4UC, C4UC to C4, C8 to C8UC, C8UC to C8 (Respectively Falling Edge to Falling Edge and Rising Edge to Rising Edge)	t_{FDIO}		60	100	200	ns
	t_{RDIO}			15		
Input Capacitance	C_{IN}	(Note 1)			10	pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET AND CLOCK FOR CARD INTERFACE: RST, CLK						
Output Level High	V_{OH}	I_{OH} =-200μA	0.9 x V_{CC}		V_{CC}	V
Output Level Low	V_{OL}	I_{OL}=200μA	0		0.15 x V_{CC}	V
Output Voltage When Outside of Session	V_{INACT}	I_{OL} = 0mA			0.1	V
		I_{OL} = 1mA			0.3	
Output Current Limit, RST	I_{RST_LIM}				30	mA
Output Current Limit, CLK	I_{CLK_LIM}				70	mA
Output Rise Time, Fall Time	t_R, t_F	C_L = 35pF for CLK, 10% to 90%			8	ns
		C_L = 200pF for RST, 10% to 90%			100	
Duty Cycle for CLK	δ	C_L =35pF, f_{CLK} ≤ 20MHz	45		55	%

Note 1: Guaranteed by design; not production tested.

2.4 Digital Signals Characteristics

Table 5 lists the 73S8014BN digital signals characteristics.

Table 5: Digital Signals Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input High Voltage	V_{IH}		1.8		V_{DD} + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -1mA	V_{DD} - 0.45			V
Pullup Resistor, $\overline{OFF}$	R_{OUT}		13.5	20	26.5	kΩ
Input Leakage Current	$\|I_{IL1}\|$	V_{GND} < V_{IN} < V_{DD}	-5		+5	μA
Input Level, CLKDIV	V_{INCD1}	Level Range 1	-0.3		+0.400	V
	V_{INCD2}	Level Range 2	0.26 x V_{DD}		0.40 x V_{DD}	
	V_{INCD3}	Level Range 3	0.6 x V_{DD}		0.80 x V_{DD}	
	V_{INCD4}	Level Range 4	V_{DD} - 0.400		V_{DD} + 0.3	
Input Low Voltage, XTALIN	V_{ILXTAL}		-0.3		0.3 x V_{DD}	V
Input High Voltage, XTALIN	V_{IHXTAL}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Current, XTALIN	I_{ILXTAL}	V_{GND} < V_{IN} < V_{DD}	-30		+30	μA
Max Frequency Oscillator or External Clock	f_{MAX}				27	MHz
External Input Duty-Cycle Limit	δin	t_R/t_F < 10% f_{IN}, 45% < δ_{CLK} < 55% (Note 1)	48		52	%

Note 1: Guaranteed by design; not production tested.

2.5 DC Characteristics

Table 6 lists the 73S8014BN DC characteristics.

Table 6: DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Current	I_{DD}	V_{DD} = 2.7V to 3.6V		2.0	4	mA
V_{DD} Supply Current	I_{PD}	Power-down		1	5	µA
V_{PC} Supply Current	I_{PC}	V_{CC} on, I_{CC} = 0mA, CLK = 2.0MHz, external load < 10pF, I/O, C4, C8 = high		1	2	mA
V_{PC} Supply Current	I_{PCPD}	$\overline{CMDVCC}$ = 1		1	2	µA

2.6 Voltage Fault-Detection Circuits

Table 7 lists the 73S8014BN voltage and current fault-detection circuits.

Table 7: Voltage and Current Fault-Detection Circuits

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Fault	V_{DDF}	V_{DD} falling	2.15		2.4	V
I_{CC} Fault Current	I_{CCF}	V_{CC} = 3V or 5V	70		145	mA
		V_{CC} = 1.8V	50		110	
V_{CC} Fault (V_{CC} Voltage Supervisor Threshold)	V_{CCF}	V_{CC} = 5V			4.6	V
		V_{CC} = 3V			2.7	
		V_{CC} = 1.8V (Note 1)			1.65	

Note 1: Guaranteed by design; not production tested.

3 Applications Information

This section provides general usage information for the design and implementation of the 73S8014BN.

3.1 Example 73S8014BN Schematics

Figure 3 shows a typical application schematic for the implementation of the 73S8014BN.

Note that minor changes can occur to the reference material from time to time and the reader is encouraged to contact Maxim for the latest information.

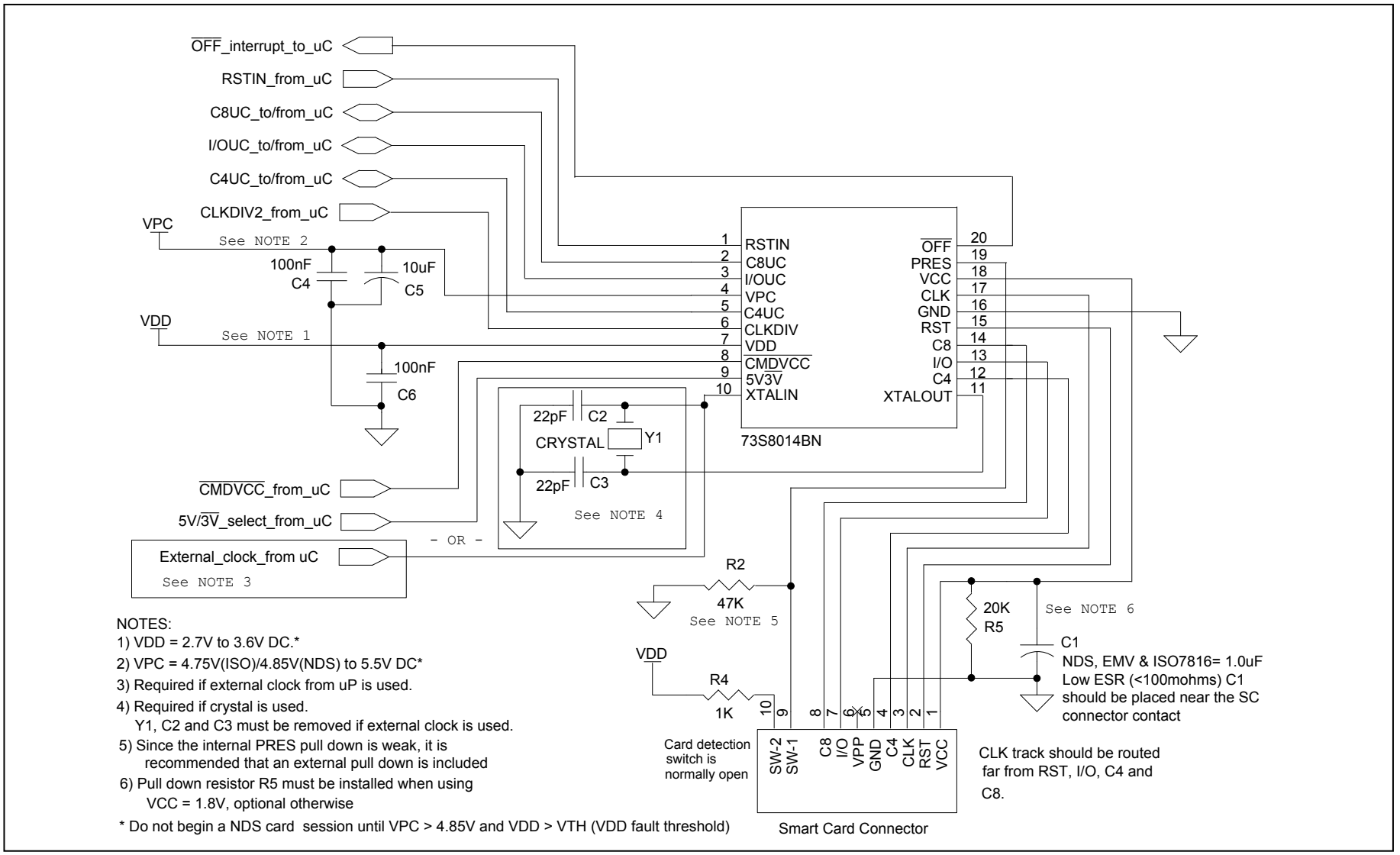


Figure 3: 73S8014BN—Typical Application Schematic

3.2 System Controller Interface

Three digital inputs allow direct control of the card interface by the host. The 73S8014BN is controlled as follows:

- Pin $\overline{\text{CMDVCC}}$: When asserted low, starts an activation sequence. When deasserted high, starts deactivation sequence.
- Pin RSTIN: Controls the card RST signal (when enabled by the sequencer) while the card is activated and the power-down mode when the card is not activated.
- Pin 5V/$\overline{3V}$: Defines the card V_{DD} voltage according to Table 8.

Table 8: V_{CC} Voltage Logic Table

CONTROL PINS		V_{CC} VOLTAGE (V)	NOTES
$\overline{\text{CMDVCC}}$	5V/$\overline{3V}$		
1	x	0	Off
↓	1	5	5V/$\overline{3V}$ must be stable for at least 1µs before assertion of $\overline{\text{CMDVCC}}$ and held high until deassertion of $\overline{\text{CMDVCC}}$.
↓	0	3	5V/$\overline{3V}$ must be stable for at least 1µs before assertion of $\overline{\text{CMDVCC}}$ and held low until deassertion of $\overline{\text{CMDVCC}}$.
↓	↓	1.8	Must be asserted low within 400ns of each other to generate 1.8V and held low until assertion of $\overline{\text{CMDVCC}}$.

The $\overline{\text{OFF}}$ digital output reports status back to the host. See the Fault Detection and $\overline{\text{OFF}}$ section for details on the operation of the $\overline{\text{OFF}}$ output.

Note: 5V/$\overline{3V}$ should not change during a card session. Doing so does not change the voltage on V_{CC} during that session, but if it is changed, the 5V/$\overline{3V}$ must be taken high outside the current card session and before beginning the next card session. Otherwise, the next card session may not power up to the selected V_{CC} voltage.

3.3 Power-Down Mode

The 73S8014BN includes a power-down mode to greatly reduce the power consumption on the V_{DD} and V_{PC} supplies when the smart card interface is deactivated. The power-down mode shuts down the crystal oscillator and other internal circuits to save power. When the power-down mode is released, the oscillator is restarted. It requires some time to start up and stabilize. During this time, the $\overline{\text{OFF}}$ output goes low (if a card is inserted) and is held low until the oscillator stabilizes, and then the $\overline{\text{OFF}}$ output goes high to indicate that the device is ready to activate the card.

The power-down mode is initiated when RSTIN, $\overline{\text{CMDVCC}}$, and 5V/$\overline{3V}$ are all logic-high for more than 2ms. The power-down mode is released immediately by bringing RSTIN low. This action forces the $\overline{\text{OFF}}$ output low for approximately 5ms to 7ms to allow the oscillator to start up and stabilize. This action informs the host that the 73S8014BN is busy and should not be activated while the $\overline{\text{OFF}}$ output is low. This ensures a proper activation sequence after coming out of power-down.

The card-detection logic on the PRES input remains active in power-down mode. The card status is reported on $\overline{\text{OFF}}$.

Note: The $\overline{\text{CMDVCC}}$ and 5V/$\overline{3V}$ inputs have no effect when exiting power-down. Bringing RSTIN low is the only way to exit power-down.

Figure 4 shows the power-down mode control timing with PRES debounce. See Section 3.9 for a full description of the PRES debounce behavior.

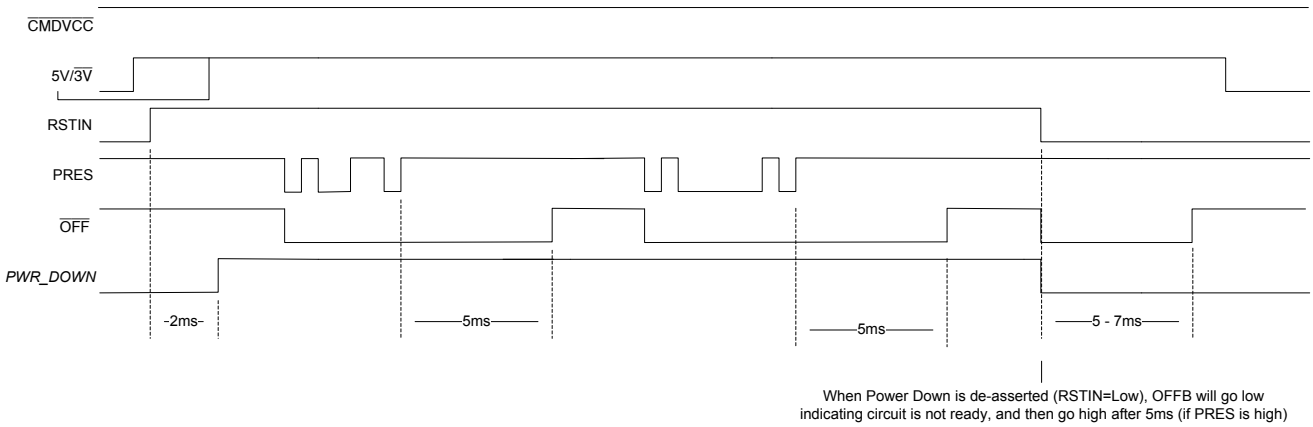


Figure 4: Power-Down Mode and PRES Debounce

3.4 Power Supply and Voltage Supervision

The 73S8014BN smart card interface IC incorporates a low dropout (LDO) voltage regulator for V_{CC}. The voltage output is controlled by the digital input 5V/$\overline{3V}$ of the 73S8014BN. This regulator can provide 1.8V, 3V, or 5V card voltage from the power supply applied on the V_{PC} pin. The voltage regulator can provide a current of at least 65mA on V_{CC} for both 3V and 5V or 40mA for 1.8V that complies with EMV 4.0 and NDS specifications. An overcurrent supervisor triggers a fault if the current on V_{CC} exceeds the threshold at the given V_{CC} voltage.

Digital circuitry is powered by the power supply applied on the V_{DD} pin. V_{DD} is sourced by 2.7 to 3.6V so the system controller must operate with this supply level. A card deactivation sequence is forced upon fault of any voltage or overcurrent supervisor. One supervisor monitors the V_{CC} output voltage at the selected V_{CC} voltage level. The maximum V_{CC} voltage-fault threshold does not exceed the minimum V_{CC} voltage spec according to ISO 7816. See V_{CCF} specification for the V_{CC} voltage thresholds. Another voltage supervisor constantly monitors the V_{DD} voltage. This fixed threshold supervisor is used to initialize the ISO 7816-3 sequencer at power-on and to deactivate the card at power-off or upon fault. The voltage threshold of the V_{DD} voltage supervisor is internally set to 2.26V typical (V_{DDF}). If an adjustable V_{DD} threshold (>2.26V) is required on the device, then the 73S8024RN should be considered or an external circuit configured for the desired V_{DD} threshold should be added to the circuit to control either the $\overline{CMDVCC}$ or PRES input for an immediate V_{CC} deactivation.

Note: Since the V_{DD} and the V_{PC} power supplies are separate, special care must be taken to ensure that the V_{PC} voltage is greater than 4.85V before beginning activating the card. In addition, V_{DD} must be greater than the threshold for V_{DD} fault before card activation. When turning off power to the V_{DD} and the V_{PC} power supplies, the card should be deactivated before shutdown or the V_{PC} power supply must remain higher than 4.85V when the V_{DD} fault is detected and the emergency deactivation sequence is completed.

3.5 Card Power Supply

The 73S8014BN smart card interface IC incorporates an LDO voltage regulator for V_{CC}. The voltage output is controlled by the digital inputs 5V/$\overline{3V}$ and $\overline{CMDVCC}$ of the 73S8014BN. This regulator can provide 1.8V, 3V, or 5V card voltage from the power supply applied on the V_{PC} pin. The voltage regulator can provide a current of at least 65mA on V_{CC} for both 3V and 5V and 40mA for 1.8V that complies with EMV 4.2 and NDS specifications.

Note: When using V_{CC} = 1.8V, a minimum load is required on V_{CC} to ensure proper output regulator stability. A 20kΩ resistor is required between V_{CC} and GND to meet this minimum load requirement. If V_{CC} = 1.8V is never used in a given application, the resistor is not required.

3.6 On-Chip Oscillator and Card Clock

The 73S8014BN device has an on-chip oscillator that can generate the smart card clock using an external crystal (connected between XTALIN and XTALOUT) to set the oscillator frequency. When the clock signal is available from another source it can be connected to XTALIN, and XTALOUT should be left unconnected.

For this device the card clock frequency can be chosen among four different division rates, defined by multiple-state input CLKDIV, as per the following table:

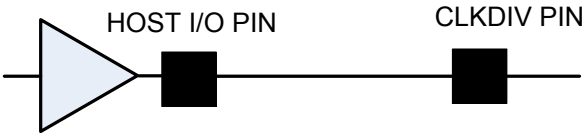
CLKDIV	CLK	MAX XTALIN/CLKIN (MHz)
GND	1/4 XTALIN	27
V_{DD}/3	XTALIN	20
V_{DD} x 2/3	1/8 XTALIN	27
V_{DD}	1/2 XTALIN	27

Note: The clock-divider ratio must be configured prior to activation and must not change during the card session.

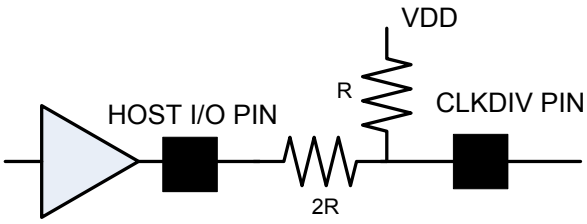
Note: Special care should be taken when configuring the CLKDIV input when using the power-down mode. The CLKDIV input does not contain an internal pullup or pulldown so it must not be allowed to be left unconnected. In addition, the CLKDIV input should be set in such a manner as to set the voltage level to GND or V_{DD} to keep the current consumption to an absolute minimum.

There are numerous simple methods available to control CLKDIV as shown in Figure 5.

1. Selecting between Divide by 2 (I/O HIGH) or divide by 4 (I/O LOW)



2. Selecting between Divide by 2 (IO HIGH) or divide by 8 (IO LOW)



3. Selecting any of the four Divide ratios

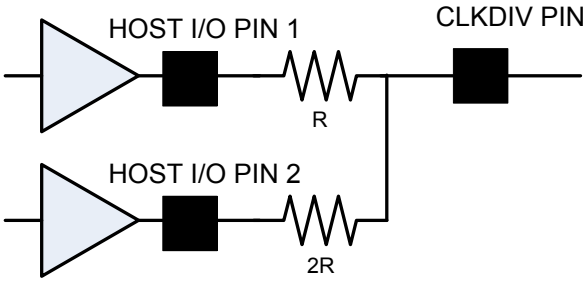


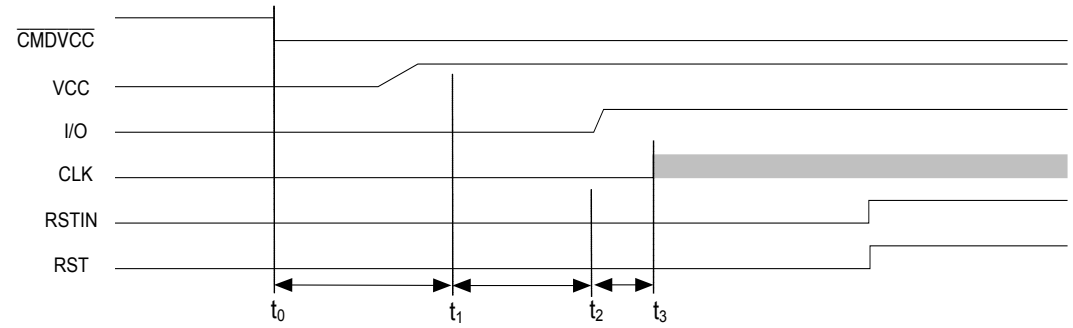
Figure 5: CLKDIV Usage

3.7 Activation Sequence

The 73S8014BN smart card interface IC has an internal 1ms delay on the application of V_{DD} where $V_{DD} > V_{DDF}$. No activation is allowed during this 1ms period. The $\overline{\text{CMDVCC}}$ (edge triggered) signal must then be set low to activate the card. To initiate activation, the card must be present and there can be no V_{DD} fault.

The following steps show the activation sequence and the timing of the card control signals when the system controller sets $\overline{\text{CMDVCC}}$ low while the RSTIN is low:

- $\overline{\text{CMDVCC}}$ is set low at t_0.
- V_{CC} rises to the selected level and then the internal V_{CC} control circuit checks the presence of V_{CC} at the end of t_1. In normal operation, the voltage V_{CC} to the card becomes valid before t_1. If V_{CC} is not valid at t_1, $\overline{\text{OFF}}$ goes low to report a fault to the system controller, and V_{CC} to the card is shut off.
- Turn I/O to reception mode at t_2.
- CLK is applied to the card at t_3.
- RST is a copy of RSTIN after t_3.

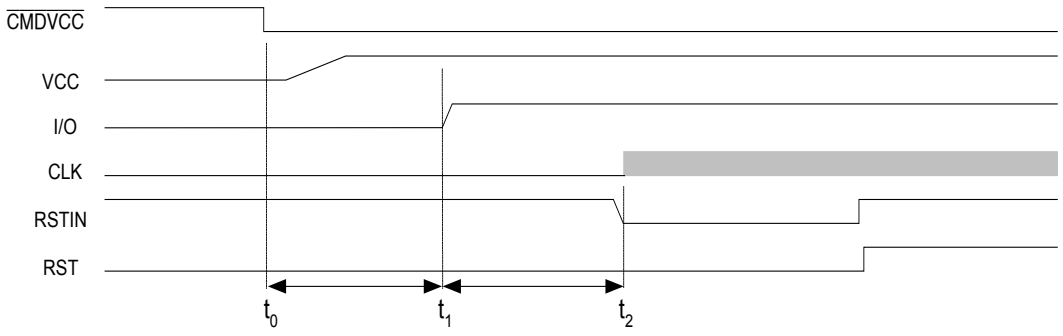


t_1 = 0.2ms (timing by 1.5MHz internal oscillator)
t_2 = 1.5µs, I/O goes to reception state
t_3 = > 0.5µs, CLK starts, RST to become the copy of RSTIN

Figure 6: Activation Sequence—RSTIN Low When $\overline{\text{CMDVCC}}$ Goes Low

The startup of the CLK output can be delayed in the activation sequence by setting the RSTIN input high before beginning activation by bringing $\overline{\text{CMDVCC}}$ low. The CLK output is delayed until RSTIN is taken low. Special care must be taken when performing this type of activation. The power-down mode is initiated by setting the RSTIN and 5V/$\overline{\text{3V}}$ inputs high while $\overline{\text{CMDVCC}}$ is high (outside a card session). If this state is held for more than 2ms, the power mode is initiated. As a result, to use this activation mode, the $\overline{\text{CMDVCC}}$ falling edge must occur within 1ms of the RSTIN input being set high. The following steps show the activation sequence and the timing of the card control signals when the system controller pulls the $\overline{\text{CMDVCC}}$ low while the RSTIN is high:

- $\overline{\text{CMDVCC}}$ is set low at t_0.
- V_{CC} rises to the selected level and then the internal V_{CC} control circuit checks the presence of V_{CC} at the end of t_1. In normal operation, the voltage V_{CC} to the card becomes valid before t_1. If V_{CC} is not valid at t_1, $\overline{\text{OFF}}$ goes low to report a fault to the system controller, and V_{CC} to the card is shut off.
- At the fall of RSTIN (under host control) at t_2, CLK is applied to the card.
- RST is a copy of RSTIN after t_2.



t_1 = 0.2 ms (timing by 1.5MHz internal oscillator, I/O goes to reception state)
t_2 = RSTIN goes low and CLK becomes active
t_3 = > 0.5µs, CLK active, RST to become the copy of RSTIN

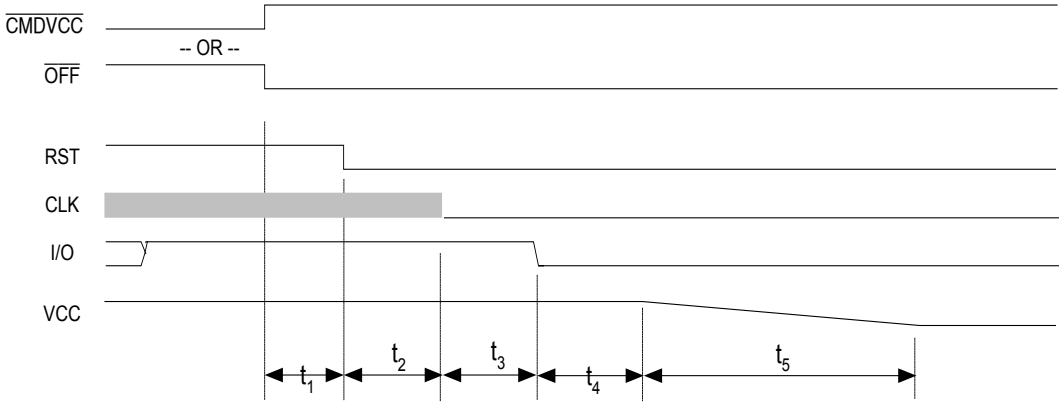
Figure 7: Activation Sequence—RSTIN High When $\overline{\text{CMDVCC}}$ Goes Low

3.8 Deactivation Sequence

Deactivation is initiated either by the system controller by setting the $\overline{\text{CMDVCC}}$ high or automatically in the event of hardware faults. Hardware faults are overcurrent, V_{DD} fault, V_{CC} fault, and card extraction during the session.

The following steps show the deactivation sequence and the timing of the card control signals when the system controller sets the $\overline{\text{CMDVCC}}$ high or $\overline{\text{OFF}}$ goes low due to a fault or card removal:

- RST goes low at the end of t_1.
- CLK is set low at the end of t_2.
- I/O goes low at the end of t_3. Out of reception mode.
- V_{CC} is shut down at the end of time t_4. After a delay t_5 (discharge of the V_{CC} capacitor), V_{CC} is low.



t_1 = > 0.5µs, timing by 1.5MHz internal oscillator
t_2 = > 7.5µs
t_3 = > 0.5µs
t_4 = > 0.5µs
t_5 = depends on V_{CC} filter capacitor
For NDS application, C_F=1µF makes $t_1 + t_2 + t_3 + t_4 + t_5$ < 100µs

Figure 8: Deactivation Sequence

3.9 Fault Detection and $\overline{\text{OFF}}$

There are two different cases that the system controller can monitor the $\overline{\text{OFF}}$ signal: to query regarding the card presence and device readiness outside card sessions, or for fault detection during card sessions. The $\overline{\text{OFF}}$ interrupt output operates as follows:

As long as the card is not activated ($\overline{\text{CMDVCC}}$ is always high), $\overline{\text{OFF}}$ informs the host about the card presence or device readiness. When no card is inserted, the $\overline{\text{OFF}}$ output is low. When a card is inserted, the $\overline{\text{OFF}}$ output is set high after a 5ms debounce period. Upon card removal, there is no debounce on the PRES input as the emergency deactivation must occur as soon as possible to prevent any potential card errors or data corruption. The $\overline{\text{OFF}}$ output goes low immediately upon detection of a logic-low on the PRES input, but the $\overline{\text{OFF}}$ output does not bounce and remains low for at least 5ms.

In addition, when a card is present and the power-down mode is released, the $\overline{\text{OFF}}$ output is taken low for about 5ms to indicate that the device is not ready. This time allows the crystal oscillator to start up and stabilize. When $\overline{\text{CMDVCC}}$ is asserted low (card activation sequence requested from the host), low level on $\overline{\text{OFF}}$ means a fault has been detected (e.g., card removal during card session, voltage fault, or overcurrent fault) that automatically initiates a deactivation sequence.

Figure 9 shows the timing diagram for the signals $\overline{\text{CMDVCC}}$, PRES, and $\overline{\text{OFF}}$ while the card is activated and deactivated:

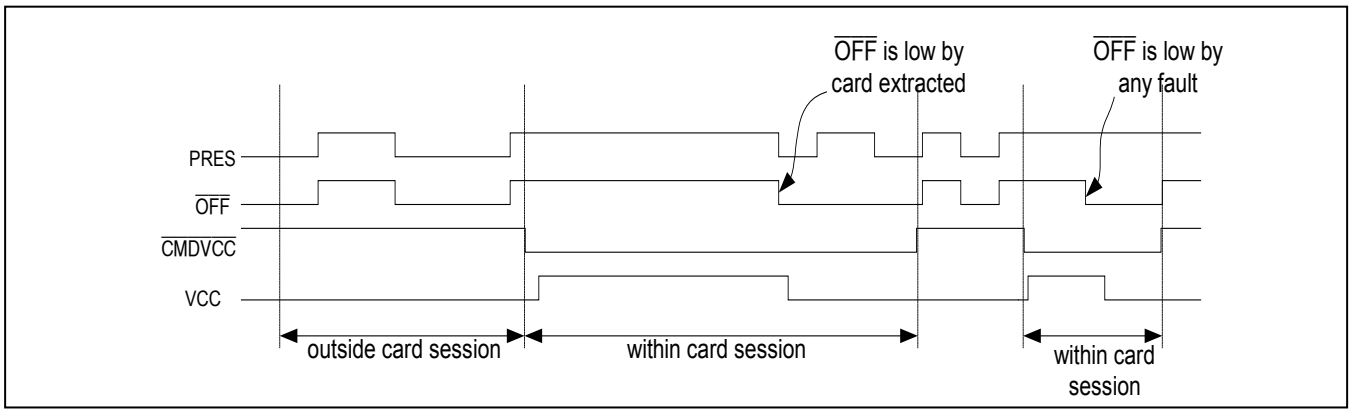


Figure 9: Timing Diagram—Management of the Interrupt Line $\overline{\text{OFF}}$

3.10 I/O, C4, and C8 Circuitry and Timing

The I/O, C4, and C8 are smart card data signals that operate identically, and I/OUC, C4UC, and C8UC are the corresponding microcontroller interface signals. The I/O and I/OUC data signals are described henceforth. The state of the I/O and I/OUC pins are low after power-on reset and goes high when the activation sequencer turns on the I/O reception state. See the Activation Sequence section for details on when the I/O reception is enabled. The state of I/OUC is high after power-on reset.

When the card is activated and the I/O reception state is turned on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected, both I/O lines return to their neutral state.

Note: In certain situations and conditions, the I/O logic can get confused if the host and the card attempt to drive the I/OUC and the I/O signal low at the same time. It should be noted that this is an illegal condition as all card communication is initiated by the host with a command/response protocol. The next host command should not be sent until a valid response has been completely received from the card. However, if this condition should occur, the 73S8014BN could set both I/OUC and I/O as outputs where they are both driven low at the same time. When either side drives their respective signal high, this mode should be released. However, if there is a series resistance between the host and the 73S8014BN, there may not be enough drive to release this mode. If the series resistance is greater than approximately 100Ω, this can cause this mode to become locked for the duration of the card session. If the host detects this condition (I/OUC held low for more than 1 byte time), the card session must be terminated and restarted.

Figure 10 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output. The delay between the I/O signals is shown in Figure 11.

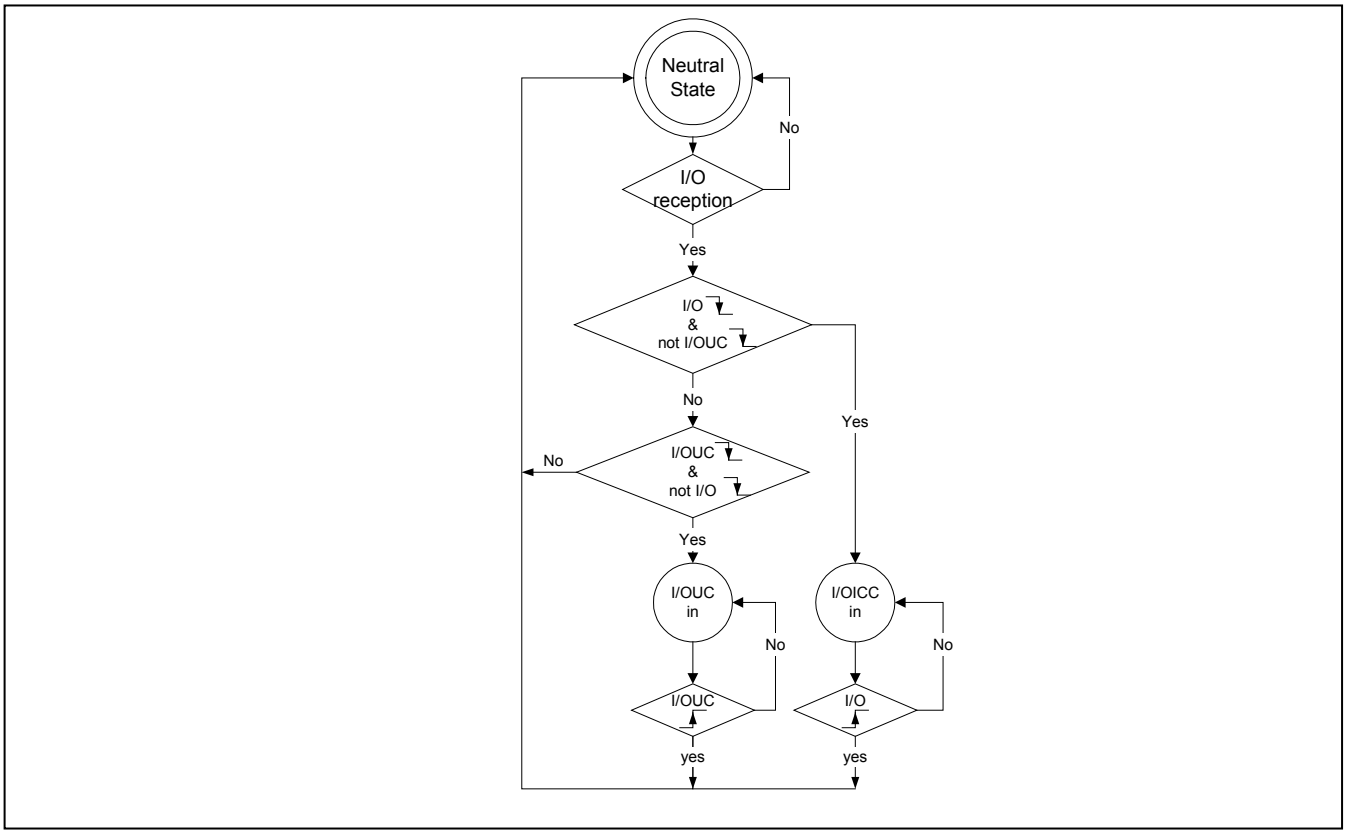


Figure 10: I/O and I/OUC State Diagram

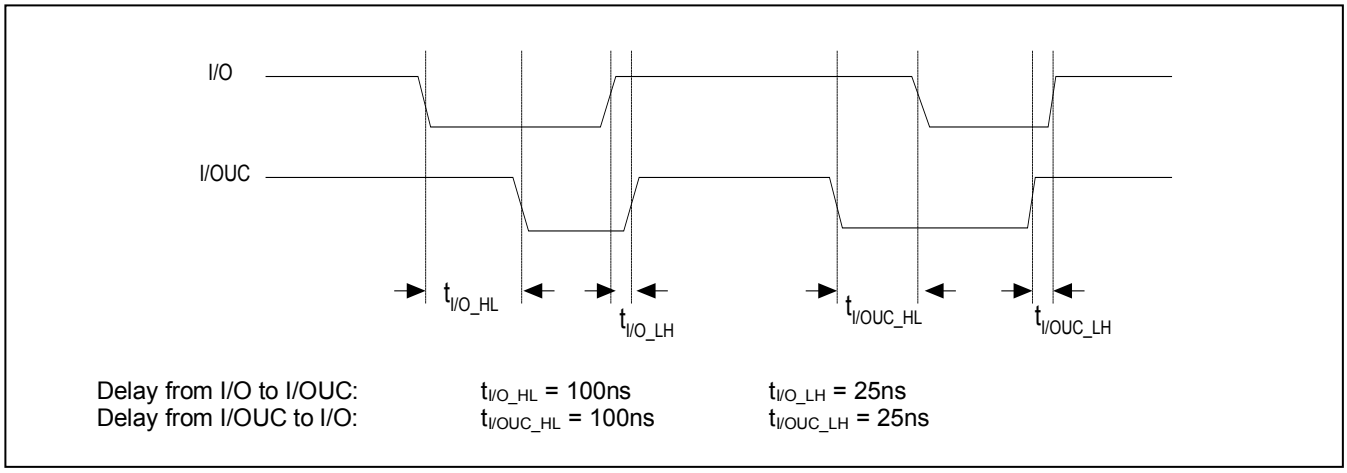


Figure 11: Timing Diagram—I/O to I/OUC Delays

4 Equivalent Circuits

This section provides illustrations of circuits equivalent to those described in the pinout section.

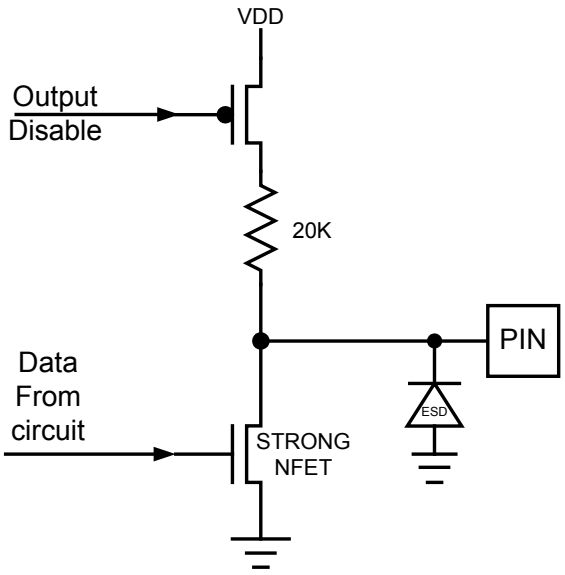


Figure 12: Open-Drain Type—$\overline{OFF}$

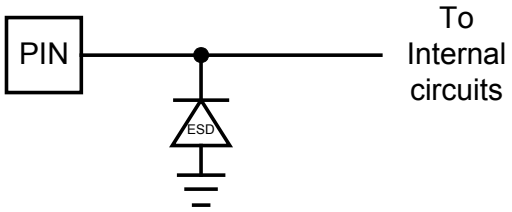


Figure 13: Power Input/Output Circuit—V_{DD}, V_{PC}, V_{CC}

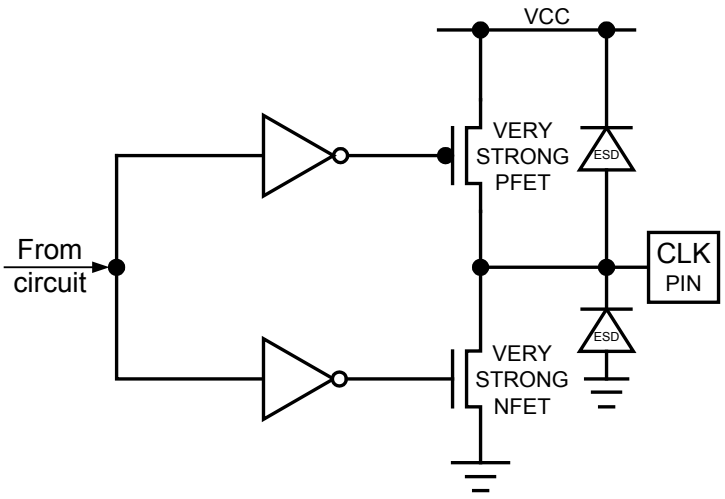


Figure 14: Smart Card CLK Driver Circuit

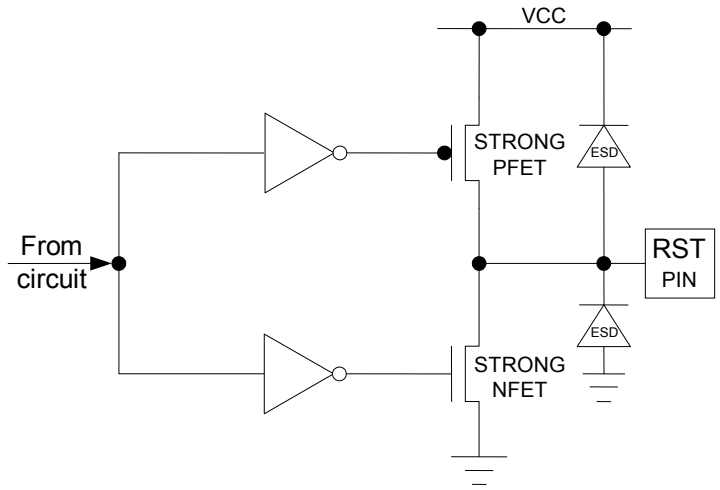


Figure 15: Smart Card RST Driver Circuit

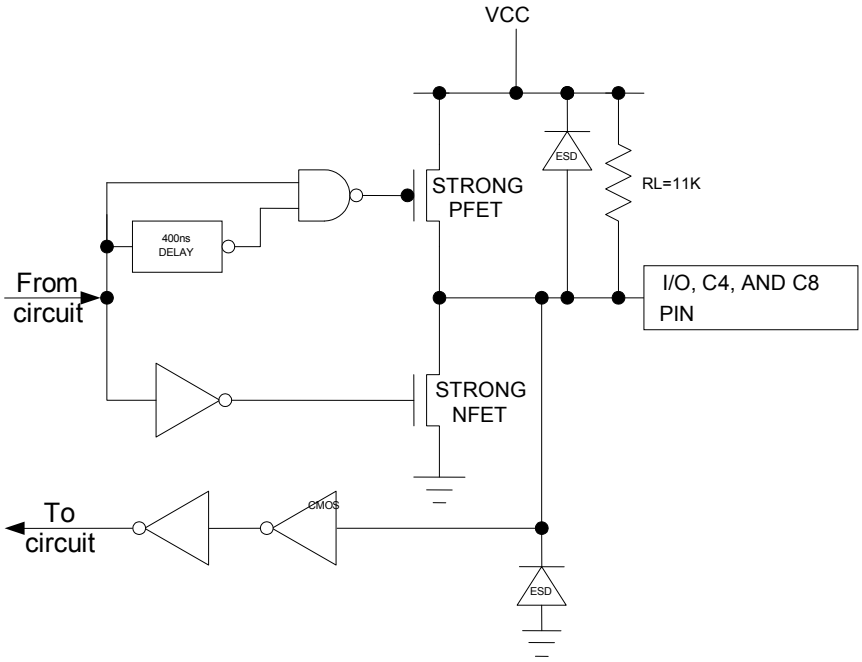


Figure 16: Smart Card I/O, C4, and C8 Interface Circuit

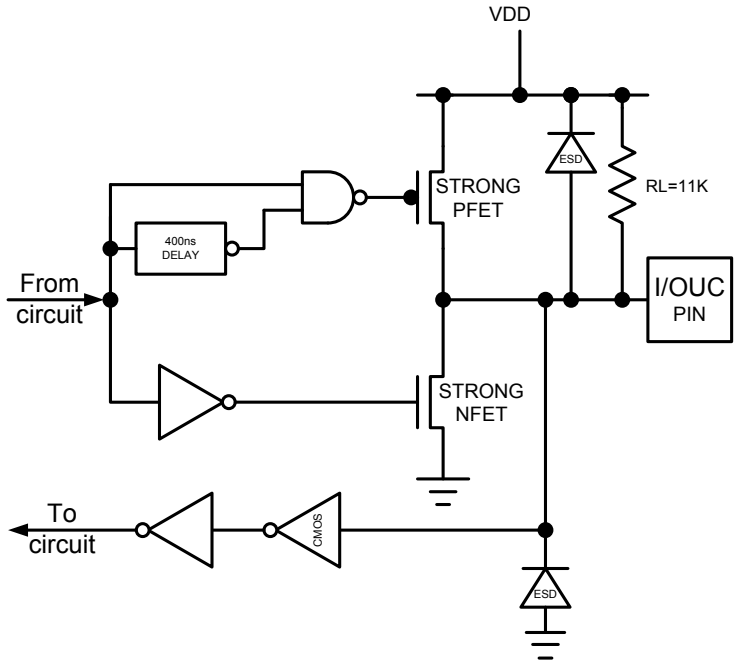
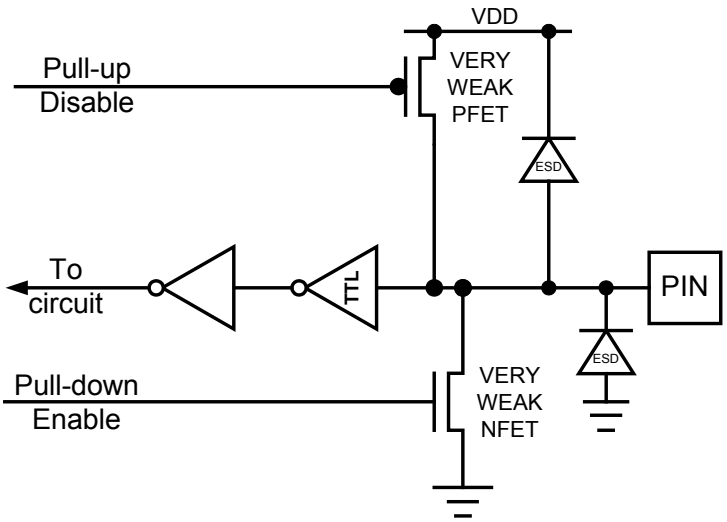


Figure 17: Smart Card I/OUC Interface Circuit



Note: 5V/$\overline{3V}$ has the pullup enabled. PRES has the pulldown enabled. $\overline{CMDVCC}$ and RSTIN have pullup and pulldown disabled.

Figure 18: General Input Circuit

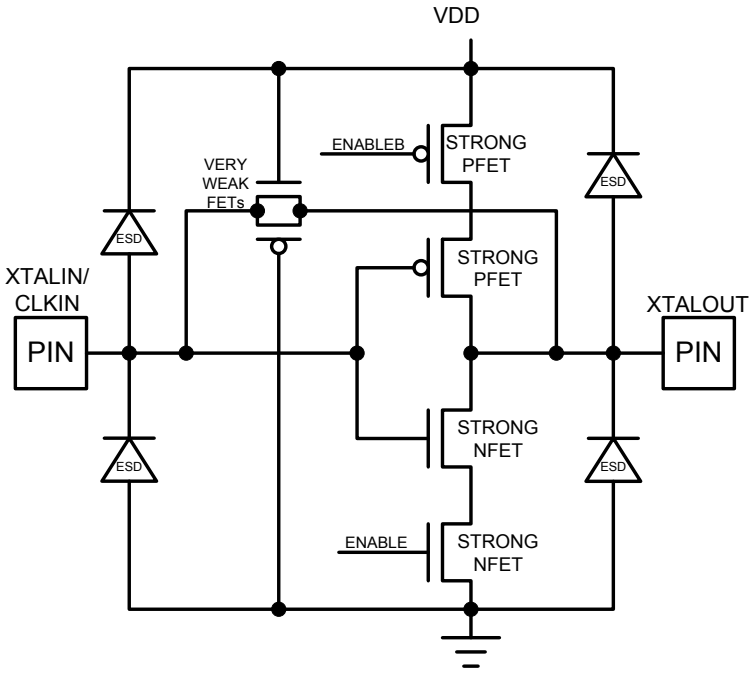


Figure 19: Oscillator Circuit

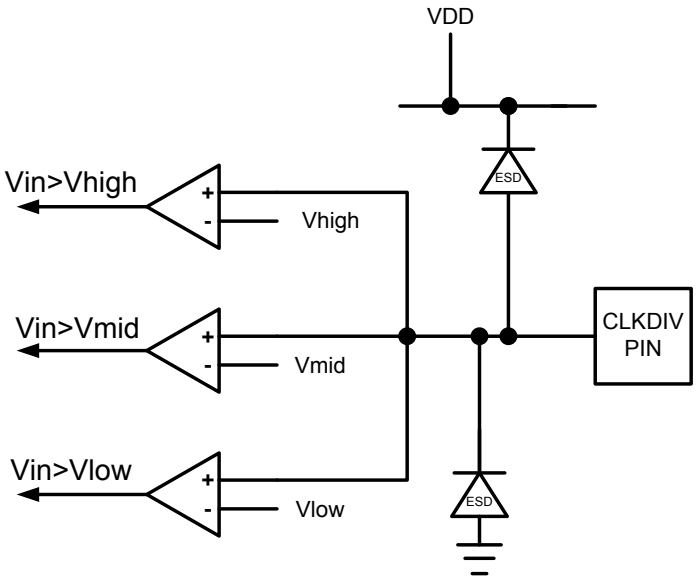


Figure 20: CLKDIV

5 Mechanical Drawing

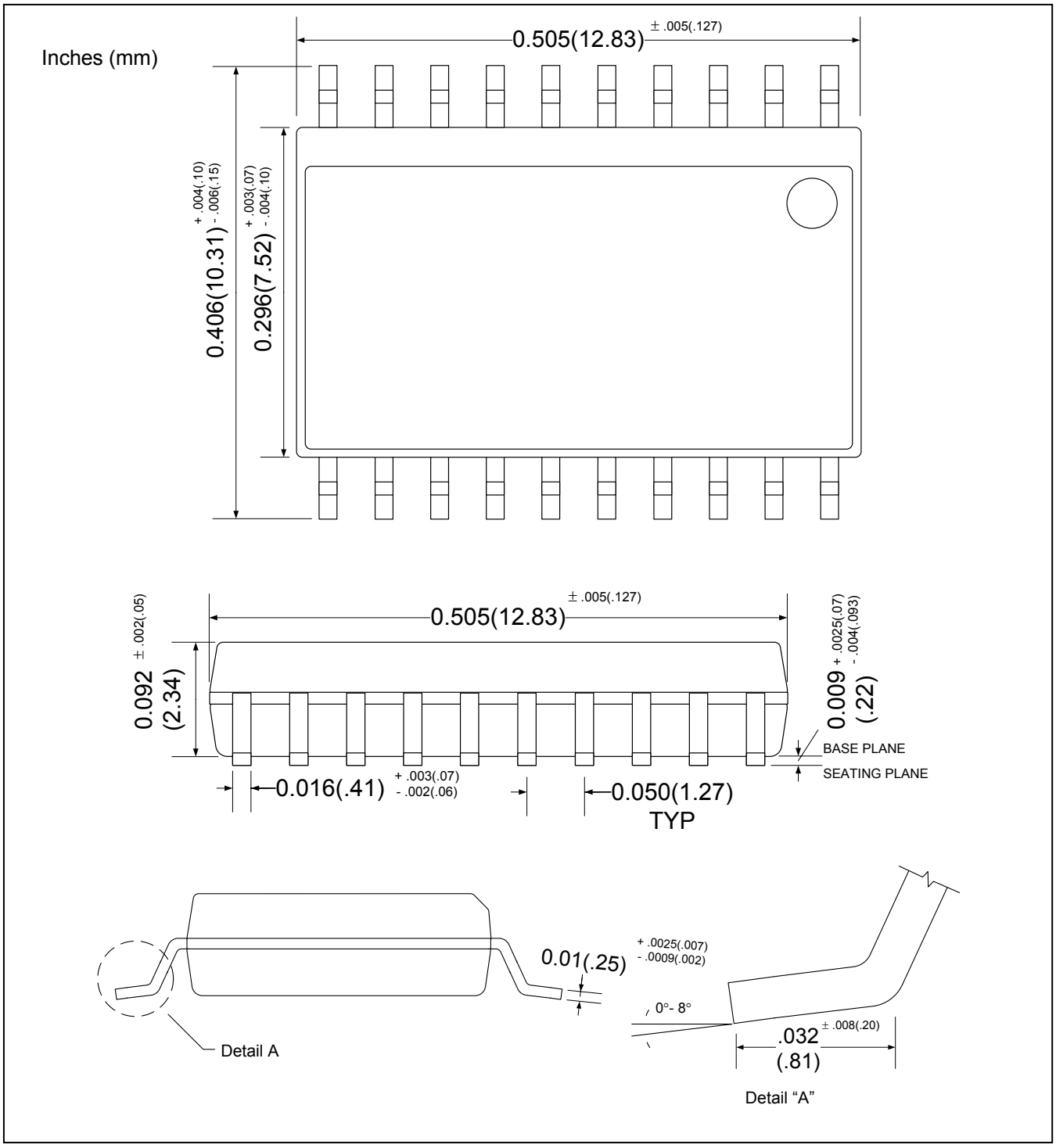


Figure 21: Mechanical Drawing 20-Pin SO Package

6 Ordering Information

Table 9 lists the order numbers and packaging marks used to identify 73S8014BN products.

Table 9: Order Numbers and Packaging Marks

PART	PIN-PACKAGE	TOP MARK
73S8014BN-IL/F	20 SO	73S8014BN
73S8014BN-ILR/F	20 SO	73S8014BN

F = Lead(Pb)-free/RoHS-compliant package.
R = Tape and reel.

7 Contact Information

For more information about Maxim products or to check the availability of the 73S8014BN, contact technical support at **www.maxim-ic.com/support**.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1.0	12/10	Initial release	—
2	12/11	Deleted “Certification Pending” from the NDS logo. Added “designed to provide full electrical compliance with ISO 7816-3, EMV® 4.2, and NDS specifications” to the first sentence. Added “For NDS applications requiring an on-chip adjustable POR, see the Maxim 73S8024RN series of interface ICs.” to the first paragraph.	1
		Provided additional description to Section 3.4.	16

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