

January 1997

### Features

- -15A and -19A, -80V and -100V
- $r_{DS(ON)} = 0.20\Omega$  and  $0.30\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

### Description

The IRF9540, IRF9541, IRF9542, IRF9543, RF1S9540, and RF1S9540SM are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and as drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

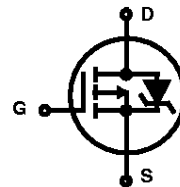
### Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF9540	TO-220AB	IRF9540
IRF9541	TO-220AB	IRF9541
IRF9542	TO-220AB	IRF9542
IRF9543	TO-220AB	IRF9543
RF1S9540	TO-262AA	RF1S9540
RF1S9540SM	TO-263AB	RF1S9540SM

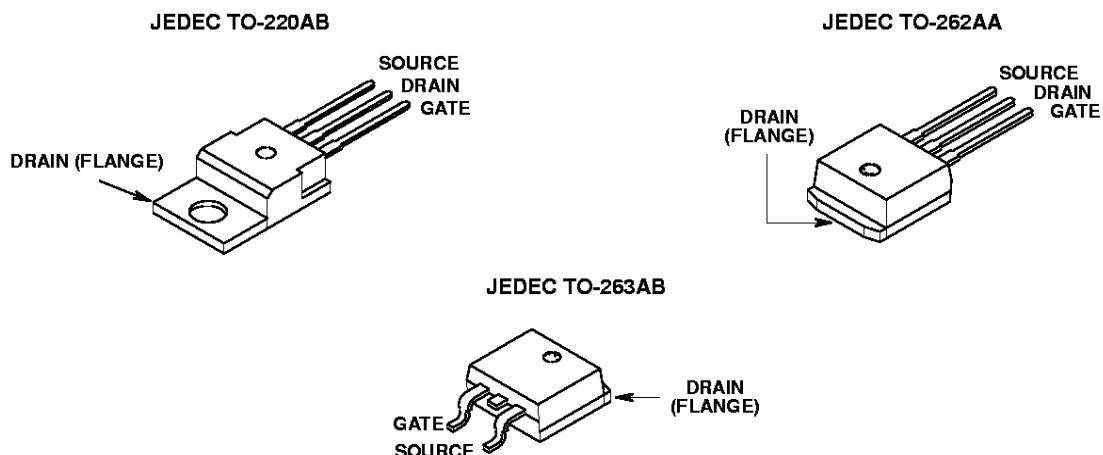
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., RF1S9540SM9A.

Formerly Developmental Type TA17521.

### Symbol



### Packaging



## IRF9540, IRF9541, IRF9542, IRF9543, RF1S9540, RF1S9540SM

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	IRF9540, RF1S9540, RF1S9540SM	IRF9541	IRF9542	IRF9543	UNITS
Drain to Source Breakdown Voltage (Note 1) . . . . . $V_{DS}$	-100	-80	-100	-80	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . . $V_{DGR}$	-100	-80	-100	-80	V
Continuous Drain Current					
$T_C = 25^\circ\text{C}$ . . . . . $I_D$	-19	-19	-15	-15	A
$T_C = 100^\circ\text{C}$ . . . . . $I_D$	-12	-12	-10	-10	A
Pulsed Drain Current (Note 3) . . . . . $I_{DM}$	-76	-76	-60	-60	A
Gate to Source Voltage . . . . . $V_{GS}$	$\pm 20$	$\pm 20$	$\pm 20$	$\pm 20$	V
Maximum Power Dissipation (Figure 1) . . . . . $P_D$	150	150	150	150	W
Linear Derating Factor (Figure 1) . . . . .	1	1	1	1	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4) . . . . . $E_{AS}$	960	960	960	960	mJ
Operating and Storage Temperature . . . . . $T_J, T_{STG}$	-55 to 175	-55 to 175	-55 to 175	-55 to 175	$^\circ\text{C}$
Maximum Lead Temperature for Soldering . . . . . $T_L$ (0.063in (1.6mm) from case for 10s)	300	300	300	300	$^\circ\text{C}$

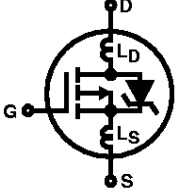
*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

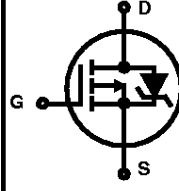
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRF9540, IRF9542, RF1S9540, RF1S9540SM	$BV_{DSS}$	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-100	-	-	V
IRF9541, IRF9543			-80	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-2	-	-4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	-25	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$ $T_C = 125^\circ\text{C}$	-	-	-250	$\mu\text{A}$
On-State Drain Current (Note 2) IRF9540, IRF9541, RF1S9540, RF1S9540SM	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON) \text{ MAX}}, V_{GS} = -10\text{V}$	-19	-	-	A
IRF9542, IRF9543			-15	-	-	A
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
On Resistance (Note 2) IRF9540, IRF9541, RF1S9540, RF1S9540SM	$r_{DS(ON)}$	$I_D = -10\text{A}, V_{GS} = -10\text{V}$	-	0.15	0.20	$\Omega$
IRF9542, IRF9543			-	0.22	0.30	$\Omega$
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON) \text{ MAX}}, I_D = -6\text{A}$	5	7	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = -50\text{V}, I_D \approx 19\text{A}, R_G = 9.1\Omega, R_L = 5\Omega$ (Figure 19) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	20	ns
Rise Time	$t_r$		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	$t_f$		-	28	70	ns

**IRF9540, IRF9541, IRF9542, IRF9543, RF1S9540, RF1S9540SM**

**Electrical Specifications**  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	$L_D$	Measured From the Contact Screw on Tab to the Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) from Package to the Center of Die		-	4.5	-	nH
Internal Source Inductance	$L_S$	Measured From the Source Lead, 6mm (0.25in) From Package to Source Bonding Pad		-	7.5	-	nH
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = -10\text{V}$ , $I_D = -19\text{A}$ , $V_{DS} = 80\text{V Max}$ , $I_{g(REF)} = -1.5\text{mA}$ (See Figure 20 for Test Circuit) Gate Charge is Essentially Independent of Operating Temperature		-	70	90	nC
Gate to Source Charge	$Q_{gs}$			-	14	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$			-	56	-	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = -25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 11)		-	1100	-	pF
Output Capacitance	$C_{OSS}$			-	550	-	pF
Reverse Transfer Capacitance	$C_{RSS}$			-	250	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Typical Socket Mount		-	-	80	$^\circ\text{C/W}$

**Source to Drain Diode Specifications**

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source Current (Body Diode)	$I_{SD}$	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 		-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	$I_{SM}$			-	-	-76	A
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$T_C = 25^\circ\text{C}$ , $I_{SD} = -19\text{A}$ , $V_{GS} = 0\text{V}$		-	-	-1.5	V
Reverse Recovery Time	$t_{rr}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = 19\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	170	-	ns
Reverse Recovery Charge	$Q_{RR}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = 19\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	0.8	-	$\mu\text{C}$

NOTES:

- $T_J = 25^\circ\text{C}$  to  $T_J = 175^\circ\text{C}$ .
- Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 25\text{V}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 4\text{mH}$ ,  $R_G = 25\Omega$ , peak  $I_{AS} = 19\text{A}$ . (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

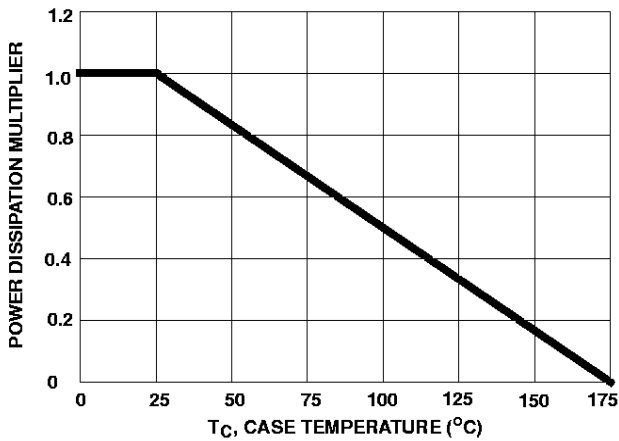


FIGURE 1. NORMALIZED POWER DISSIPATION TEMPERATURE DERATING CURVE

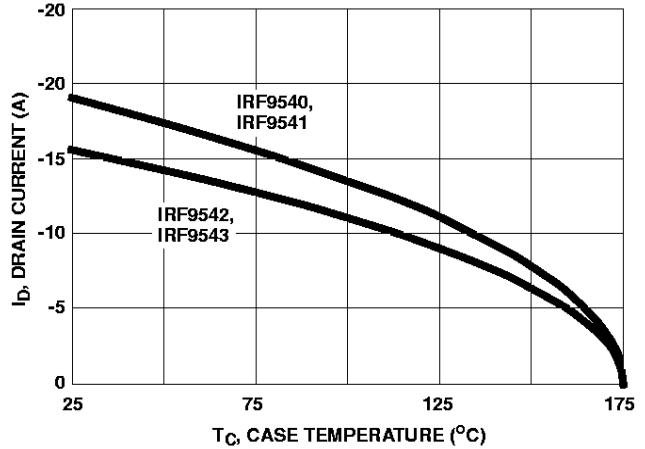


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

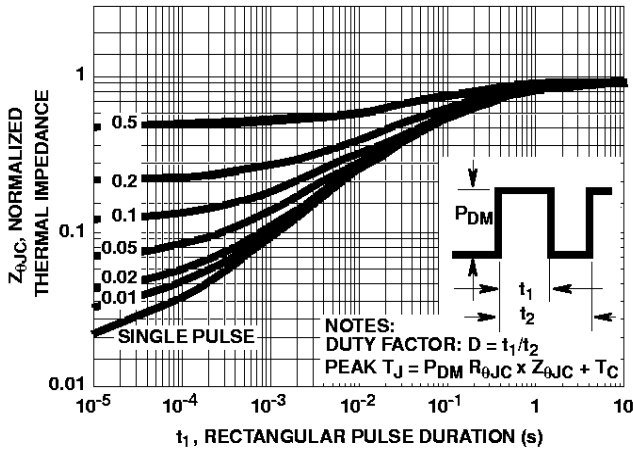


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

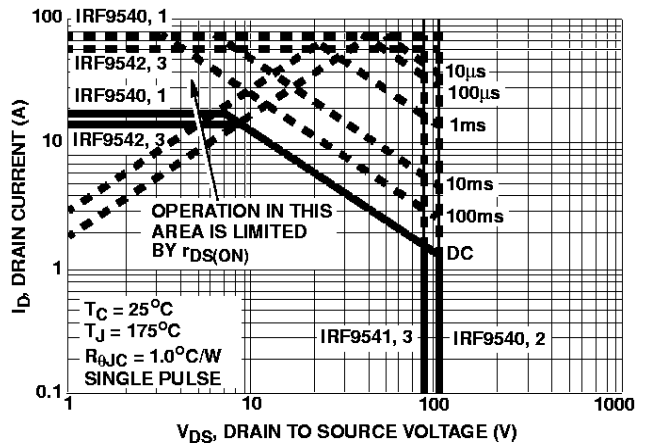


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

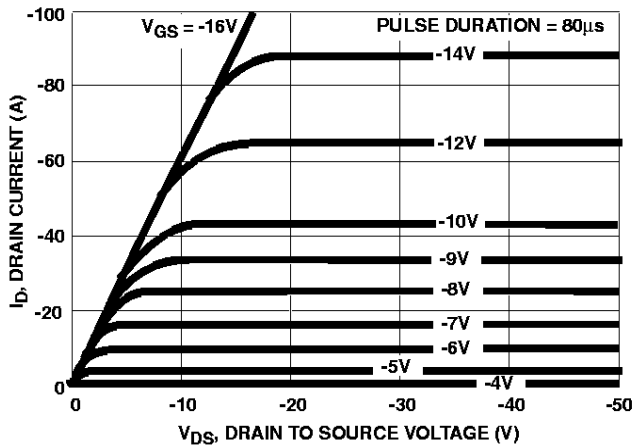


FIGURE 5. OUTPUT CHARACTERISTICS

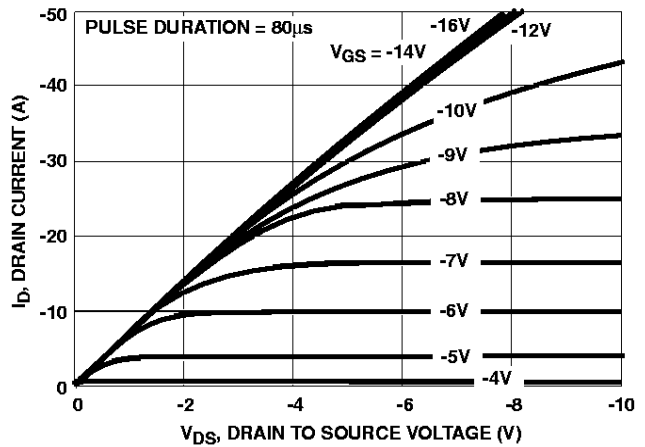


FIGURE 6. SATURATION CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

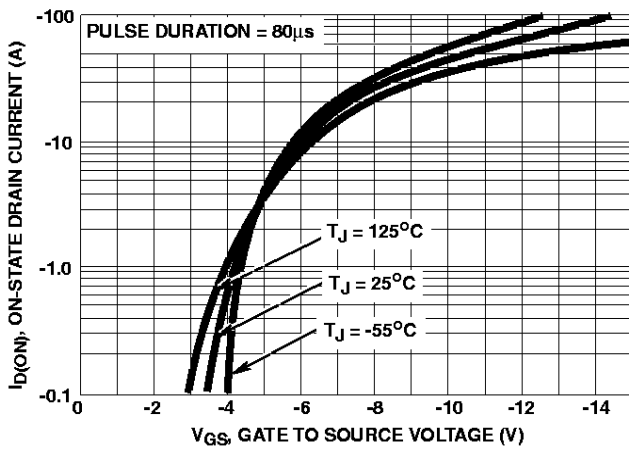
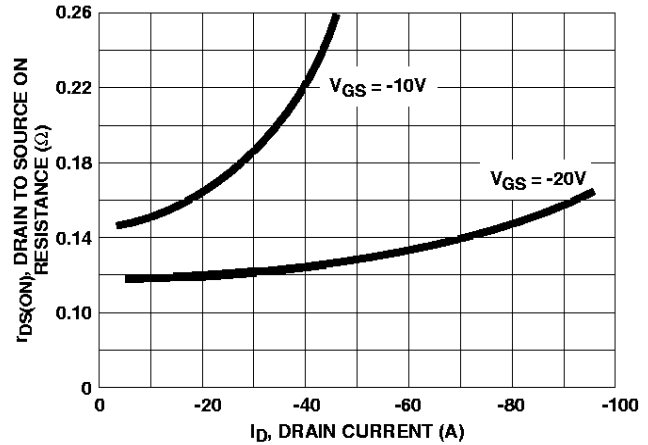


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 5µs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

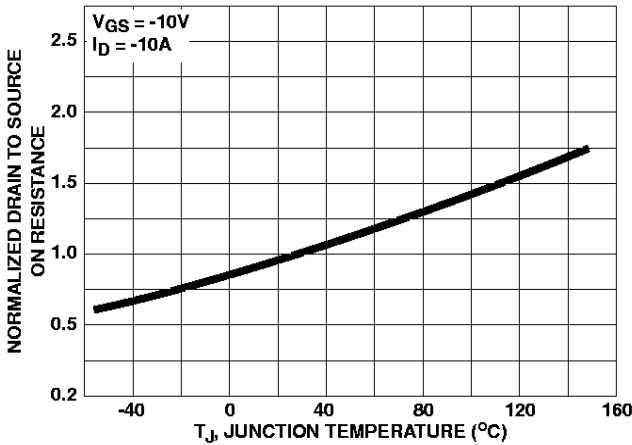


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

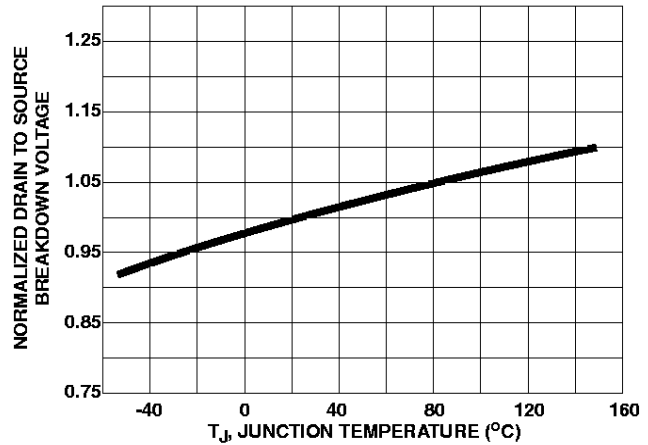


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

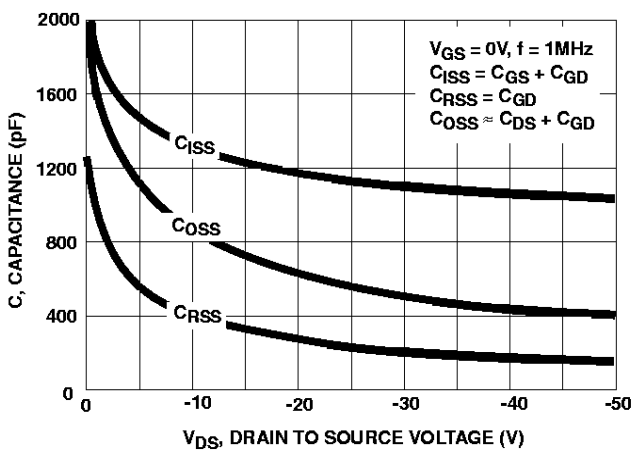


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

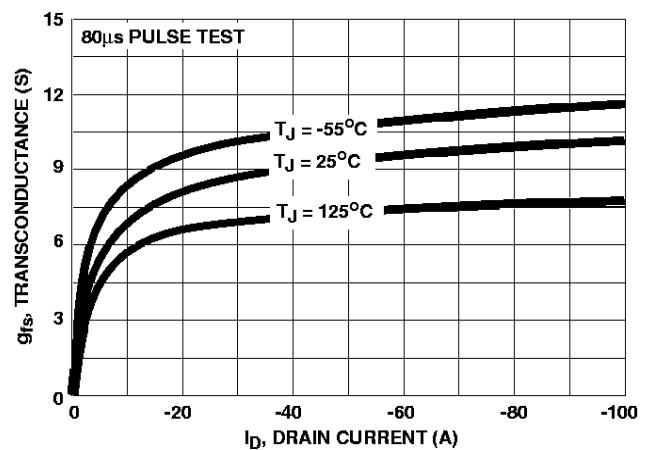


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

**Typical Performance Curves** Unless Otherwise Specified (Continued)

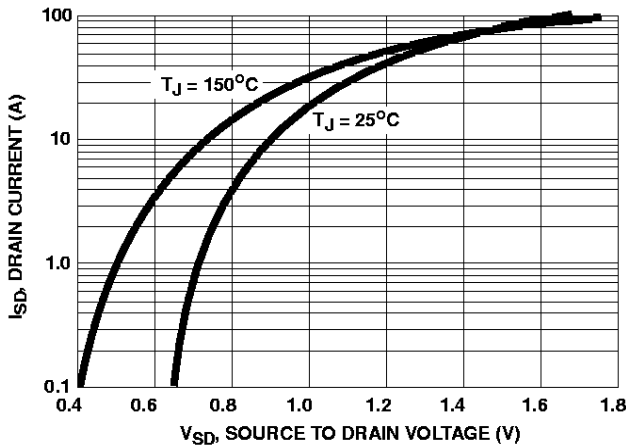


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

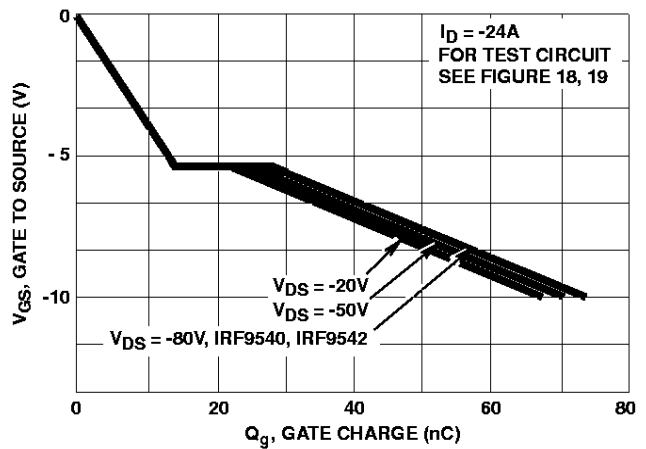


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

**Test Circuits and Waveforms**

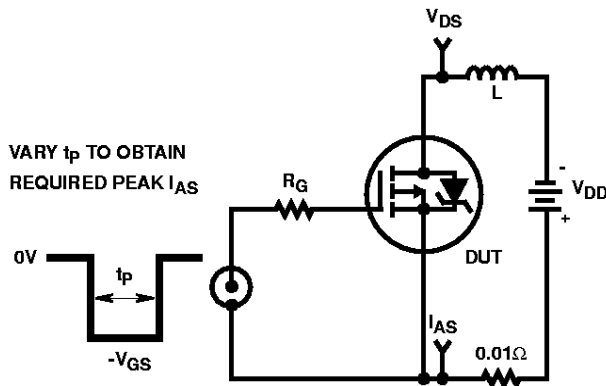


FIGURE 15. UNCLAMPED INDUCTIVE ENERGY TEST CIRCUIT

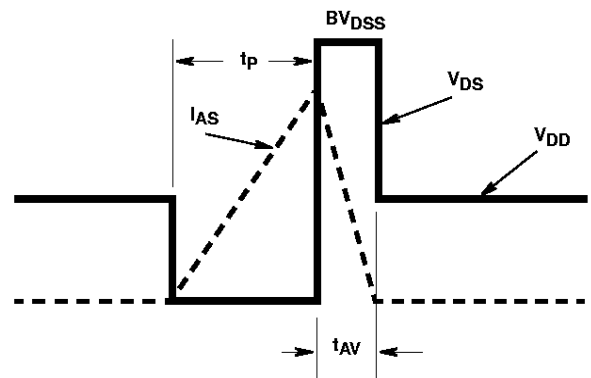


FIGURE 16. UNCLAMPED INDUCTIVE ENERGY WAVEFORMS

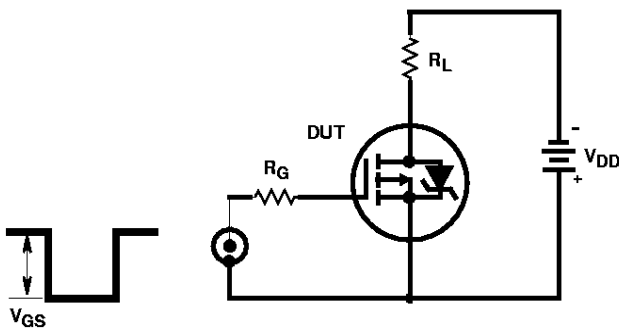


FIGURE 17. SWITCHING TIME TEST CIRCUIT

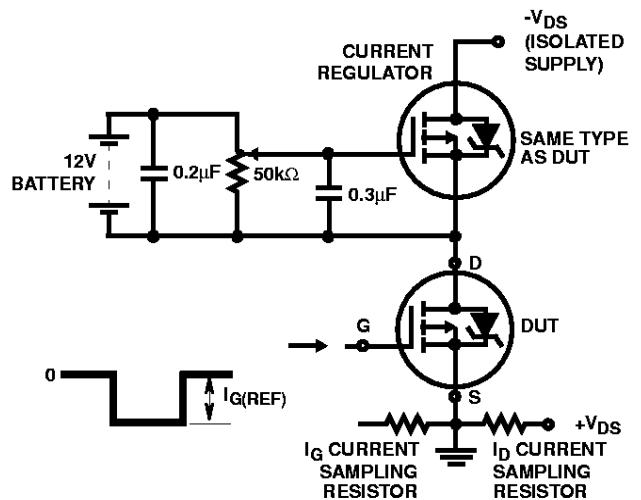


FIGURE 18. GATE CHARGE TEST CIRCUIT

**Test Circuits and Waveforms** (Continued)

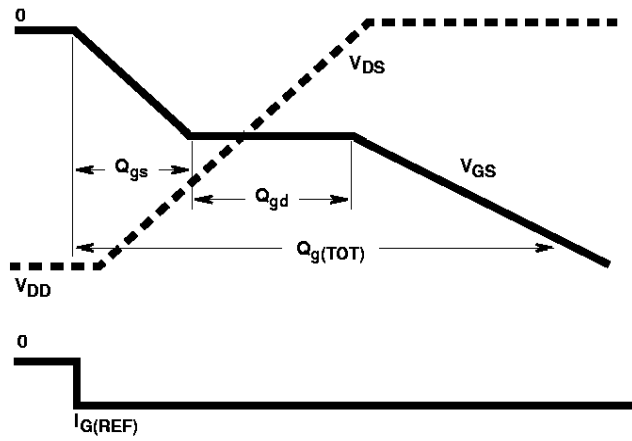
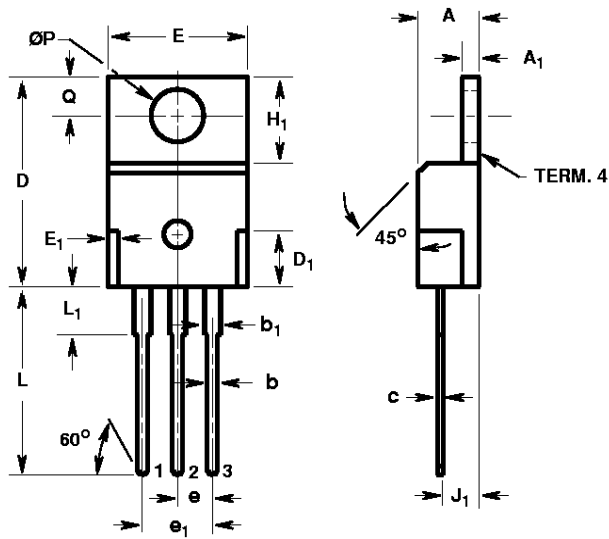


FIGURE 19. GATE CHARGE WAVEFORMS

IRF9540, IRF9541, IRF9542, IRF9543, RF1S9540, RF1S9540SM

**TO-220AB**

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b <sub>1</sub>	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D <sub>1</sub>	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E <sub>1</sub>	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e <sub>1</sub>	0.200 BSC		5.08 BSC		5
H <sub>1</sub>	0.235	0.255	5.97	6.47	-
J <sub>1</sub>	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L <sub>1</sub>	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

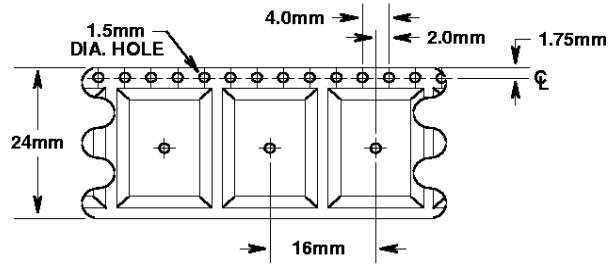
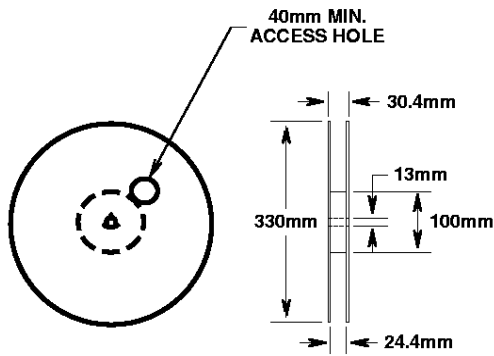
NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L<sub>1</sub>.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

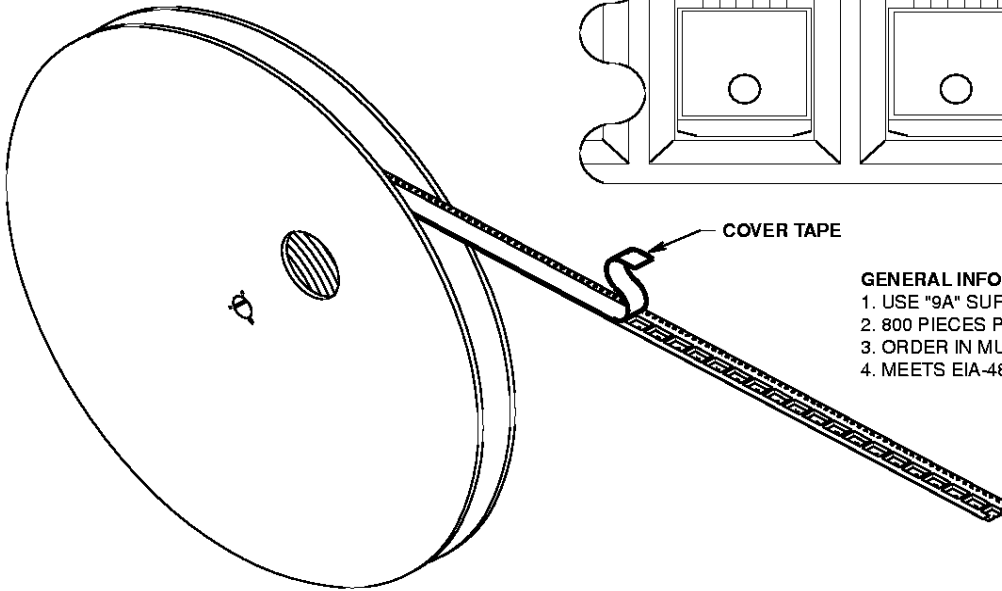
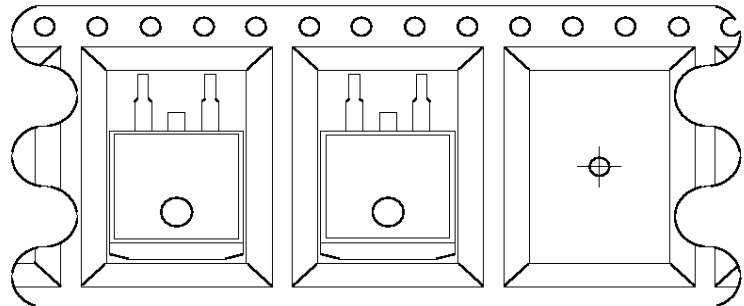


**TO-263AB**

24mm TAPE AND REEL



USER DIRECTION OF FEED



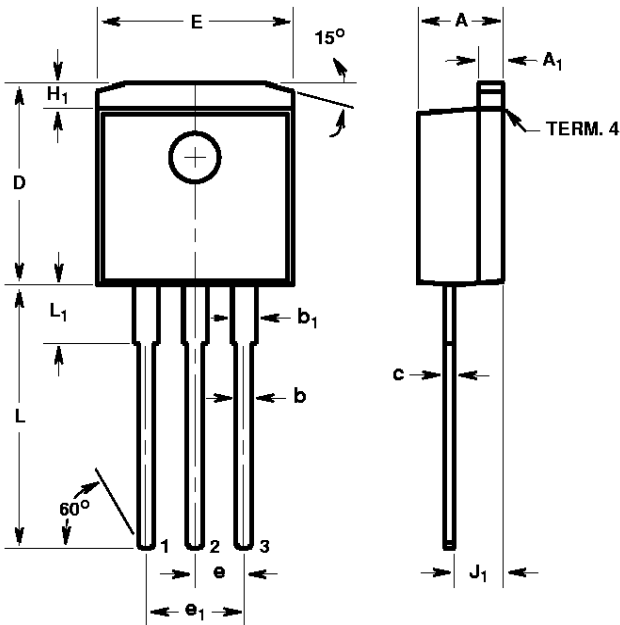
**GENERAL INFORMATION**

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 7 dated 10-95

**TO-262AA**

3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b <sub>1</sub>	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e <sub>1</sub>	0.200 BSC		5.08 BSC		5
H <sub>1</sub>	0.045	0.055	1.15	1.39	-
J <sub>1</sub>	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L <sub>1</sub>	0.110	0.130	2.80	3.30	2

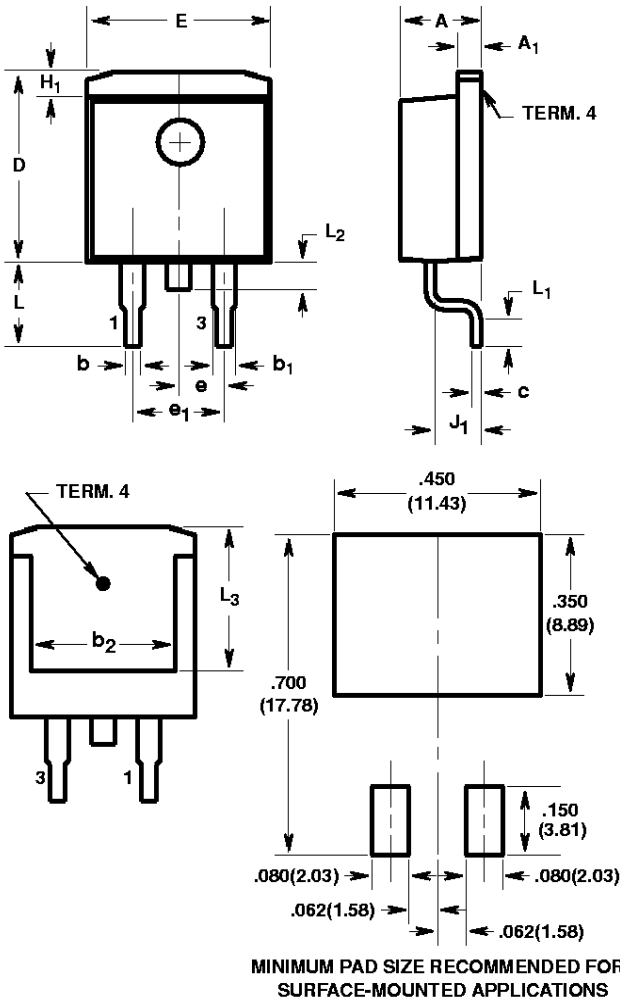
NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 4 dated 10-95.

IRF9540, IRF9541, IRF9542, IRF9543, RF1S9540, RF1S9540SM

**TO-263AB**

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b <sub>1</sub>	0.045	0.055	1.15	1.39	4, 5
b <sub>2</sub>	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e <sub>1</sub>	0.200 BSC		5.08 BSC		7
H <sub>1</sub>	0.045	0.055	1.15	1.39	-
J <sub>1</sub>	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L <sub>1</sub>	0.090	0.110	2.29	2.79	4, 6
L <sub>2</sub>	0.050	0.070	1.27	1.77	3
L <sub>3</sub>	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L<sub>3</sub> and b<sub>2</sub> dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L<sub>1</sub> is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 7 dated 10-95.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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**ASIA**  
 Harris Semiconductor PTE Ltd.  
 No. 1 Tannery Road  
 Cencon 1, #09-01  
 Singapore 1334  
 TEL: (65) 748-4200  
 FAX: (65) 748-0400

