To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

DESCRIPTION

The M62399P,FP is an integrated circuit semiconductor of high voltage type CMOS structure with 8 channels of built-in D-A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer formal of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 2.5mA or more,and it operates in the whole voltage range from VrefU to ground.

And because of connects maximum 8 pieces,it is possible to 64 channels control.

FEATURES
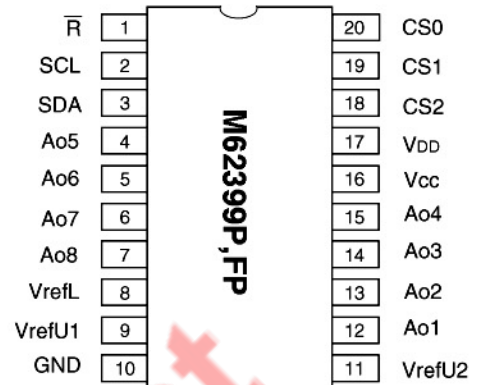
- Digital data transfer format
  I^{2}C-bus serial data method
- Output buffer operational amplifier
  it operates in the whole voltage range from VrefU(0~12V)to ground.
- High output current drive capacity
  ±2.5mA over
- Preparation two high level reference voltage terminal
  because there are two high level reference voltage terminal,it can set up two kinds differ voltage range.

APPLICATION

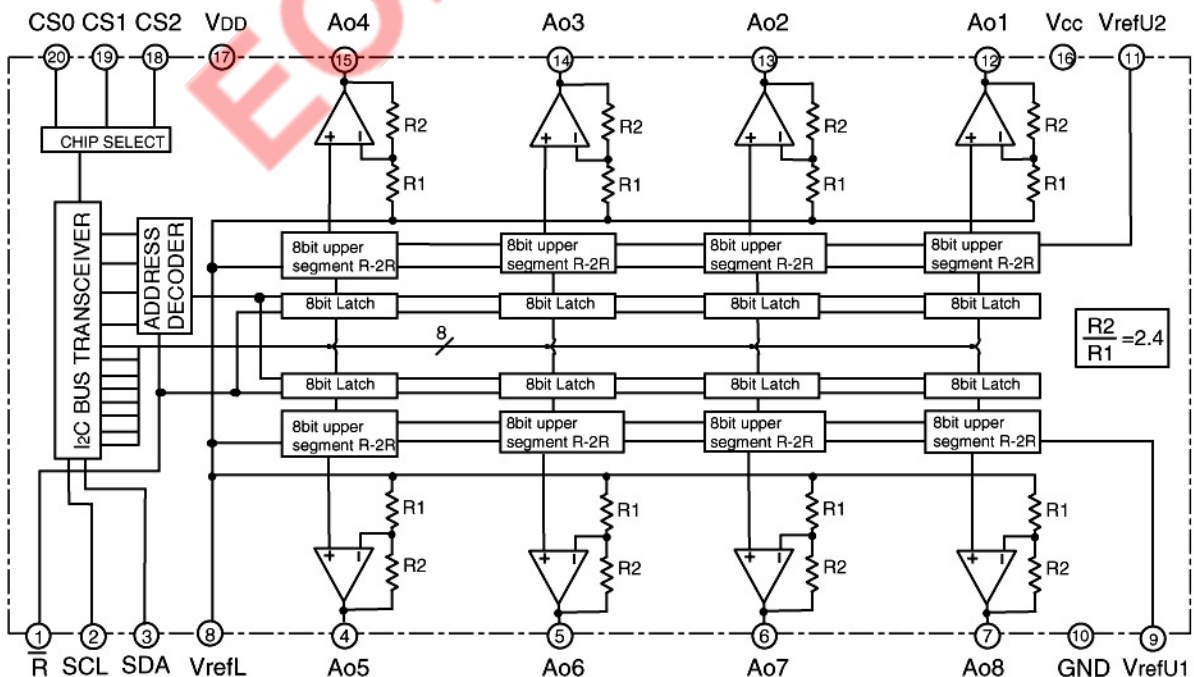Conversion from digital control data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of DISPLAY-MONITOR or CTV.

PIN CONFIGURATION (TOP VIEW)

Pin	Name		Pin	Name
1	$\overline{R}$		20	CS0
2	SCL		19	CS1
3	SDA		18	CS2
4	Ao5		17	VDD
5	Ao6		16	Vcc
6	Ao7		15	Ao4
7	Ao8		14	Ao3
8	VrefL		13	Ao2
9	VrefU1		12	Ao1
10	GND		11	VrefU2

M62399P,FP

Outline 20P4(P)
20P2N-A(FP)

BLOCK DIAGRAM

$\dfrac{R2}{R1}=2.4$

EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
③	SDA	Serial data input terminal
①	$\overline{\text{R}}$	Reset signal input terminal
②	SCL	Serial clock input terminal
⑫	Ao1	
⑬	Ao2	
⑭	Ao3	
⑮	Ao4	8-bit D-A converter output terminal
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	
⑯	Vcc	Analog power supply terminal
⑰	VDD	Digital power supply terminal
⑩	GND	Analog and digital common GND
⑧	VrefL	D-A converter low level reference voltage input terminal
⑨	VrefU1	D-A converter high level reference voltage input terminal 1
⑪	VrefU2	D-A converter high level reference voltage input terminal 2
⑱	CS2	Chip select data input terminal 2
⑲	CS1	Chip select data input terminal 1
⑳	CS0	Chip select data input terminal 0

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3~+13.5	V
VDD	Supply voltage		-0.3~+7.0	V
VrefU1,2	D-A converter upper reference voltage		VDD	V
VIND	Digital input voltage		-0.3~VDD+0.3	V
Topr	Operating temperature		-20~+85	°C
Tstg	Storage temperature		-40~+125	°C

ELECTRICAL CHARACTERISTICS

Digital part(Vcc=13V,VDD=VrefU1,2=+5V±10%,GND=VrefL=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VDD	Supply voltage		4.5	5.0	5.5	V
IDD	Supply current	CLK=1MHz operation IAO=0μA			1	mA
IILK	Input leak current	VIN=0~VDD	-10		10	μA
VIL	Input low voltage				0.2Vcc	V
VIH	Input high voltage		0.8Vcc			V

Analog part(Vcc=13V,VDD=VrefU1,2=+5V±10%,GND=VrefL=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Vcc	Supply voltage		VDD		13	V
Icc	Circuit current	CLK=1MHz operation IAO=0μA		2.0	4.0	mA
IrefU	D-A converter upper reference voltage input current	VrefU=5V VrefL=0V Data condition:at maximum current		1.2	2.5	mA
VrefU	D-A converter upper reference voltage range	The output does not necessarily be the values within the reference voltage setting range.	3.5		VDD	V
VrefL	D-A converter lower reference voltage range		GND		1.5	V
VAO	Buffer amplifier output voltage range	IAO=±500μA	0.1		Vcc-0.1	V
		IAO=±1.0mA	0.2		Vcc-0.2	
IAO	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-2.5		2.5	mA
SDL	Differential nonlinearity error	VrefU=4.79V VrefL=0.95V Vcc=5.5V(15mV/LSB) without load(IAO=0)	-1.0		1.0	LSB
SL	Nonlinearity error		-1.5		1.5	LSB
SZERO	Zero code error		-2.0		2.0	LSB
SFULL	Full scale error		-2.0		2.0	LSB
Eo	Gain error		-3.0		3.0	%
SR	Output slew rate			0.2		V/μs

I²C-BUS LINE CHARACTERISTICS

Symbol	Parameter	Normal mode		High speed mode		Unit
		Min	Max	Min	Max	
f$_{SCL}$	SCL clock frequency	0	100	0	400	KHz
t$_{BUF}$	Time the bus must be free before a new transmission can start	4.7	—	1.3	—	µs
t$_{HD:STA}$	Hold time start condition.After this period.The first clock pulse is generated	4.0	—	0.6	—	µs
t$_{LOW}$	The low period of the clock	4.7	—	1.3	—	µs
t$_{HIGH}$	The high period of the clock	4.0	—	0.6	—	µs
t$_{SU:STA}$	Set up time for start condition(only relevant for a repeated start condition)	4.7	—	4.7	—	µs
t$_{HD:DAT}$	Hold time data	0	—	0	0.9	µs
t$_{SU:DAT}$	Set up time data	250	—	100	—	ns
t$_{R}$	Rise time of both SDA and SCL lines	—	1000	20	300	ns
t$_{F}$	Fall time of both SDA and SCL lines	—	300	20	300	ns
t$_{SU:STO}$	Set up time for stop condition	4.0	—	0.6	—	µs

*Note that transmitter must internally at reset a hold time to bridge the undefined region(max.300ns)of the falling edge of SCL.
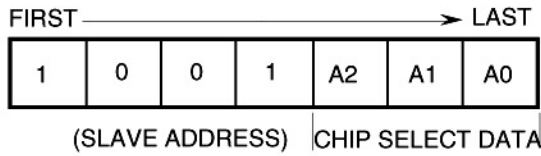
TIMING CHART
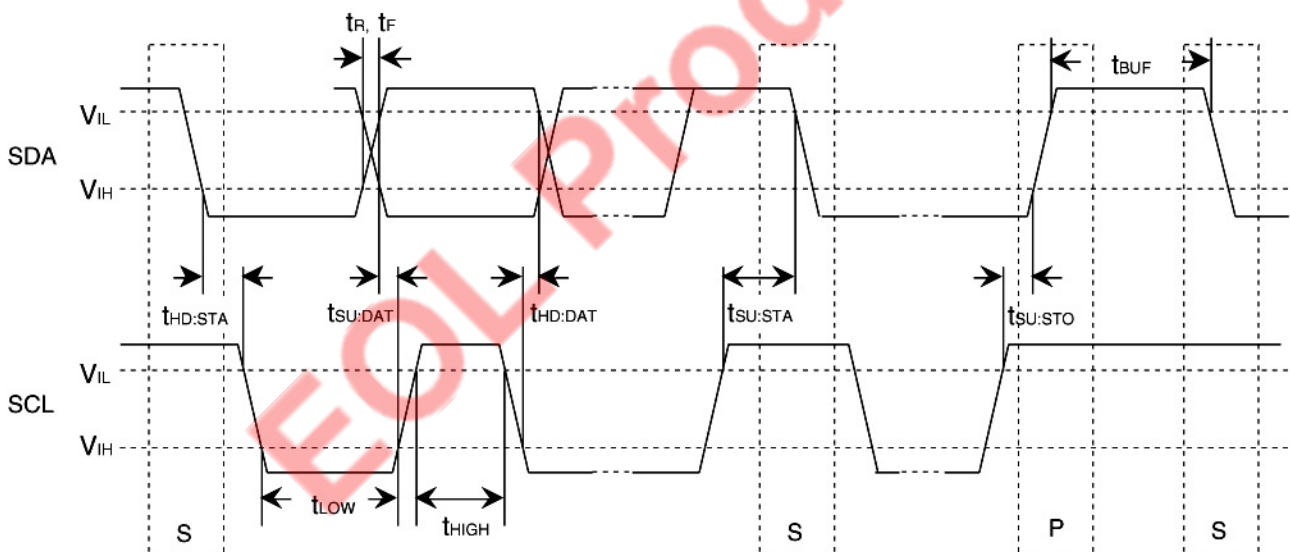
I2C BUS FORMAT

STA	SLAVE ADDRESS	W	A	SUB ADDRESS	A	DAC DATA	A	STP

DIGITAL DATA FORMAT

•SLAVE ADDRESS

FIRST ────────────────→ LAST

1	0	0	1	A2	A1	A0

(SLAVE ADDRESS)　　CHIP SELECT DATA

•SUB ADDRESS

FIRST ────────────────→ LAST

X	X	X	X	S3	S2	S1	S0

◄──── Don't care ────►◄─ CHANNEL SELECT DATA ─►

•DAC DATA

FIRST ────────────────→ LAST
MSB ─────────────────→ LSB

D7	D6	D5	D4	D3	D2	D1	D0
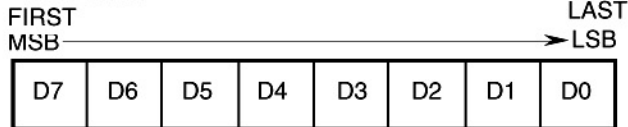
(1)CHIP SELECT DATA

A2 (MSB)	A1	A0	CS2	CS1	CS0 (LSB)
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1

(2)CHANNEL SELECT DATA

S3 (MSB)	S2	S1	S0 (LSB)	Channel selection
0	0	0	0	Don't care.
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
⋮	⋮	⋮	⋮	⋮
0	1	1	1	ch7 selection
1	0	0	0	ch8 selection
1	0	0	1	Don't care.
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Don't care.

(3)DAC DATA

FIRST ────────────────→ LAST
MSB ─────────────────→ LSB

D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	$(VrefU-VrefL)/256 \times 1 \times 2.4 + VrefL$
0	0	0	0	0	0	0	1	$(VrefU-VrefL)/256 \times 2 \times 2.4 + VrefL$
0	0	0	0	0	0	1	0	$(VrefU-VrefL)/256 \times 3 \times 2.4 + VrefL$
0	0	0	0	0	0	1	1	$(VrefU-VrefL)/256 \times 4 \times 2.4 + VrefL$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(VrefU-VrefL)/256 \times 255 \times 2.4 + VrefL$
1	1	1	1	1	1	1	1	$VrefU \times 2.4 + VrefL$