Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

- **Fixed 3.3-V Output**
- **±1% Maximum Output Voltage Tolerance at T_J = 25°C**
- **500-mV Maximum Dropout Voltage at 500 mA**
- **500-mA Dropout Current**
- **±2% Absolute Output Voltage Variation**
- **Internal Overcurrent Limiting**
- **Internal Thermal-Overload Protection**
- **Internal Overvoltage Protection**
- **Package Options Include Plastic Flange Mounted (KTP), Power (KC), and Thin Shrink Small-Outline (PW) Packages, and Ceramic Chip Carriers (FK) and DIPs (J)**

description

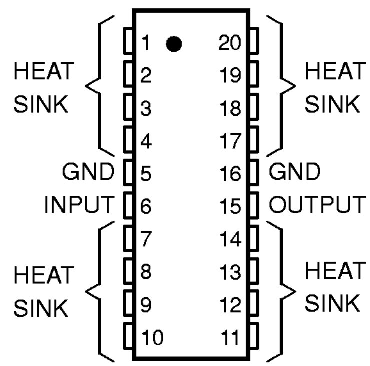
The TLV2217-33 is a low-dropout 3.3-V fixed-voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V or less. The TLV2217-33 provides internal overcurrent limiting, thermal-overload protection, and overvoltage protection.

The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator can drop as low as 3.8 V, and the TLV2217-33 can continue to regulate the system. For higher voltage systems, the TLV2217-33 can be operated with a continuous input voltage of 12 V.

The TLV2217-33 regulators are characterized for operation from 0°C to 125°C virtual junction temperature.

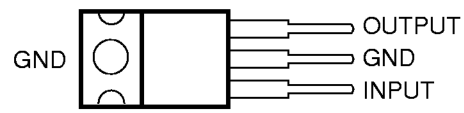
The TLV2217-33M regulators are characterized for operation over the full military virtual junction temperature range of –55°C to 125°C.

PW PACKAGE
(TOP VIEW)



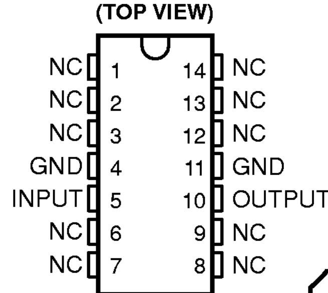
HEAT SINK – These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.

KC PACKAGE
(TOP VIEW)

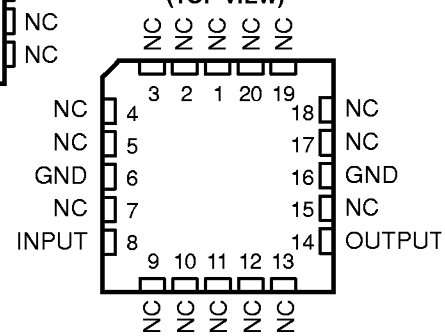


The GND terminal is in electrical contact with the mounting base.

J PACKAGE
(TOP VIEW)

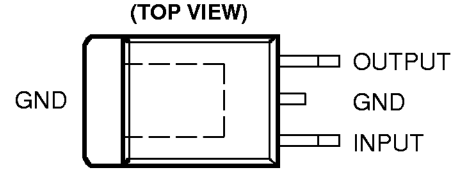


FK PACKAGE
(TOP VIEW)



NC – No internal connection

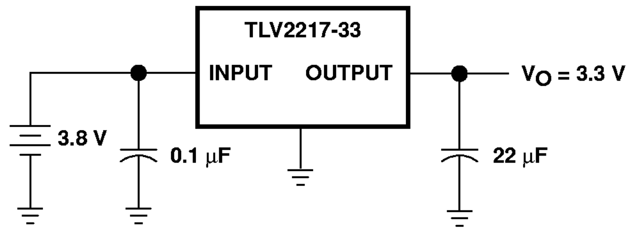
KTP PACKAGE
(TOP VIEW)



The GND terminal is in electrical contact with the mounting base.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

application schematic



AVAILABLE OPTIONS

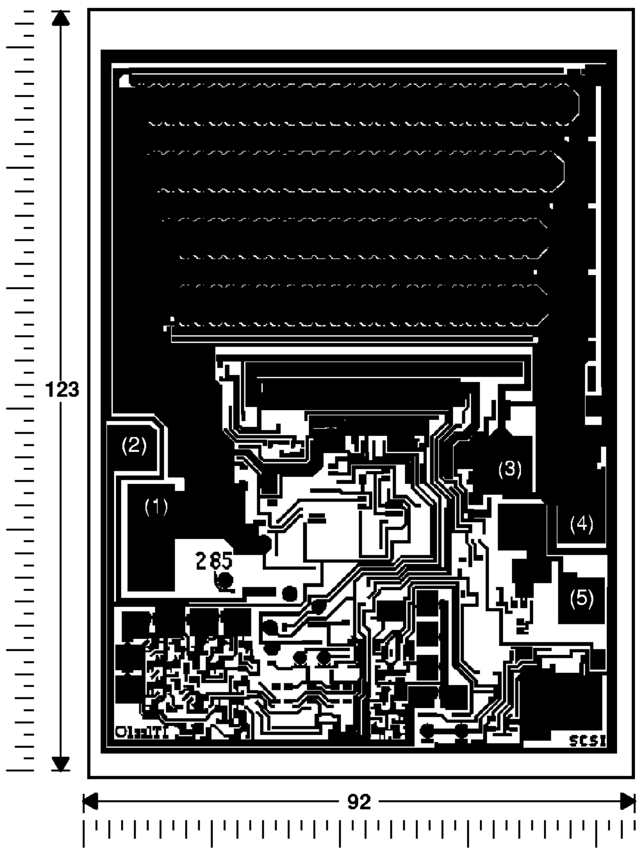
T_J	PACKAGED DEVICES					CHIP FORM (Y)
	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC POWER (KC)	SURFACE MOUNT (PW)†	PLASTIC FLANGE MOUNT (KTP)†	
0°C to 125°C	—	—	TLV2217-33KC	TLV2217-33PWR	TLV2217-33KTPR	TLV2217-33Y
–55°C to 125°C	TLV2217-33MFKB	TLV2217-33MJB	—	—	—	

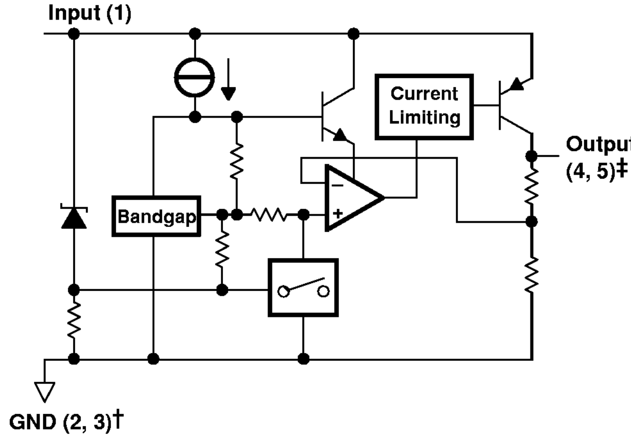
† The KTP and PW packages are available left-end taped and reeled only.

TLV2217-33Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2217-33 (see electrical tables). Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





Chip Thickness: 11 Typical
Bonding Pads: 7 × 7 Minimum
$T_{J(max)}$ = 150°C
Tolerances Are ±10%.
All Dimensions Are in Mils.

† Must connect pads 2 and 3 together
‡ Must connect pads 4 and 5 together

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I . . . . 16 V
Continuous total power dissipation (see Note 1) . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package . . . . 300°C
KC or PW package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
FK	T_A	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	T_A	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
KC	T_A	2000 mW	16 mW/°C	1280 mW	1040 mW	400 mW
	T_C‡	20000 mW	182 mW/°C	14540 mW	11810 mW	4530 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37 mW/°C	2960 mW	2405 mW	925 mW
KTP	T_A	1800 mW	14.5 mW/°C	1147 mW	943 mW	363 mW
	T_C‡	18000 mW	163.6 mW/°C	13091 mW	10636 mW	4091 mW

‡ Derate above 40°C

MAXIMUM CONTINUOUS DISSIPATION vs FREE-AIR TEMPERATURE

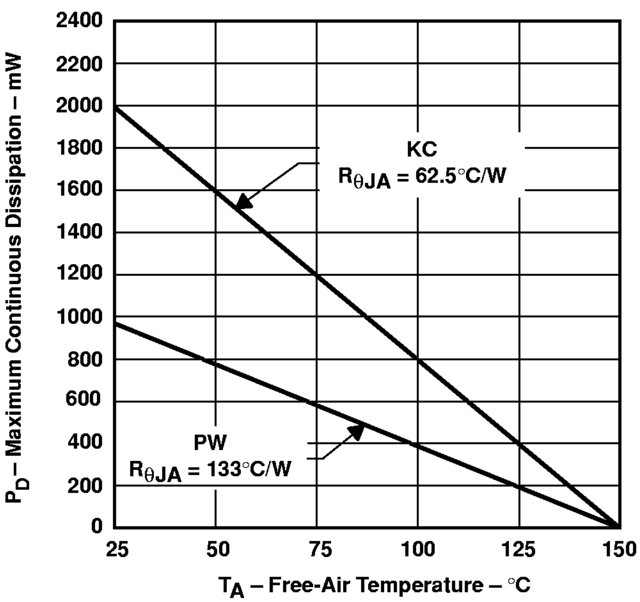


Figure 1

MAXIMUM CONTINUOUS DISSIPATION vs CASE TEMPERATURE

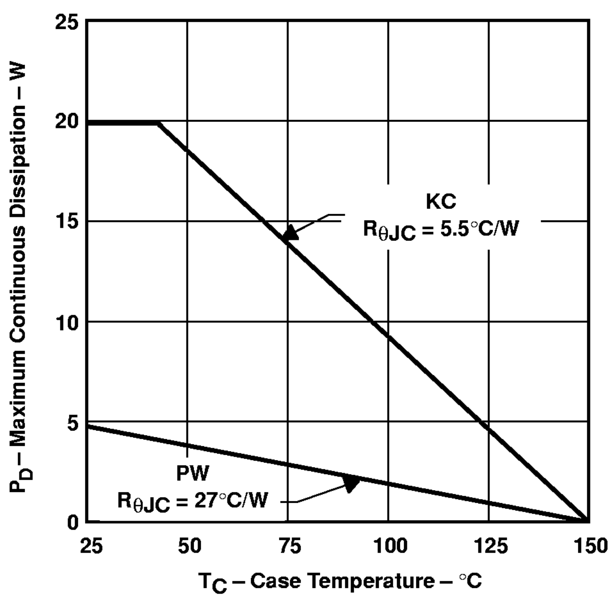


Figure 2

TLV2217-33 recommended operating conditions

	TLV2217-33 MIN	TLV2217-33 MAX	UNIT
Input voltage, V_I	3.8	12	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

TLV2217-33M recommended operating conditions

		TLV2217-33M MIN	TLV2217-33M MAX	UNIT
Input voltage, V_I	T_J = 25°C	3.8	12	V
	T_J = –55°C to 125°C	3.9	12	
Output current, I_O		0	480	mA
Operating virtual junction temperature range, T_J		–55	125	°C

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	3.267	3.30	3.333	V
		T_J = 0°C to 125°C	3.234		3.366	
Input voltage regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}			–62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33M MIN	TLV2217-33M TYP	TLV2217-33M MAX	UNIT
Output voltage	I_O = 20 mA to 480 mA	V_I = 3.8 V to 5.5 V, T_J = 25°	3.267	3.3	3.333	V
		V_I = 3.9 V to 5.5 V	3.234		3.366	
Input voltage regulation	V_I = 3.8 V to 5.5 V,	T_J = 25°C			15	mV
Ripple rejection	f = 120 Hz,	V_{ripple} = 1 V_{PP}		–62		dB
Output voltage regulation	I_O = 20 mA to 480 mA,	T_J = 25°C			30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 480 mA,	T_J = 25°C			500	
	I_O = 480 mA				550	
Bias current	I_O = 0				5	mA
	I_O = 480 mA				49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33Y MIN	TLV2217-33Y TYP	TLV2217-33Y MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA,	V_I = 3.8 V to 5.5 V	3.267	3.30	3.333	V
Input voltage regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz,	V_{ripple} = 1 V_{PP}		–62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

ESR OF OUTPUT CAPACITOR vs LOAD CURRENT

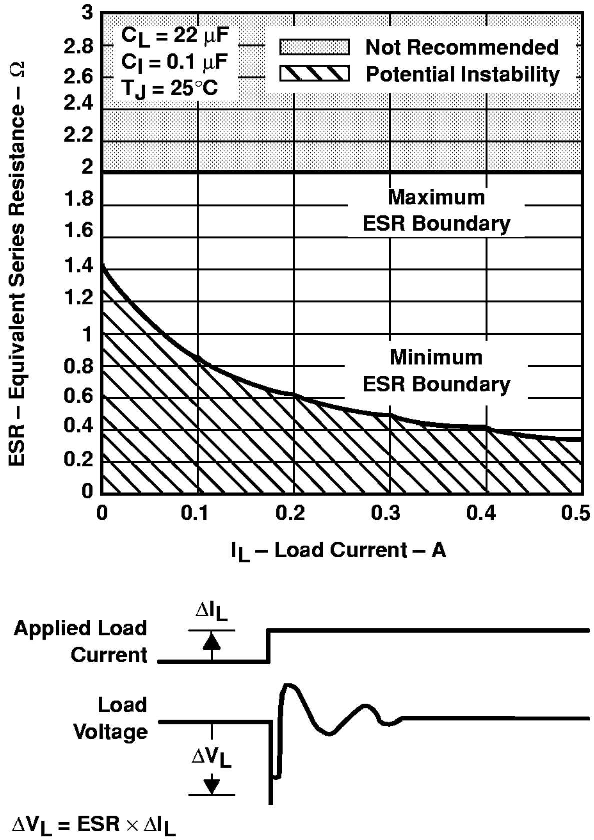


Figure 3

STABILITY vs ESR

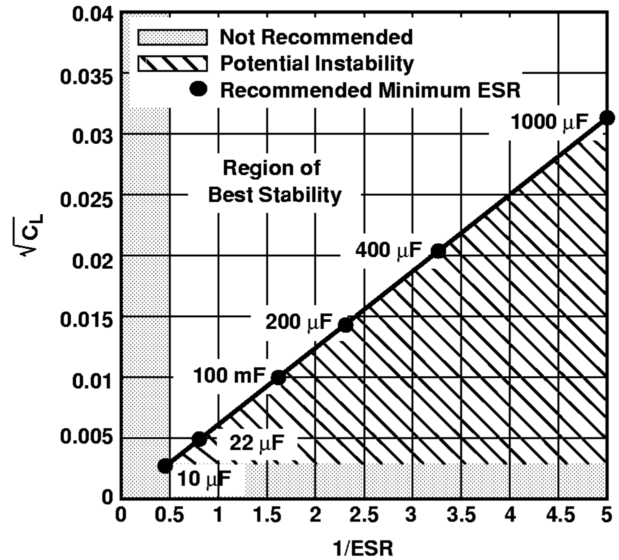


Figure 4

IMPORTANT NOTICE