

# MM54HCT164/MM74HCT164 8-Bit Serial-in/Parallel-out Shift Register

## General Description

The MM54HCT164/MM74HCT164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

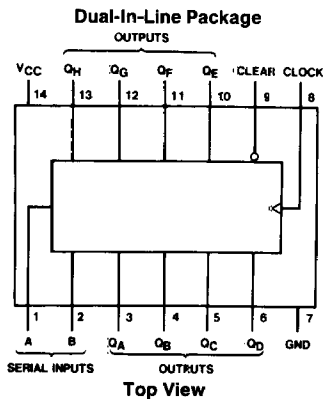
The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

## Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40  $\mu A$  maximum (74HCT Series)
- Low input current: 1  $\mu A$  maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

## Connection Diagram



## Truth Table

Inputs				Outputs			
Clear	Clock	A	B	QA	QB	...	QH
L	X	X	X	L	L		L
H	L	X	X	QA0	QB0		QH0
H	↑	H	H	H	QAn		QGn
H	↑	L	X	L	QAn		QGn
H	↑	X	L	L	QAn		QGn

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

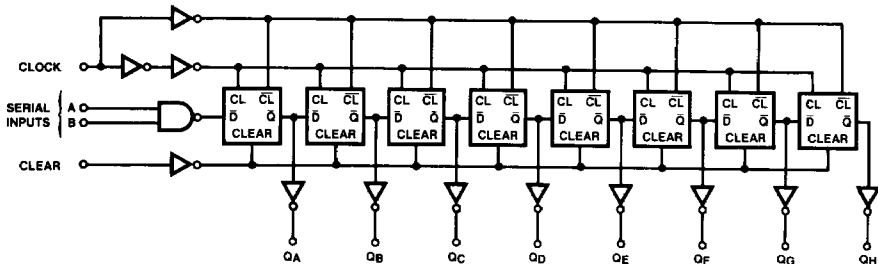
QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady state input conditions were established.

QAn, QGn = The level of QA or QG before the most recent ↑ transition of the clock; indicated a one-bit shift.

Order Number MM54HCT164\* or MM74HCT164\*

\*Please look into Section 8, Appendix D for availability of various package types.

## Logic Diagram



**Absolute Maximum Ratings** (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package Only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.5	5.5	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )		500	ns

**DC Electrical Characteristics**  $V_{CC} = 5V \pm 10\%$  (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage			2.0	2.0	2.0	V
$V_{IL}$	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu A$ $ I_{OUT}  = 4.0$ mA, $V_{CC} = 4.5V$ $ I_{OUT}  = 4.8$ mA, $V_{CC} = 5.5V$	$V_{CC}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
			4.2	3.98	3.84	3.7	V
			5.2	4.98	4.84	4.7	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu A$ $ I_{OUT}  = 4.0$ mA, $V_{CC} = 4.5V$ $ I_{OUT}  = 4.8$ mA, $V_{CC} = 5.5V$	0	0.1	0.1	0.1	V
			0.2	0.26	0.33	0.4	V
			0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8.0	80	160	$\mu A$
		$V_{IN} = 2.4V$ or 0.4V (Note 4)		1.0	1.3	1.5	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** This is measured per pin. All other inputs are held at  $V_{CC}$  ground.

### AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency from Clock to Q	50% Duty Cycle Clock	55	35	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Clock to Q		17	27	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay from Clear to Q		23	38	ns
$t_{REM}$	Minimum Removal Time, Clear to Clock		3	6	ns
$t_S$	Minimum Set Up Time Data to Clock	$t_H \geq 20 \text{ ns}$	6	13	ns
$t_H$	Minimum Hold Time Clock to Data	$t_S \geq 20 \text{ ns}$	1.5	5	ns
$t_W$	Minimum Pulse Width Clock, Preset or Clear		9	16	ns

### AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%, C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT $T_A = -40^\circ C \text{ to } 85^\circ C$		54HCT $T_A = -55^\circ C \text{ to } 125^\circ C$		Units
			Typ	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Operating Frequency	50% Duty Cycle Clock	45	30		25		22	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay from Clock to Q		20	30		38		45	ns
$t_{PHL}$	Maximum Propagation Delay from Clear to Q		26	41		51		61	ns
$t_{REM}$	Minimum Removal Time Clear to Clock		4	8		10		14	ns
$t_S$	Minimum Setup Time Data to Clock	$t_H \geq 20 \text{ ns}$	7	15		19		23	ns
$t_H$	Minimum Hold Time Clock to Data	$t_S \geq 20 \text{ ns}$	1.5	5		5		5	ns
$t_W$	Minimum Pulse Width Clock, or Clear		10	18		22		27	ns
$t_r, t_f$	Maximum Input Rise and Fall Time			500		500		500	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time			15		19		22	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per flip-flop)	160						pF
$C_{IN}$	Maximum Input Capacitance		5	10		10		10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Note 6:** Refer to back of the section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.