

**FEATURES**

- Functionally compliant with IEEE 802.3z Gigabit Ethernet Applications
- 1250 MHz (Gigabit Ethernet) operating rate - 1/2 Rate Operation
- Quad Transmitter incorporating phase-locked loop (PLL) clock synthesis from low speed reference
- Quad Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- Low-jitter serial PECL interface
- Local Loopback
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 2.3 W Power dissipation
- Compact 23mm x 23mm 208 TBGA package

**APPLICATIONS**

High-speed data communications

- Ethernet Backbones
- Multi-port Gigabit Ethernet Cards
- Switched networks
- Data broadcast environments

**GENERAL DESCRIPTION**

The S2066 quad transmitter and receiver chip is designed to provide four channels of high-speed serial data transmission over fiber optic or copper interfaces conforming to the requirements of the IEEE 802.3z Gigabit Ethernet specification. The chip runs at 1250.0 Mbit/s serial data rate with an associated 10-bit parallel data word. The chip provides four separate transceivers which can be operated individually at slightly different frequencies.

Each bi-directional channel provides parallel to serial and serial to parallel conversion, clock generation and recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip quad receive PLL is used for clock recovery and data re-timing on the four independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces and provide excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates approximately 2.3 watts.

Figure 1 shows the use of the S2064 and S2066 in a Gigabit Ethernet application. Figure 2 summarizes the input/output signals of the device. Figures 3 and 4 show the transmit and receive block diagrams, respectively.

**Figure 1. Typical Quad Gigabit Ethernet Application**

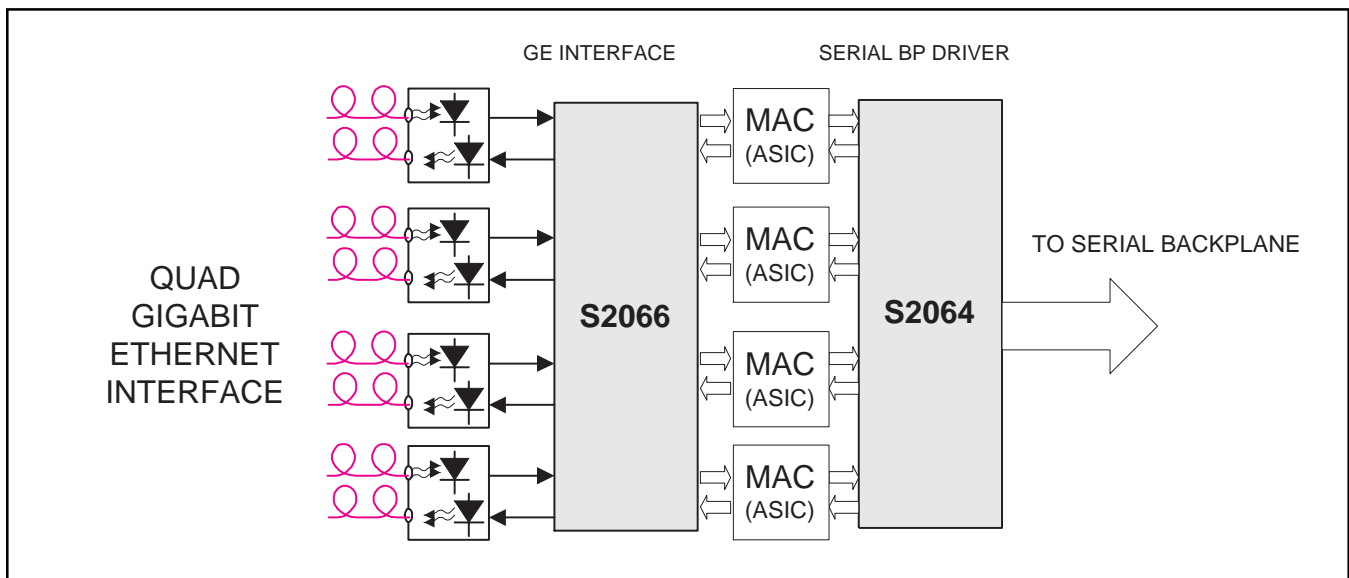


Figure 2. S2066 Input/Output Diagram

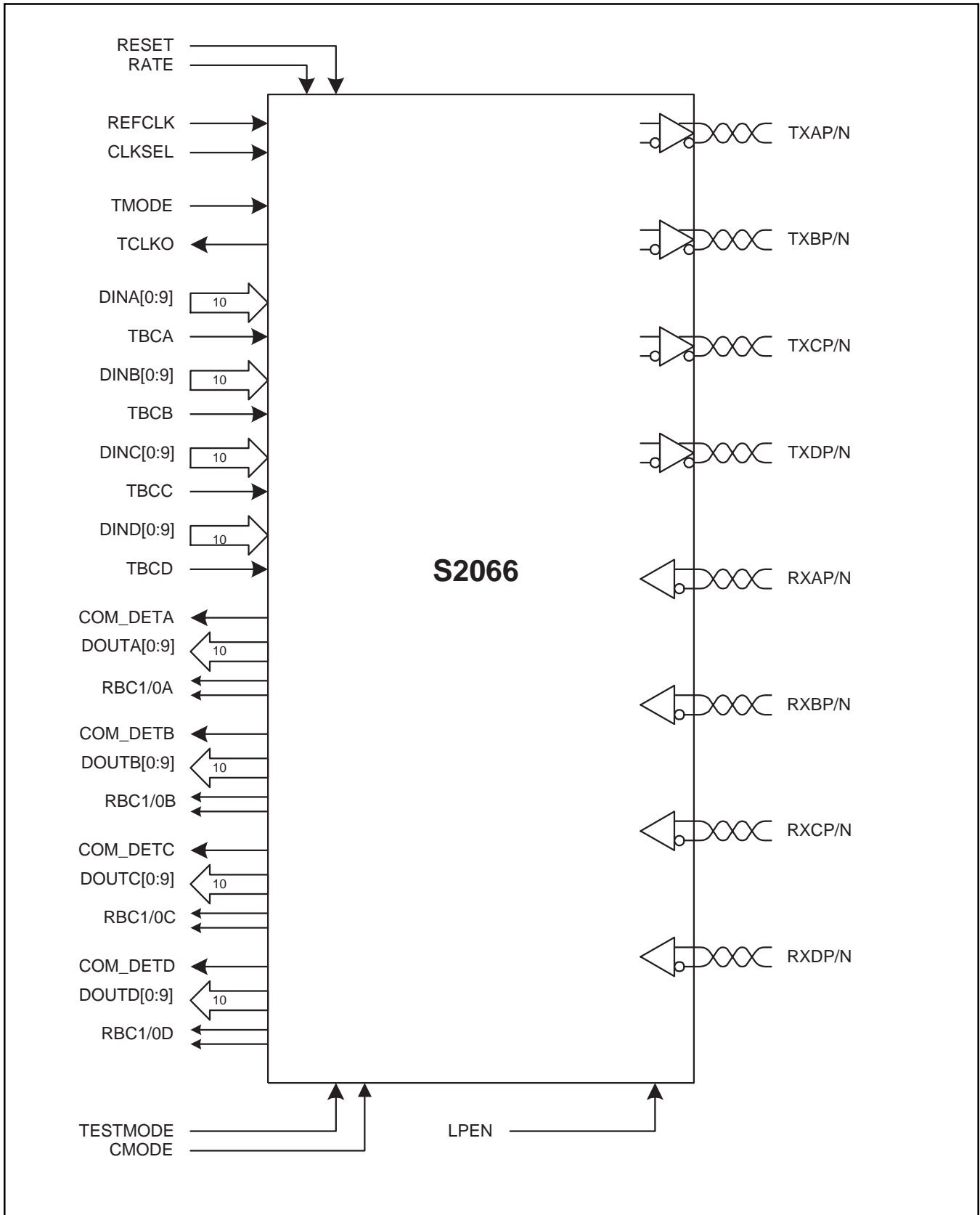


Figure 3. Transmitter Block Diagram

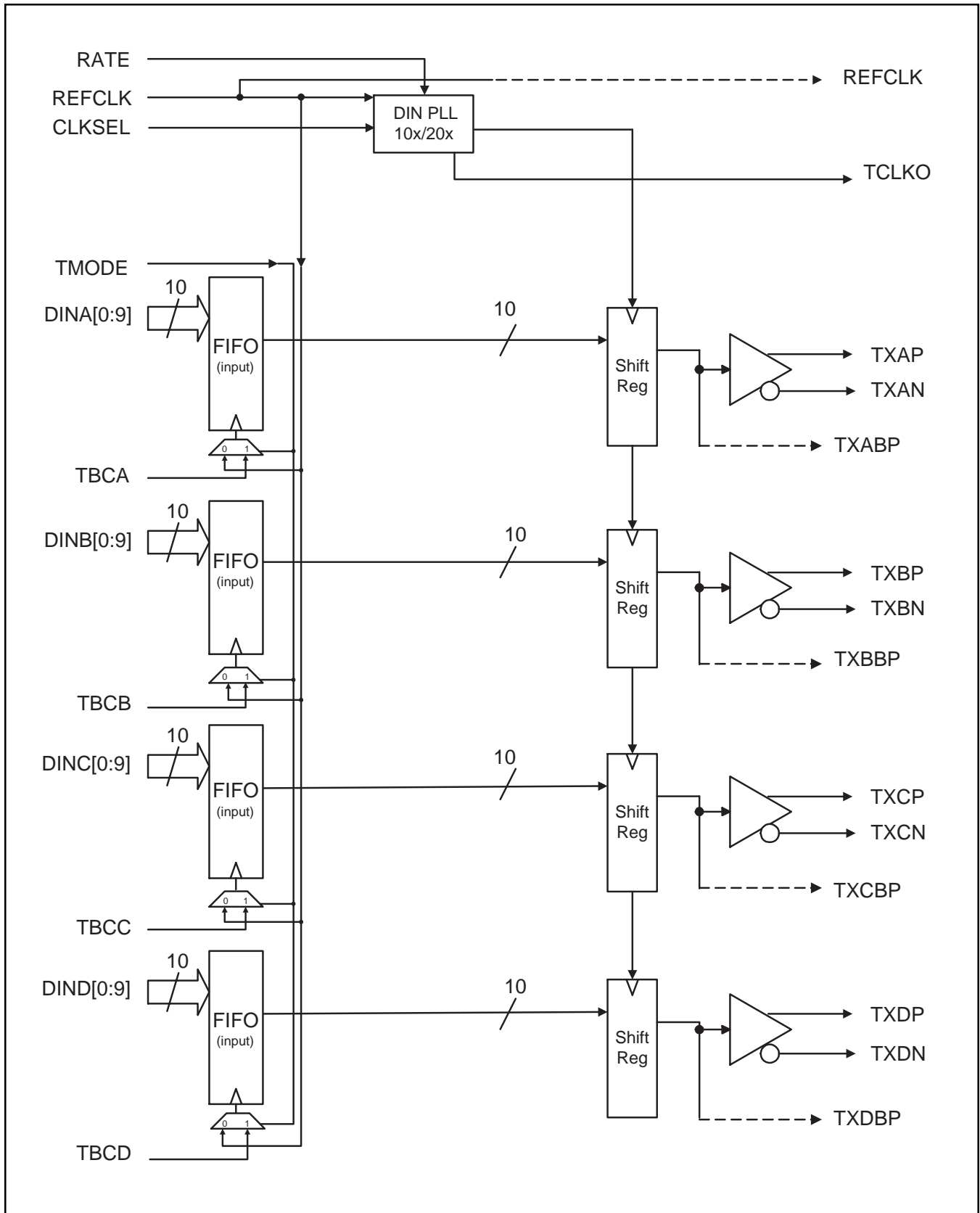
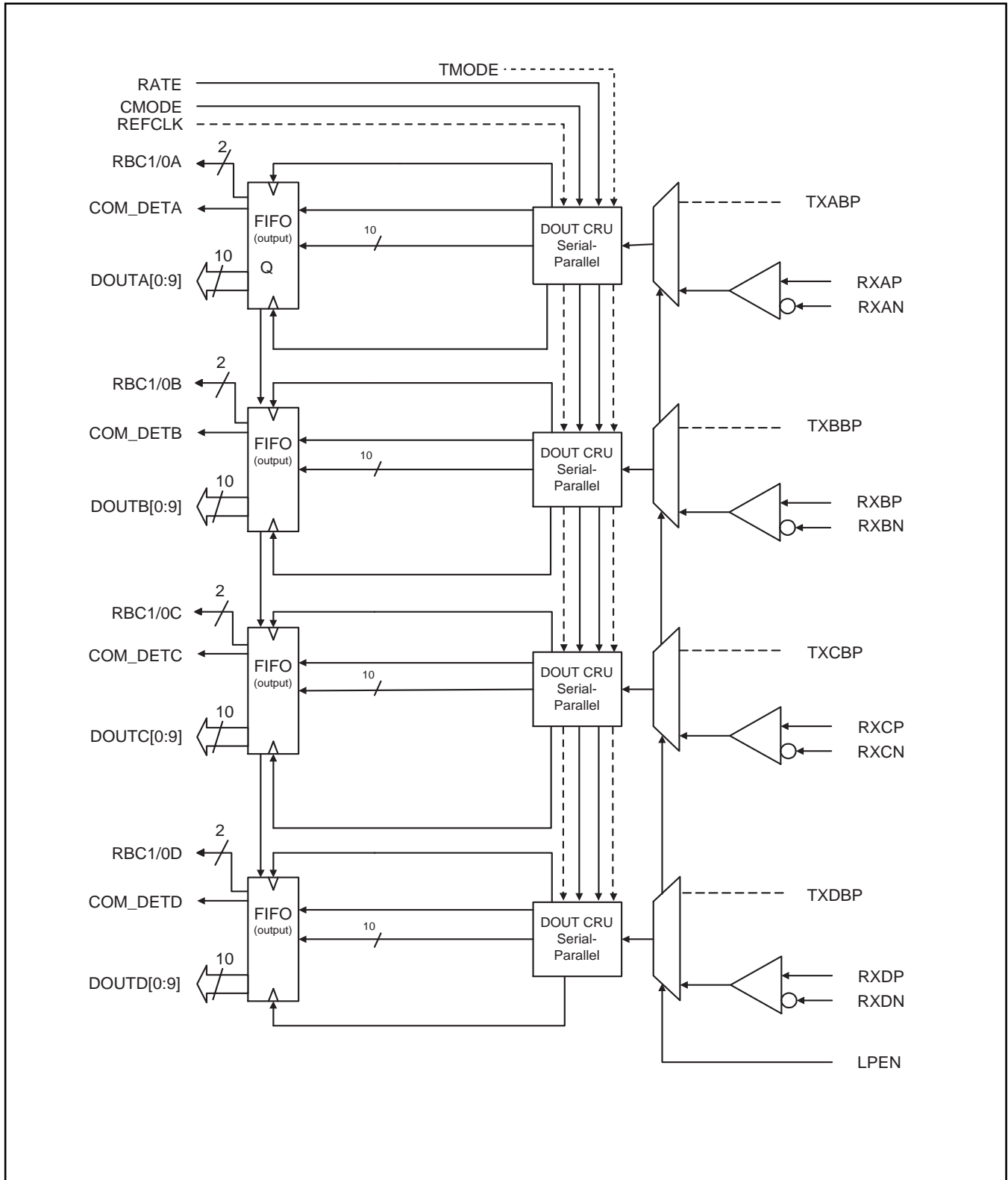


Figure 4. Receiver Block Diagram



**TRANSMITTER DESCRIPTION**

The transmitter section of the S2066 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Transmitter functionalities are shown schematically in Figure 3. Four channels are provided with a variety of options regarding input clocking and loopback. The transmitters operate at 1.250 GHz, 10 or 20 times the reference clock frequency.

**Data Input**

The S2066 has been designed to simplify the parallel interface data transfer and provides flexibility in the clocking of parallel data. Prior implementations of this function have either forced the user to synchronize transmit data to the reference clock or to provide the output clock as a reference to the PLL, resulting in increased jitter at the serial interface. The S2066 incorporates a unique FIFO structure which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device.

**Table 1. Operating Rates**

RATE	CLKSEL	REFCLK Frequency	Serial Output Rate	TCLK0 Freq
0	0	SDR/10	1250 Mbps	SDR/10
0	1	SDR/20	1250 Mbps	SDR/10
1	0	SDR/10	625 Mbps	SDR/10
1	1	SDR/20	625 Mbps	SDR/10

Note: SDR = Serial Data Rate.

**Table 2. Input Modes**

TMODE	Operation
0	REFCLK Mode. REFCLK used for all channels.
1	TBC Mode. TBCx used to clock data into all FIFOs.

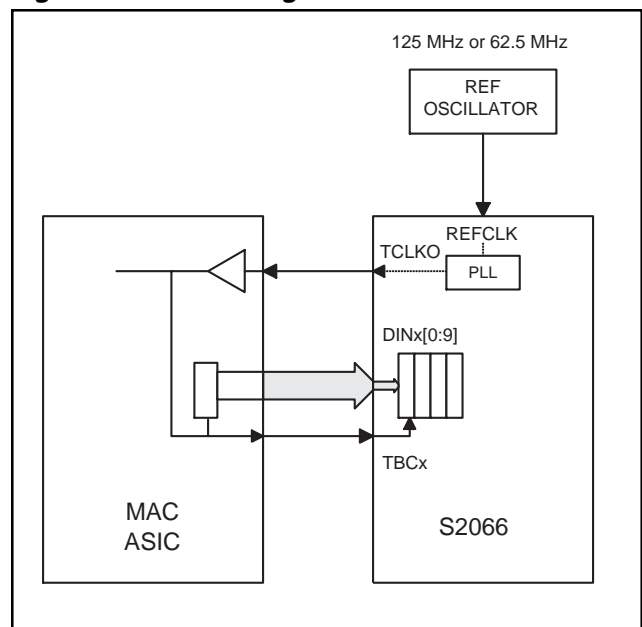
Note that internal synchronization of FIFOs is performed upon de-assertion of RESET.

The S2066 also provides a system clock output, TCLK0, which is derived from the internal VCO. The frequency of this output is constant at the parallel word rate, 1/10 the serial data rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be used by upstream circuitry as a system clock. See Table 1.

Data to be input to the S2066 should be coded to insure transition density and DC balance. Data is input to each channel of the S2066 as a 10 bit wide word. An input FIFO and a clock input, TBCx, are provided for each channel of the S2066. The device can operate in two different modes. The S2066 can be configured to use either the TBCx (TBC MODE) input or the REFCLK input (REFCLK MODE). Table 2 provides a summary of the input modes for the S2066.

Operation in the TBC MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the 125 Mbps 10 bit interface. The TBC signal is used to clock the data into an internal holding register and the S2066 synchronizes its internal data flow to ensure stable operation. REFCLK, not TBCx, is used as the reference for the DIN PLL. This ensures minimum jitter on the high speed serial data stream.

**Figure 5. DIN Clocking with TBC**



The TBC must be frequency locked to REFCLK, but may have an arbitrary but fixed phase relationship. Adjustment of internal timing of the S2066 is performed during reset. Once synchronized, the S2066 can tolerate up to  $\pm 3$ ns of phase drift between TBC and REFCLK.

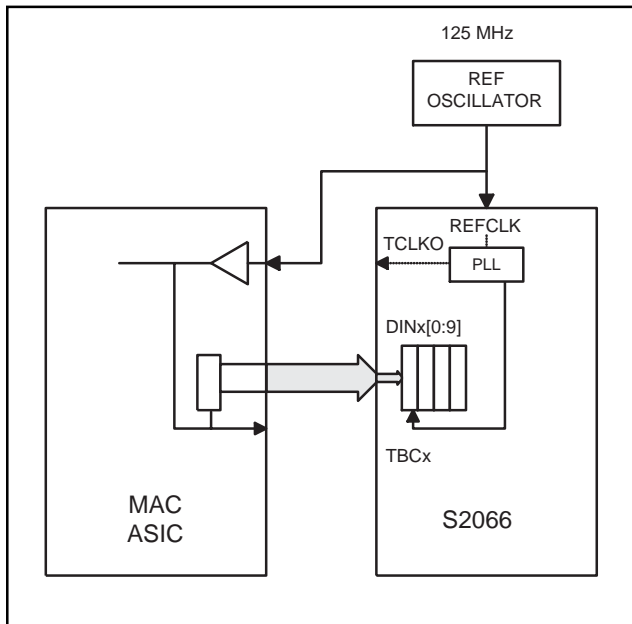
Figure 5 demonstrates the flexibility afforded by the S2066. A low jitter reference is provided directly to the S2066 at either 1/10 or 1/20 the serial data rate. This insures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. This clock can be buffered as required without concern about added delay. There is no phase requirement between TCLKO and the TBCx clock, which is provided back to the S2066, other than that they remain within  $\pm 3$ ns of the phase relationship established at reset .

The S2066 also supports the traditional REFCLK clocking found in Gigabit Ethernet applications and is illustrated in Figure 6.

### Half Rate Operation

The S2066 supports full and 1/2 rate operation for all modes of operation. When RATE is LOW, the S2066

**Figure 6. GE DIN Clocking with REFCLK**



serial data rate equals the VCO frequency. When RATE is HIGH, the VCO frequency is divided by 2 before being provided to the rest of the chip. Thus the S2066 can support Gigabit Ethernet and serial backplane functions at both full and 1/2 the VCO rate.

### Parallel-to-Serial Conversion

The 10-bit parallel data handled by the S2066 device should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded, 8 bits at a time, into a 10-bit transmission character and must be compliant with IEEE 802.3z Gigabit Ethernet specification.

The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data<sup>1</sup>.

Table 3 identifies the mapping of the 8B/10B characters to the data inputs of the S2066. The S2066 will serialize the parallel data for each channel and will transmit bit "a" or DIN[0] first.

### Frequency Synthesizer (PLL)

1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

**Table 3. Data to 8B/10B Alphabetic Representation**

DIN[0:9] or DOUT[0:9]	Data Byte									
	0	1	2	3	4	5	6	7	8	9
8B/10B alph. repr.	a	b	c	d	e	i	f	g	h	j

The S2066 synthesizes a serial transmit clock from the reference signal provided. The S2066 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

### Test Functions

The S2066 can be configured for factory test to aid in functional testing of the device. When in the test mode, the internal transmit and receive voltage-controlled oscillator (VCO) is bypassed and the reference clock substituted. This allows full functional testing of the digital portion of the chip or bypassing the internal synthesized clock with an external clock source. (See the section Other Operating Modes.)

### Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to insure that the clock recovery units can lock to the serial data.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL = 1. Note that in both cases, the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate.

### Serial Data Outputs

The S2066 provides LVPECL level serial outputs. Each high speed output should be provided with a resistor to VSS (Gnd) near the device. A value of 4.5K $\Omega$  provides optimal performance with minimum impact on power dissipation. The resistance may be as low as 450 $\Omega$ , but will dissipate additional power with no substantive performance improvement.

### Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TBC to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET signal. The DIN FIFO is automatically reset upon power up immediately after the DIN PLL obtains stable frequency lock. If the circuit has not reached steady state timing at this point, then the user must initialize by asserting the RESET signal. The TCLKO output will operate normally even when RESET is asserted and is available for use as an upstream clock source.

## RECEIVER DESCRIPTION

Each receiver channel is designed to implement the IEEE 802.3z Gigabit Ethernet receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 4.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2066 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the word-aligned data on its parallel outputs.

### Data Input

A differential input receiver is provided for each channel of the S2066. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for all four channels is controlled by the loopback enable signal, LPEN.

The high speed serial inputs to the S2066 are internally biased to VDD-1.3V. This facilitates AC-coupling of the differential inputs and termination with a single differential termination.

### Clock Recovery Function

Clock recovery is provided for each channel of the S2066. The receiver PLL has been optimized for the needs of Gigabit Ethernet systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs.

The run-length requirements insure that the S2066 will respond appropriately and quickly to a loss of signal. The run-length checker looks for a minimum of 120 consecutive ones or zeros. The checking is done in parallel, thus 12 parallel words are examined.

An off-frequency detection circuit in the S2066 monitors the receiver VCO frequency to ensure that the input signal is at a valid data rate. The recovered data clock must be within 200 ppm of the reference clock for reliable locking of the CRU to the data stream.

If both the off-frequency test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. Note that if the run length test is satisfied due to noise on the inputs, and no signal is present, the receiver VCO will maintain frequency accuracy to within 100 ppm of the target rate as determined by the REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RBC1/0x outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

If at any time, the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This is required to guarantee that the VCO maintains the correct frequency in the absence of data.

### Reference Clock Input

The reference clock must be provided from a low jitter clock source. The frequency of the recovered data clock (divided by 10 or 20) must be within 200 ppm of the reference clock to insure reliable locking of the receiver PLL. A single reference clock is provided to both the transmitter and the receiver of the S2066.



**Serial to Parallel Conversion**

Once bit synchronization has been attained by the S2066 CRU, the S2066 must synchronize to the 10 bit word boundary. Word synchronization in the S2066 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2066 will detect and byte-align to either polarity of the K28.5. Each channel of the S2066 will detect and align to a K28.5 anywhere in the data stream. The presence of a K28.5 is indicated for each channel by the assertion of the COM\_DET<sub>x</sub> (Comma Detect) signal.

**Data Output**

Data is output on the DOUT<sub>x</sub>[0:9] outputs. The COM\_DET<sub>x</sub> signal is used to indicate the reception of a valid K28.5 character and is driven concurrent with the K28.5 character on the DOUT<sub>x</sub>[0:9] outputs.

The S2066 TTL outputs are optimized to drive 65Ω line impedances. Internal source matching provides good performance on unterminated lines of reasonable length.

**Parallel Output Clock Rate**

Two output clock modes are supported. When CMODE is HIGH, a complementary TTL clock at the data rate is provided on the RBC1/0<sub>x</sub> outputs. Data should be clocked on the rising edge of RBC1<sub>x</sub>. When CMODE is LOW, the S2066 outputs a complementary TTL clock at 1/2 the data rate in compliance with the the Gigabit Ethernet Physical Media Attachment (PMA) specification. Data should be latched on the rising edge of RBC1<sub>x</sub> and the rising edge of RBC0<sub>x</sub>.

If consecutive K28.5 characters are received, the S2066 RBC1/0<sub>x</sub> clock operates without glitches or loss of cycles.

**Table 4. Output Clock Modes**

Mode	CMODE	RBC1/0 <sub>x</sub> Freq.
Half Clock Mode	0	62.5 MHz
Full Clock Mode	1	125 MHz

**Table 5. Transmitter Input Signals Assignment and Description**

Pin Name	Level	I/O	Pin #	Description
DINA9 DINA8 DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	U15 U14 P12 R12 T13 T12 U13 P11 R11 T11	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TBCA or REFCLK. (See Table 2.)
TBCA	TTL	I	U12	Transmit Byte Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:9] into the S2066. When TMODE is Low, TBCA is ignored.
DINB9 DINB8 DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	R16 T16 R15 P14 T15 R14 U17 U16 P13 T14	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TBCB or REFCLK. (See Table 2.)
TBCB	TTL	I	R13	Transmit Byte Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:9] into the S2066. When TMODE is Low, TBCB is ignored.
DINC9 DINC8 DINC7 DINC6 DINC5 DINC4 DINC3 DINC2 DINC1 DINC0	TTL	I	N17 P17 M15 N16 M14 R17 P16 N15 T17 N14	Transmit Data for Channel C. Parallel data on this bus is clocked in on the rising edge of TBCC or REFCLK. (See Table 2.)
TBCC	TTL	I	P15	Transmit Byte Clock C. When TMODE is High, this signal is used to clock Data on DINC[0:9] into the S2066. When TMODE is Low, TBCC is ignored.

Note: All TTL inputs except REFCLK have internal pull-up networks.

**Table 5. Transmitter Input Signals Assignment and Description (Continued)**

Pin Name	Level	I/O	Pin #	Description
DIND9 DIND8 DIND7 DIND6 DIND5 DIND4 DIND3 DIND2 DIND1 DIND0	TTL	I	J16 K17 L17 K16 K15 K14 M17 L16 M16 L15	Transmit Data for Channel D. Parallel data on this bus is clocked in on the rising edge of TBCD or REFCLK. (See Table 2.)
TBCD	TTL	I	L14	Transmit Byte Clock D. When TMODE is High, this signal is used to clock Data on DIND[0:9] into the S2066. When TMODE is Low, TBCD is ignored.

Note: All TTL inputs except REFCLK have internal pull-up networks.

**Table 6. Transmitter Output Signals Assignment and Description**

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	A17 B17	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	C17 D17	High speed serial outputs for Channel B.
TXCP TXCN	Diff. LVPECL	O	F16 E17	High speed serial outputs for Channel C.
TXDP TXDN	Diff. LVPECL	O	F17 G17	High speed serial outputs for Channel D.
TCLKO	TTL	O	J14	TTL Output Clock at the parallel data rate. This clock is provided for use by up-stream circuitry.

**Table 7. Receiver Output Signals Assignment and Description**

Pin Name	Level	I/O	Pin #	Description
DOUTA9 DOUTA8 DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	G1 G3 J1 J3 J2 H1 H2 H3 F1 G2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1A in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
COM_DETA	TTL	O	F2	Channel A Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:9].
RBC1A RBC0A	TTL	O	K2 K1	Receive Byte Clocks. Parallel receive data, DOUTA[0:9] and COM_DETA are valid on the rising edge of RBC1A when in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
DOUTB9 DOUTB8 DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	K3 P2 R1 P1 M3 N2 M2 N1 L2 M1	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1B in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.
COM_DET B	TTL	O	L1	Channel B Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:9].
RBC1B RBC0B	TTL	O	U1 T1	Receive Byte Clocks. Parallel receive data, DOUTB[0:9] and COM_DET B are valid on the rising edge of RBC1B when in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.
DOUTC9 DOUTC8 DOUTC7 DOUTC6 DOUTC5 DOUTC4 DOUTC3 DOUTC2 DOUTC1 DOUTC0	TTL	O	T2 P3 R7 R6 T5 U3 T4 R5 U2 T3	Channel C Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1C in full clock mode and valid on the rising edge of both RBC1C and RBC0C in half clock mode.

**Table 7. Receiver Output Signals Assignment and Description (Continued)**

Pin Name	Level	I/O	Pin #	Description
COM_DETC	TTL	O	R2	Channel C Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTC[0:9].
RBC1C RBC0C	TTL	O	U5 U4	Receive Byte Clocks. Parallel receive data, DOUTC[0:9] and COM_DETC are valid on the rising edge of RBC1C when in full clock mode and valid on the rising edge of both RBC1C and RBC0C in half clock mode.
DOUTD9 DOUTD8 DOUTD7 DOUTD6 DOUTD5 DOUTD4 DOUTD3 DOUTD2 DOUTD1 DOUTD0	TTL	O	T6 T7 U11 R10 U9 R9 T9 U8 U7 T8	Channel D Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1D in full clock mode and valid on the rising edge of both RBC1D and RBC0D in half clock mode.
COM_DETD	TTL	O	U6	Channel D Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTD[0:9].
RBC1D RBC0D	TTL	O	T10 U10	Receive Byte Clocks. Parallel receive data, DOUTD[0:9] and COM_DETD are valid on the rising edge of RBC1D when in full clock mode and valid on the rising edge of both RBC1D and RBC0D in half clock mode.

**Table 8. Receiver Input Signals Assignment and Description**

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	D4 B3	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	C6 B5	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXCP RXCN	Diff. LVPECL	I	A8 A9	Differential LVPECL compatible inputs for channel C. RXCP is the positive input, RXCN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXDP RXDN	Diff. LVPECL	I	C11 B12	Differential LVPECL compatible inputs for channel D. RXDP is the positive input, RXDN is the negative. Internally biased to VDD-1.3V for AC coupled applications.

**Table 9. Receiver Control Signals Assignment and Description**

Pin Name	Level	I/O	Pin #	Description
LPEN	TTL	I	D14	Loopback Enable. When Low, input source for each channel is the high speed serial output. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RBC1/0x) rate equals 1/2 the data rate. When High, the parallel output clocks (RBC1/0x) rate is equal to the data rate.

Note: All TTL inputs except REFCLK have internal pull-up networks.

**Table 10. S2066 Mode Control Signal Assignment and Description**

Pin Name	Level	I/O	Pin #	Description
TESTMODE	TTL	I	E4	Test Mode Control. Keep Low for normal operation.
TMODE	TTL	I	B13	Transmit Mode Control. When TMODE is Low, REFCLK is used to clock data on DINx[0:9] into the S2066. When TMODE is High, TBCx is used to clock data into the S2066.
CLKSEL	TTL	I	C12	REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL=0, the REFCLK frequency should equal the parallel word rate. When CLKSEL=1, the REFCLK frequency should be 1/2 the parallel data rate.
REFCLK	TTL	I	H17	Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data.
RESET	TTL	I	C15	When Low, the S2066 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2066 operates normally.
RATE	TTL	I	D12	When Low, the S2066 operates with the serial output rate equal to the VCO frequency. When High, the S2066 operates with the VCO internally divided by 2 for all functions.

Note: All TTL inputs except REFCLK have internal pull-up networks.

**Table 11. Power and Ground Signals Assignment and Description**

Pin Name	Qty.	Pin #	Description
VDDA	5	A1, A6, A13, A16, C8	Analog Power (VDD) low noise.
VSSA	5	B7, B8, B15, C4, D11	Analog Ground (VSS).
VDD	5	A12, A15, B4, B6, D9	Power for high speed circuitry (VDD).
VSS VSSSUB	10	A2, A4, A7, A11, A14, B10, B14, C13, D6, D8	Ground for high speed circuitry (VSS).
PECLPWR	2	E15 G16	PECL Power (VDD).
PECLGND	2	C16, H16	PECL Ground (VSS).
DIGPWR	6	B1, B2, E3, J17, L4, P9	Core circuitry Power (VDD).
DIGGND	8	C1, C3, D2, F4, J15, N4, P10, R3	Core circuitry Ground (VSS).
TTLPWR	8	E1, G4, H4, K4, N3, P5, P7, P8	Power for TTL I/O (VDD).
TTLGND	10	D1, E2, F3, J4, L3, M4, P4, P6, R4, R8	Ground for TTL I/O (VSS).
PWR	9	A3, B9, B11, B16, C5, C9, D3, D7, D10	Power.
GND	15	A5, A10, C7, C10, D5, D15, D16, E14, E16, F14, F15, G14, G15, H14, H15	Ground.
CAP1 CAP2	2	D13 C14	Pins for external loop filter capacitor.



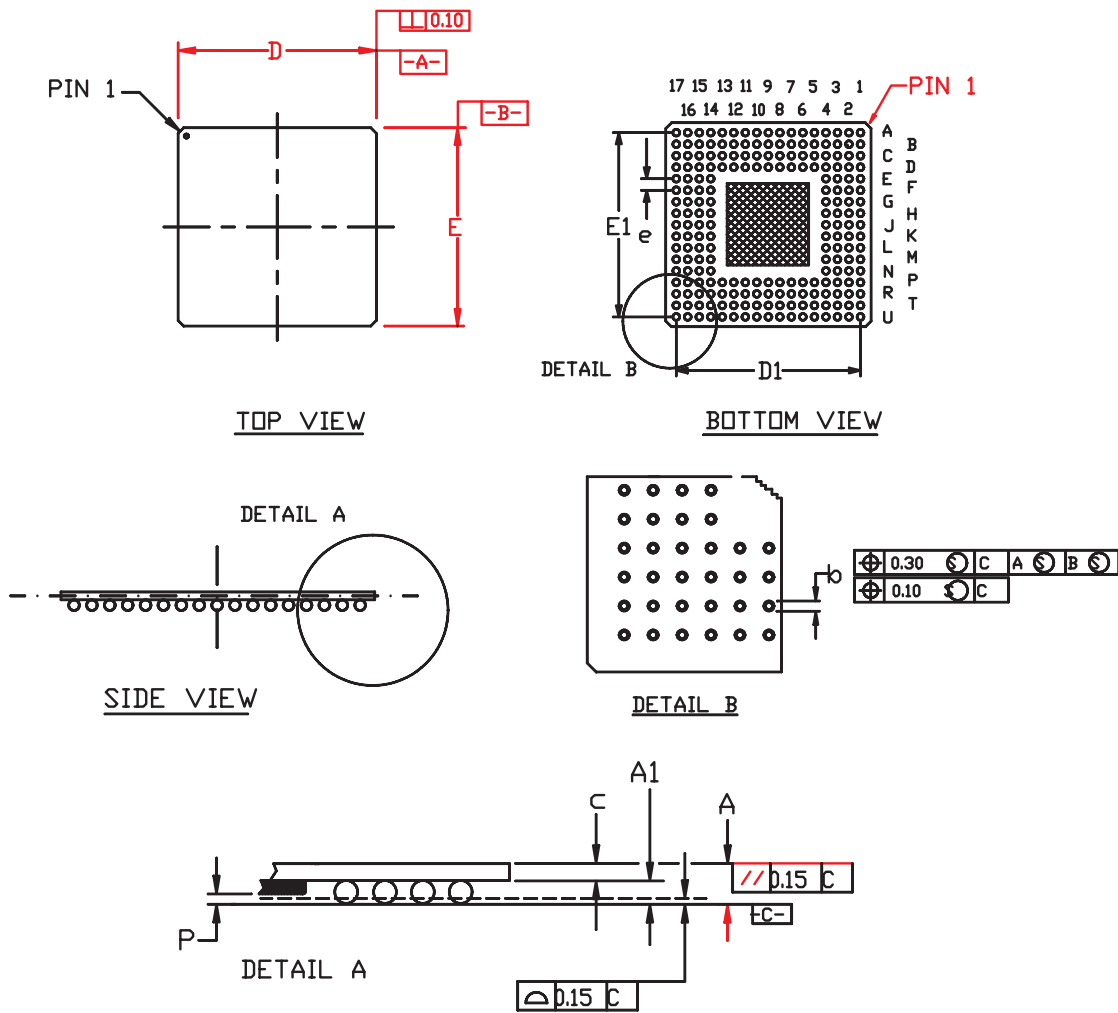
**Figure 7. S2066 Pinout (Bottom View)**

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	VDDA	DIGPWR	DIGGND	TTLGND	TTLPWR	DOUTA1	DOUTA9	DOUTA4	DOUTA7	RBC0A	COM_DET B	DOUTB0	DOUTB2	DOUTB6	DOUTB7	RBC0B	RBC1B
2	VSSSUB	DIGPWR	CMODE	DIGGND	TTLGND	COM_DET A	DOUTA0	DOUTA3	DOUTA5	RBC1A	DOUTB1	DOUTB3	DOUTB4	DOUTB8	COM_DET C	DOUTC9	DOUTC1
3	PWR	RXAN	DIGGND	PWR	DIGPWR	TTLGND	DOUTA8	DOUTA2	DOUTA6	DOUTB9	TTLGND	DOUTB5	TTLPWR	DOUTC8	DIGGND	DOUTC0	DOUTC4
4	VSS	VDD	VSSA	RXAP	TEST MODE	DIGGND	TTLPWR	TTLPWR	TTLGND	TTLPWR	DIGPWR	TTLGND	DIGGND	TTLGND	TTLGND	DOUTC3	RBC0C
5	GND	RXBN	PWR	GND										TTLPWR	DOUTC2	DOUTC5	RBC1C
6	VDDA	VDD	RXBP	VSS										TTLGND	DOUTC6	DOUTD9	COM_DET D
7	VSSSUB	VSSA	GND	PWR										TTLPWR	DOUTC7	DOUTD8	DOUTD1
8	RXCP	VSSA	VDDA	VSSSUB										TTLPWR	TTLGND	DOUTD0	DOUTD2
9	RXCN	PWR	PWR	VDD										DIGPWR	DOUTD4	DOUTD3	DOUTD5
10	GND	VSS	GND	PWR										DIGGND	DOUTD6	RBC1D	RBC0D
11	VSS	PWR	RXDP	VSSA										DINA2	DINA1	DINA0	DOUTD7
12	VDD	RXDN	CLKSEL	RATE										DINA7	DINA6	DINA4	TBCA
13	VDDA	TMODE	VSSSUB	CAP1										DINB1	TBCB	DINA5	DINA3
14	VSSSUB	VSS	CAP2	LPEN	GND	GND	GND	GND	TCLKO	DIND4	TBCD	DINC5	DINC0	DINB6	DINB4	DINB0	DINA8
15	VDD	VSSA	RESET	GND	PECL PWR	GND	GND	GND	DIGGND	DIND5	DIND0	DINC7	DINC2	TBCC	DINB7	DINB5	DINA9
16	VDDA	PWR	PECLGND	GND	GND	TXCP	PECL PWR	PECLGND	DIND9	DIND6	DIND2	DIND1	DINC6	DINC3	DINB9	DINB8	DINB2
17	TXAP	TXAN	TXBP	TXBN	TXCN	TXDP	TXDN	REFCLK	DIGPWR	DIND8	DIND7	DIND3	DINC9	DINC8	DINC4	DINC1	DINB3

Figure 8. S2066 Pinout (Top View)

U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
RBC1B	RBC0B	DOUTB7	DOUTB6	DOUTB2	DOUTB0	COM_DET B	RBC0A	DOUTA7	DOUTA4	DOUTA9	DOUTA1	TTL PWR	TTL GND	DIG GND	DIG PWR	VDDA	1
DOUTC1	DOUTC9	COM_DET C	DOUTB8	DOUTB4	DOUTB3	DOUTB1	RBC1A	DOUTA5	DOUTA3	DOUTA0	COM_DET A	TTL GND	DIG GND	C MODE	DIG PWR	VSS SUB	2
DOUTC4	DOUTC0	DIG GND	DOUTC8	TTL PWR	DOUTB5	TTL GND	DOUTB9	DOUTA6	DOUTA2	DOUTA8	TTL GND	DIG PWR	PWR	DIG GND	RX AN	PWR	3
RBC0C	DOUTC3	TTL GND	TTL GND	DIG GND	TTL GND	DIG PWR	TTL PWR	TTL GND	TTL PWR	TTL PWR	DIG GND	TEST MODE	RX AP	VSSA	VDD	VSS	4
RBC1C	DOUTC5	DOUTC2	TTL PWR										GND	PWR	RX BN	GND	5
COM_DET D	DOUTD9	DOUTC6	TTL GND										VSS	RX BP	VDD	VDDA	6
DOU D1	DOU D8	DOU C7	TTL PWR										PWR	GND	VSSA	VSS SUB	7
DOU D2	DOU D0	TTL GND	TTL PWR										VSS SUB	VDDA	VSSA	RX CP	8
DOU D5	DOU D3	DOU D4	DIG PWR										VDD	PWR	PWR	RX CN	9
RBC0D	RBC1D	DOU D6	DIG GND										PWR	GND	VSS	GND	10
DOU D7	DINA0	DINA1	DINA2										VSSA	RX DP	PWR	VSS	11
TBCA	DINA4	DINA6	DINA7										RATE	CLK SEL	RX DN	VDD	12
DINA3	DINA5	TBCB	DIN B1										CAP1	VSS SUB	T MODE	VDDA	13
DINA8	DIN B0	DIN B4	DIN B6	DINC0	DINC5	TBCD	DIND4	TCL K0	GND	GND	GND	GND	LPEN	CAP2	VSS	VSS SUB	14
DINA9	DIN B5	DIN B7	TBCC	DINC2	DINC7	DIND0	DIND5	DIG GND	GND	GND	GND	PECL PWR	GND	RESET	VSSA	VDD	15
DIN B2	DIN B8	DIN B9	DINC3	DINC6	DIND1	DIND2	DIND6	DIND9	PECL GND	PECL PWR	TXCP	GND	GND	PECL GND	PWR	VDDA	16
DIN B3	DINC1	DINC4	DINC8	DINC9	DIND3	DIND7	DIND8	DIG PWR	REFCLK	TXDN	TXDP	TXCN	TXBN	TXBP	TXAN	TXAP	17

Figure 9. 208 TBGA Package



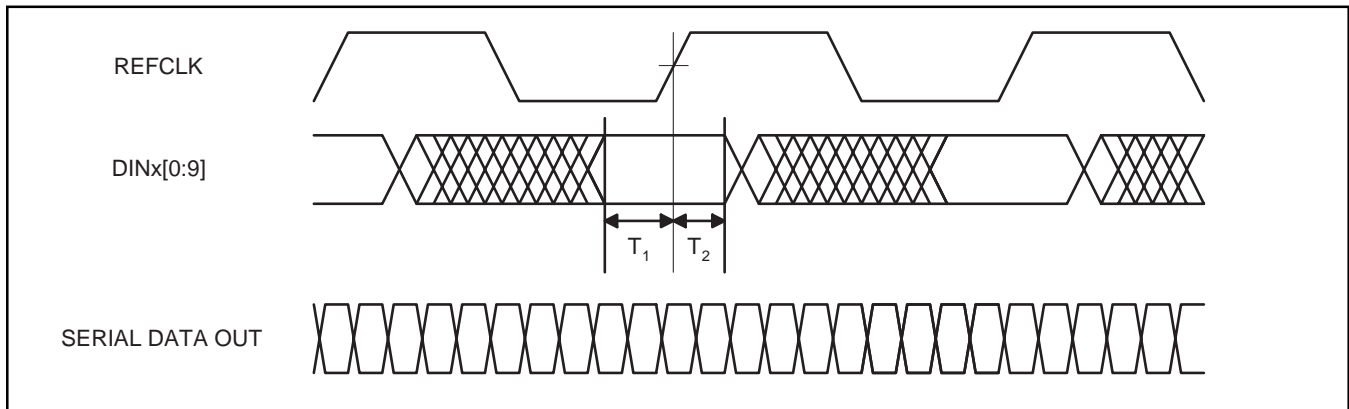
DIMENSIONS (are in millimeters)

UNIT	A	A <sub>1</sub>	D	D <sub>1</sub>	E	E <sub>1</sub>	P	b	c	e
MIN	1.45	0.60	22.80	20.32 BSC.	22.80	20.32 BSC.		0.65	0.85	1.27 BSC.
NOM	1.55	0.65	23.00		23.00			0.75	0.90	
MAX	1.65	0.70	23.20		23.20		0.25	0.85	0.95	

**Thermal Management**

Device	$\Theta_{ja}$ (Still Air)	$\Theta_{jc}$
S2066	17.7° C/W	3.5° C/W

**Figure 10. Transmitter Timing (REFCLK Mode, TMODE = 0)**

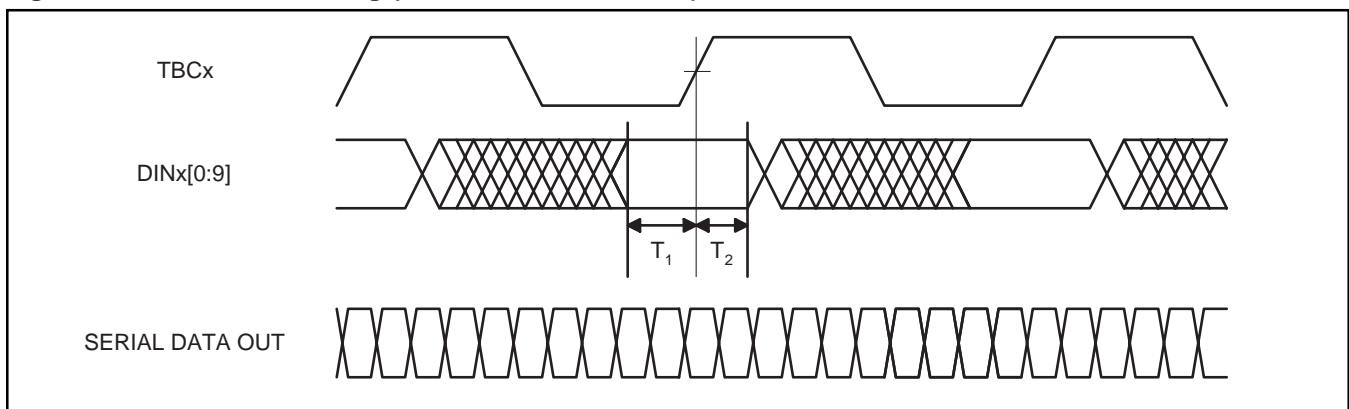


**Table 12. S2066 Transmitter Timing (REFCLK Mode, TMODE = 0)**

Parameters	Description	Min	Max	Units	Conditions
$T_1$	Data Setup w.r.t. $\uparrow$ REFCLK	0.5	-	ns	See Note 1.
$T_2$	Data Hold w.r.t. $\uparrow$ REFCLK	1.3	-	ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

**Figure 11. Transmitter Timing (TBC Mode, TMODE = 1)**



**Table 13. S2066 Transmitter Timing (TBC Mode, TMODE = 1)**

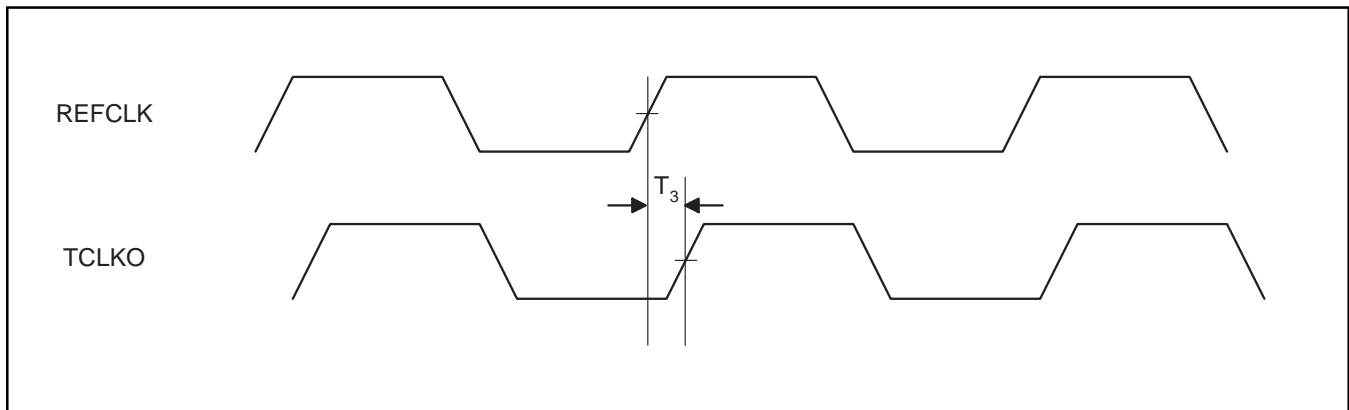
Parameters	Description	Min	Max	Units	Conditions
$T_1$	Data Setup w.r.t. $\uparrow$ TBC	1.0	-	ns	See Note 1.
$T_2$	Data Hold w.r.t. $\uparrow$ TBC	0.5	-	ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

**Table 14. S2066 Transmitter Timing**

Parameters	Description	Min	Max	Units	Conditions
$T_{SDR}, T_{SDF}$	Serial Data Rise and Fall	-	300	ps	20% - 80%, tested on sample basis. 4.5 k $\Omega$ to ground.
$T_J$	Serial Data Output total jitter (p-p)	-	192	ps	Peak-to-peak, measured on sample basis. Measured with $\pm$ K28.5 or 2 <sup>7</sup> -1 pattern at 1.25 GHz.
$T_{DJ}$	Serial Data Output deterministic jitter (p-p)	-	80	ps	Peak-to-peak, tested on a sample basis. Measured with $\pm$ K28.5 pattern at 1.25 GHz.

**Figure 12. TCLKO Timing**

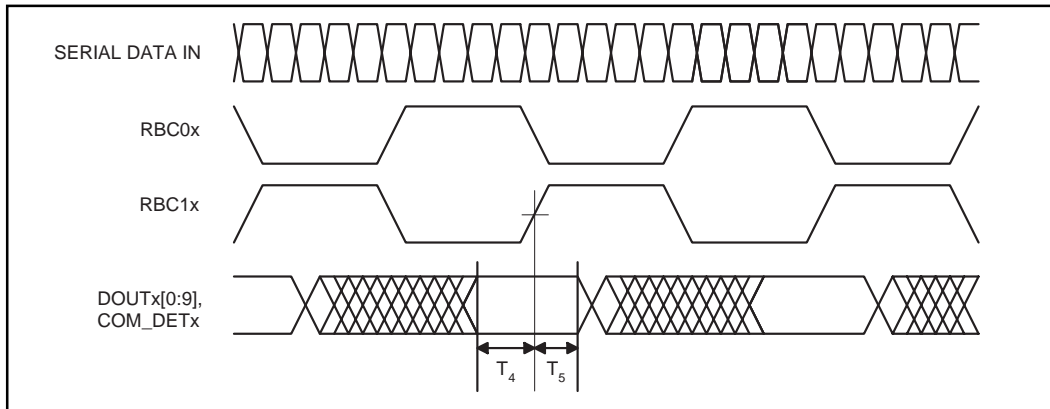


**Table 15. S2066 Transmitter (TCLKO Timing)**

Parameters	Description	Min	Max	Units	Conditions
$T_3$	TCLKO $\uparrow$ w.r.t. $\uparrow$ REFCLK	2.0	7.5	ns	
TCLKO Duty Cycle		40%	60%	%	

Note: Measurements are made at 1.4V level of clocks.

**Figure 13. Receiver Timing (Full Clock Mode, CMODE = 1)**

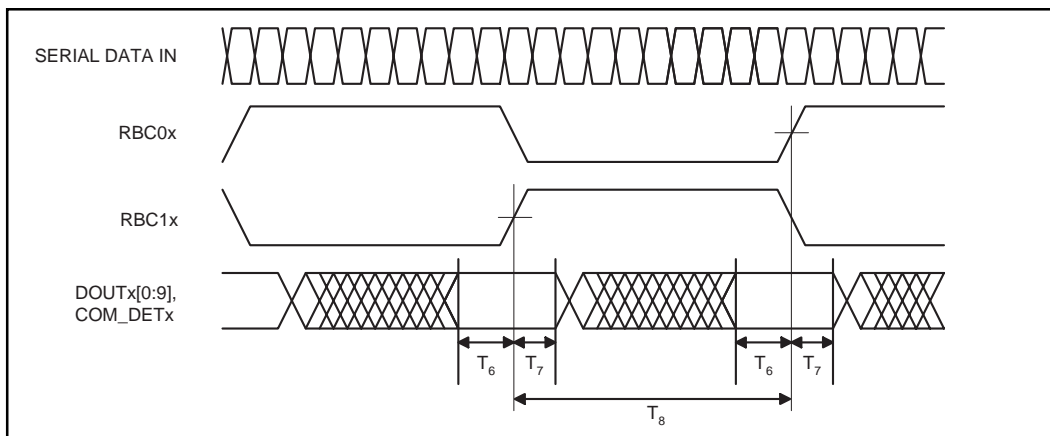


**Table 16. S2066 Receiver Timing (Full Clock Mode, CMODE = 1)**

Parameters	Description	Min	Max	Units	Conditions
$T_4$	Data Setup w.r.t. $\uparrow$ RBC1x	2.75	-	ns	See Note 1.
$T_5$	Data Hold w.r.t. $\uparrow$ RBC1x	2.0	-	ns	
RBC1/0x Duty Cycle		40	60	%	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

**Figure 14. Receiver Timing (Half Clock Mode, CMODE = 0)**



**Table 17. S2066 Receiver Timing (Half Clock Mode, CMODE = 0)**

Parameters	Description	Min	Max	Units	Conditions
$T_6$	Data Setup w.r.t. $\uparrow$ RBC1/0x	2.5	-	ns	See Note 1.
$T_7$	Data Hold w.r.t. $\uparrow$ RBC1/0x	2.0	-	ns	
$T_8$	Time from RBC1x rise to RBC0x rise	7.8	8.82	ns	
RBC1/0x Duty Cycle		40	60	%	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

**Table 18. S2066 Receiver Timing**

Parameters	Description	Min	Max	Units	Conditions
$T_{RCR}, T_{RCF}$	RBC1, RBC0 Rise and Fall Time	-	3.0	ns	Measured +.8V to +2.0V. See Figure 17.
$T_{DR}, T_{DF}$	Data Output Rise and Fall Time		3.0	ns	Measured +.8V to +2.0V. See Figure 16.
$T_{LOCK}$ (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.25 Gbps)	-	175	$\mu$ s	After power up.
$T_J$	Total Input Jitter Tolerance	599	-	ps	As specified in IEEE 802.3z.
$T_{DJ}$	Deterministic Input Jitter Tolerance	370	-	ps	As specified in IEEE 802.3z.

**OTHER OPERATING MODES**

**Loopback Mode**

When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver. Loopback mode can be simultaneously enabled for all four channels using the loopback-enable input, LPEN.

The loopback mode provides the ability to perform system diagnostics and off-line testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. Loopback is enabled when LPEN = 1.

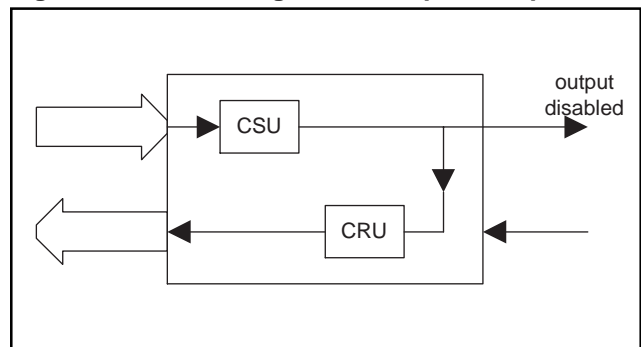
Note that the high speed outputs are disabled during loopback operation.

**Test Modes**

The S2066 has a testability input to aid in functional testing of the device. The test mode is entered when TESTMODE is HIGH and TBCB is HIGH.

The RESET pin is used to initialize the transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization). Note that Reset does not disable the TCLKO output unless the TBCB input is HIGH.

**Figure 15. S2066 Diagnostic Loopback Operation**



**Table 19. Absolute Maximum Ratings**

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	° C
Junction Temperature Under Bias	-55		150	° C
Storage Temperature	-65		150	° C
Voltage on VDD with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any PECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage, TTL I/O		2000		V
Static Discharge Voltage, PECL I/O		1500		V

**Table 20. Recommended Operating Conditions**

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	° C
Junction Temperature Under Bias			130	° C
Voltage on any Power Pin with Respect to GND/VSS	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	VDD -2V		VDD	V

**Table 21. Reference Clock Requirements**

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD <sub>1-2</sub>	Symmetry	40	60	%	Duty Cycle at 50% pt.
T <sub>RCR</sub> , T <sub>RCF</sub>	REFCLK Rise and Fall Time		2	ns	20% - 80%.
—	Jitter		80	ps	Peak-to-Peak, 77% data eye.



**Table 22. DC Characteristics**

Parameters	Description	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min $I_{OH}$ = -4mA
$V_{OL}$	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min $I_{OL}$ = 4mA
$V_{IH}$	Input High Voltage (TTL)	2.0			V	
$V_{IL}$	Input Low Voltage (TTL)	GND		0.8	V	
$I_{IH}$	Input High Current (TTL)			40	$\mu$ A	$V_{IN}$ = 2.4V, VDD = Max
$I_{IL}$	Input Low Current (TTL)			600	$\mu$ A	$V_{IN}$ = 0.8V, VDD = Max
IDD	Supply Current		700	895	mA	1010 pattern.
$P_D$	Power Dissipation		2.3	3.1	W	1010 pattern.
$V_{DIFF}$	Min. differential input voltage swing for differential PECL inputs	100		2200	mV	See Figure 19.
$\Delta V_{OUT}$	Differential Serial Output Voltage Swing	1200	1900	2200	mV	AC coupled with 4.5 k $\Omega$ pulldown. See Figure 18.
$C_{IN}$	Input Capacitance			3	pf	

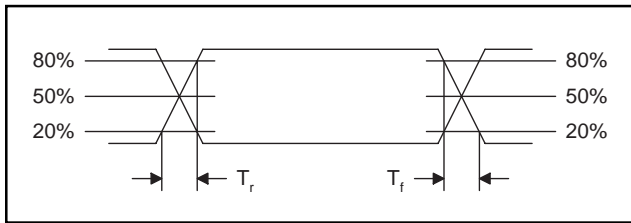
### OUTPUT LOAD

The S2066 serial outputs require a resistive load to set the output current. The recommended resistor value is 4.5 k $\Omega$  to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.

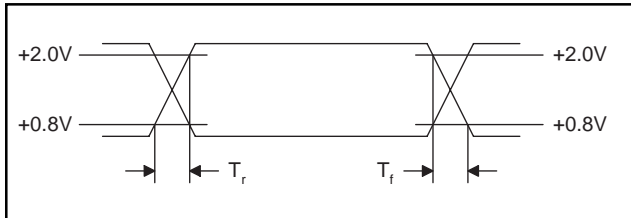
### ACQUISITION TIME

With the input eye diagram shown in Figure 21, the S2066 will recover data with  $\leq$  IE-9 BER within the time specified by  $T_{LOCK}$  in Table 18 after an instantaneous phase shift of the incoming data.

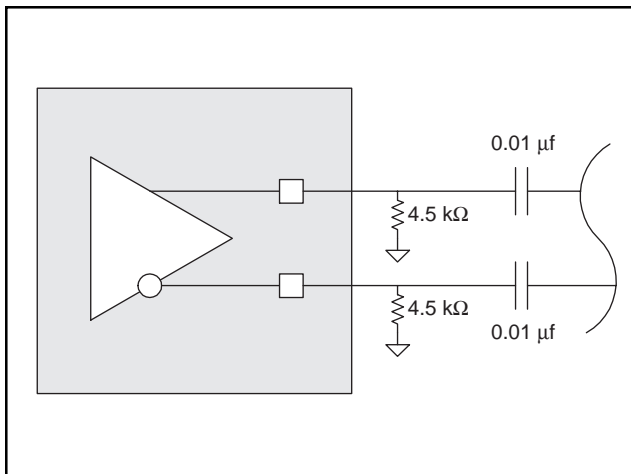
**Figure 16. Serial Input/Output Rise and Fall Time**



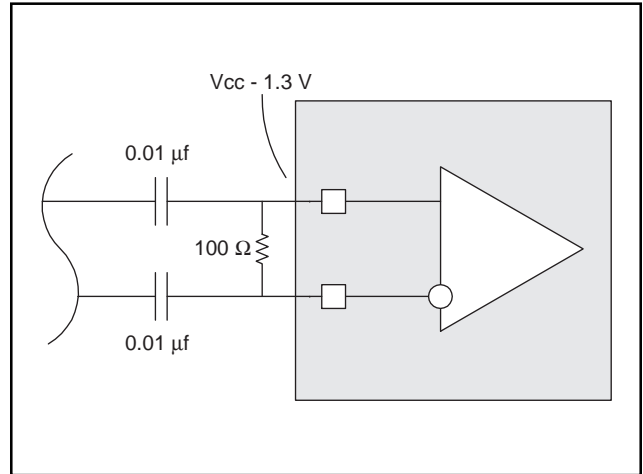
**Figure 17. TTL Input/Output Rise and Fall Time**



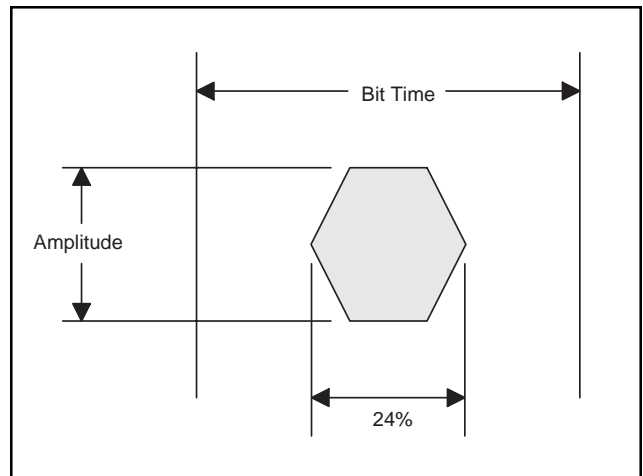
**Figure 18. Serial Output Load**



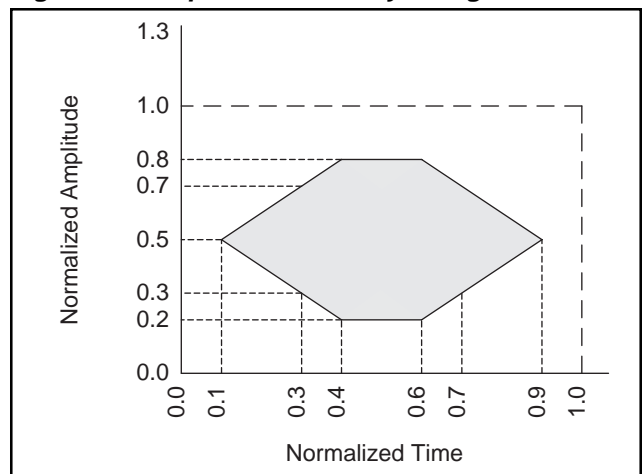
**Figure 19. High Speed Differential Inputs**



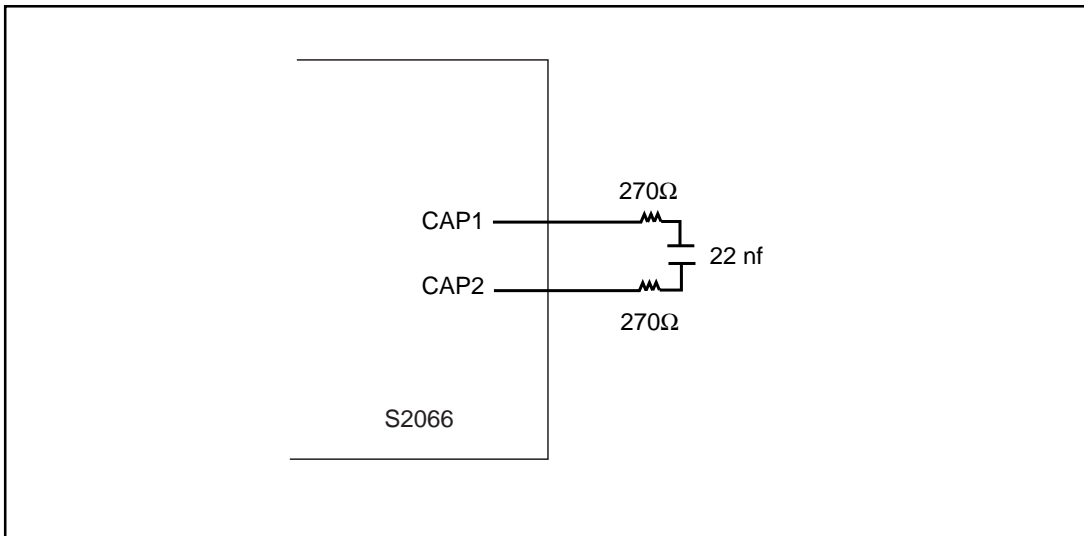
**Figure 20. Receiver Input Eye Diagram Jitter Mask**



**Figure 21. Acquisition Time Eye Diagram**

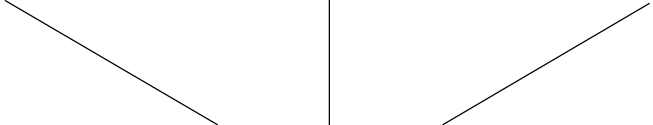


*Figure 22. Loop Filter Capacitor Connections*



**Ordering Information**

<b>GRADE</b>	<b>PART NO.</b>	<b>PACKAGE</b>
S- Commercial	2066	A-208 TBGA


  
X      XXXX      X  
Grade    Part No.    Package



**Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121**

**Phone: (619) 450-9333 • (800) 755-2622 • Fax: (619) 450-9885**

**<http://www.amcc.com>**

AMCC reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

AMCC does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.

AMCC reserves the right to ship devices of higher grade in place of those of lower grade.

AMCC SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

AMCC is a registered trademark of Applied Micro Circuits Corporation.  
Copyright © 2000 Applied Micro Circuits Corporation

D169/R261