



# **Resonant Fluorescent Lamp Driver**

# **FEATURES**

- 1µA ICC when Disabled
- PWM Control for LCD Supply
- Zero Voltage Switched (ZVS) on Push-Pull Drivers
- Open Lamp Detect Circuitry
- 4.5V to 20V Operation
- Non-saturating Transformer Topology
- Smooth 100% Duty Cycle on Buck PWM and 0% to 95% on Flyback PWM

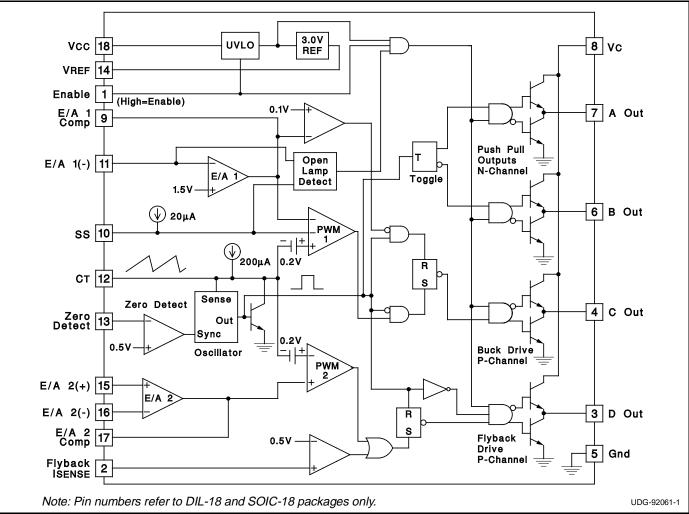
## DESCRIPTION

The UC1871 Family of IC's is optimized for highly efficient fluorescent lamp control. An additional PWM controller is integrated on the IC for applications requiring an additional supply, as in LCD displays. When disabled the IC draws only 1 $\mu$ A, providing a true disconnect feature, which is optimum for battery powered systems. The switching frequency of all outputs are synchronized to the resonant frequency of the external passive network, which provides Zero Voltage Switching on the Push-Pull drivers.

Soft-Start and open lamp detect circuitry have been incorporated to minimize component stress. An open lamp is detected on the completion of a soft-start cycle.

The Buck controller is optimized for smooth duty cycle control to 100%, while the flyback control ensures a maximum duty cycle of 95%.

Other features include a precision 1% reference, under voltage lockout, flyback current limit, and accurate minimum and maximum frequency control.



# **BLOCK DIAGRAM**

#### **ABSOLUTE MAXIMUM RATINGS**

Analog Inputs –0.3 to +10V
Vcc, Vc Voltage +20V
Zero Detect Input Current
High Impedance Source +10mA
Zero Detect
Low Impedance Source +20V
Power Dissipation at TA = 25°C 1W
Storage Temperature

DIL-18, SOIC-18 (TOP VIEW) J or N, DW Package Enable 1 18 Vcc Flyback ISENSE 2 17 E/A 2 Comp D Out 3 16 E/A 2(-) C Out 4 15 E/A 2(+) 14 VREF Gnd 5 13 Zero 13 Detect B Out 6 A Out 7 12 CT Vc 8 11 E/A 1(-) 10 SS E/A 1 Comp 9

#### Note 1: Currents are positive into, negative out of the specified terminal.

Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

#### **CONNECTION DIAGRAMS**

PLCC-20 (Top View)	PACKAGE PIN FU	PACKAGE PIN FUNCTION	
2 Package	FUNCTION	PIN	
-	Gnd	1	
	B Out	2	
	A Out	3	
	Vc	4	
3 2 1 20 19	E/A 1 Comp	5	
4 18	SS	6	
	E/A 1(-)	7	
<b>⊈5 17</b> ₽	N/C	8	
<b>≬6 16</b> ⊉	Ст	9	
7 15	Zero Detect	10	
8 14	N/C	11	
9 10 11 12 13	Vref	12	
	E/A 2(+)	13	
	E/A 2(-)	14	
	E/A 2 Comp	15	
	Vcc	16	
	Enable	17	
	Flyback Isense	18	
	D Out	19	
	C Out	20	

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these parameters apply for TA = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; Vcc = 5V, VC = 15V, VENABLE = 5V, CT = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TJ=25°C	2.963	3.000	3.037	V
	Overtemp	2.940	3.000	3.060	V
Line Regulation	Vcc = 4.75V to 18V			10	mV
Load Regulation	lo=0 to -5mA			10	mV
Oscillator Section					
Free Running Freq	TJ=25°C	57	68	78	kHz
Max Sync Frequency	TJ=25°C	160	200	240	kHz
Charge Current	VCT = 1.5V	180	200	220	μA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp 1 Section					
Input Voltage	Vo = 2V	1.445	1.475	1.505	V
Input Bias Current			-0.4	-2	μA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	VEA(-) = 1.3V	3.1	3.5	3.9	V
Output Low	VEA(-) = 1.7V		0.1	0.2	V
Output Source Current	VEA(-) = 1.3V, Vo = 2V	-350	-500		μA
Output Sink Current	VEA(-) = 1.7V, Vo = 2V	10	20		mA
Common Mode Range		0		VIN-1V	V
Unity Gain Bandwidth	TJ = 25°C (Note 4)		1		MHz
Maximum Source Impedance	Note 5			100k	Ω

# UC1871 UC2871 UC3871

#### **ELECTRICAL** CHARACTERISTICS (cont.)

Unless otherwise stated, these parameters apply for  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; Vcc = 5V, Vc = 15V, VENABLE = 5V, CT = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Lamp Detect Section					
Soft Start Threshold	VEA(-) = OV	2.9	3.4	3.8	V
Error Amp Threshold	VSS = 4.2V	0.7	1.0	1.3	V
Soft Start Current	Vss = 2V	10	20	40	μA
Error Amp 2 Section					
Input Offset Voltage	Vo = 2V		0	10	mV
Input Bias Current			-0.2	-1	μA
Input Offset Current				0.5	μA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	VID = 100mV, Vo = 2V	3.6	4	4.4	V
Output Low	VID = -100mv, Vo = 2V		0.1	0.2	V
Output Source Current	VID = 100mV, VO = 2V	-350	-500		μA
Output Sink Current	VID = -100mV, VO = 2V	10	20		mA
Common Mode Range		0		VIN-2V	V
Unity Gain Bandwidth	TJ = 25°C (Note 4)		1		MHz
Isense Section				•	-
Threshold		0.475	0.525	0.575	V
Output Section		•			
Output Low Level	IOUT = 0, Outputs A and B		0.05	0.2	V
	IOUT = 10mA		0.1	0.4	V
	IOUT = 100mA		1.5	2.2	V
Output High Level	IOUT = 0, Outputs C and D	14.7	14.9		V
	IOUT = -10mA	13.5	14.3		V
	IOUT = -100mA	12.5	13.5		V
Rise Time	$T_J = 25^{\circ}C$ , $CI = 1nF(Note 4)$		30	80	ns
Fall Time	$T_J = 25^{\circ}C, CI = 1nF(Note 4)$		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	VEA1(-) = 1V	100			%
Out C Min Duty Cycle	VEA1(-) = 2V			0	%
Out D Max Duty Cycle	VEA2(+)- VEA2(-) = 100mV		92	96	%
Out D Min Duty Cycle	VEA2(+)- VEA2(-) = -100mV			0	%
Under Voltage Lockout Section		•			
Start-Up Threshold		3.7	4.2	4.5	V
Hysterisis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	VENABLE = 5V		150	400	μA
Supply Current Section					-
VCC Supply Current	Vcc = 20V		8	14	mA
VC Supply Current	Vc=20V		7	12	mA
ICC Disabled	VCC = 20V, VENABLE = 0V		1	10	μA

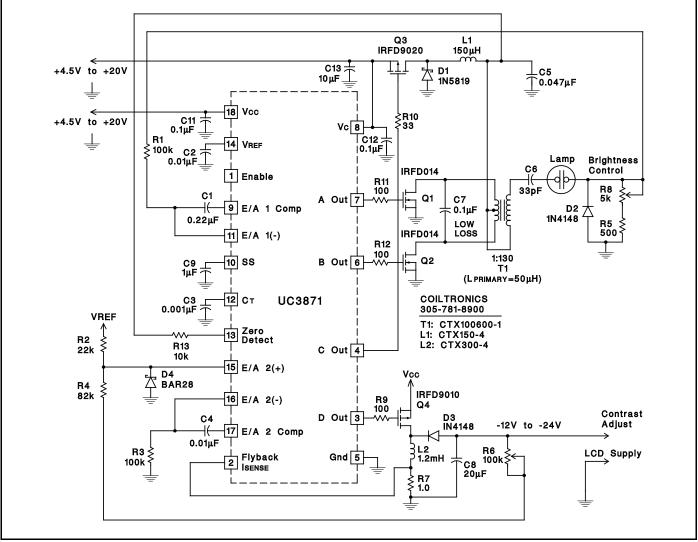
Note 3: Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.

Note 4: Guaranteed by design but not 100% tested in production.

Note 5: Impedance below specified maximum guarantees proper operation of the Open Lamp Detect.

# UC1871 UC2871 UC3871

## **TYPICAL APPLICATION**





#### **APPLICATION INFORMATION**

Figure 1 shows a complete application circuit using the UC3871 Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

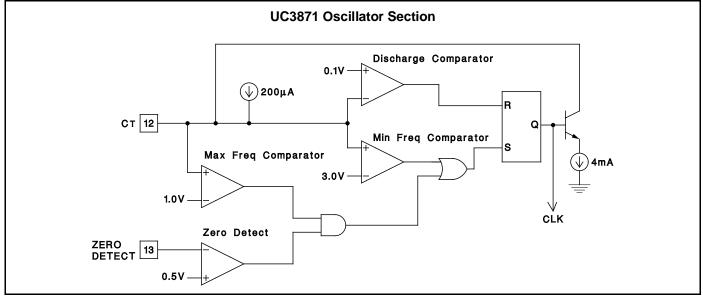
The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect

comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The  $200\mu$ A current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

# UC1871 UC2871 UC3871

#### **APPLICATION INFORMATION (cont.)**



#### Figure 2

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shutdown, the IC typically draws less than 1 $\mu$ A. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-bycycle current limiting for added protection.

UC1871 Open Lamp Detect Circuitry  $E/A \ 1(-) 11 + E/A \ 1.5V + E/A$ 

Other features are included to minimize external circuitry

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TEXAS **RUMENTS** www.ti.com

7-May-2007

# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9462201MVA	OBSOLETE			18		TBD	Call TI	Call TI
5962-9462201Q2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC1871J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1871J883B	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1871L883B	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI
UC2871DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2871DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2871DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2871DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2871N	ACTIVE	PDIP	Ν	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2871NG4	ACTIVE	PDIP	Ν	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2871Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2871QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2871QTR	ACTIVE	PLCC	FN	20	1000	TBD	CU SN	Level-2-220C-1 YEAR
UC3871DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3871DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3871DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3871DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3871N	ACTIVE	PDIP	Ν	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3871NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3871Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3871QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3871QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3871QTRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

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**OBSOLETE:** TI has discontinued the production of the device.



(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MLCC006B - OCTOBER 1996

## FK (S-CQCC-N\*\*)

#### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



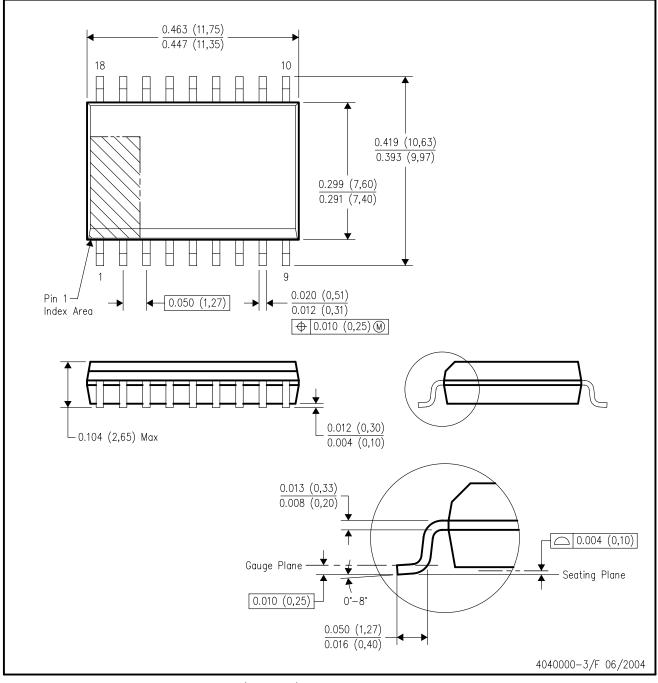
NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G18)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AB.



# **MECHANICAL DATA**

MPLC004A - OCTOBER 1994

#### PLASTIC J-LEADED CHIP CARRIER

# FN (S-PQCC-J\*\*)



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C. Falls within JEDEC MS-018



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